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R8C/L3AA Group

Timer RA (Timer Mode)

1. Abstract

This document describes the setting method and an application example of the R8C/L3AA Group's timer RA timer mode.

2. Introduction

The application example described in this document applies to the following MCU:

- MCU : R8C/L3AA Group
- XIN clock frequency : 20 MHz

The sample program in this application note can be used with other R8C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the sample program described in this application note.

3. Application Example

3.1 Program Outline

Count source f8 is counted in the prescaler register (TRAPRE) and timer RA register (TRA). The timer RA interrupt is generated every 1 ms and interrupts are counted to 10.

Settings

- TRAPRE = 249 TRA = 9
- The XIN clock (20 MHz) is selected as the system clock.

Calculation formula of settings

$$\begin{aligned}
 1 \text{ ms} &= (1 \div f8) \times (\text{TRAPRE} + 1) \times (\text{TRA} + 1) \\
 &= \{1 \div (20 \text{ MHz} \div 8)\} \times 250 \times 10 \\
 &= (4 \times 10^{-7}) \text{ s} \times 2500
 \end{aligned}$$

Figure 3.1 shows a Block Diagram.

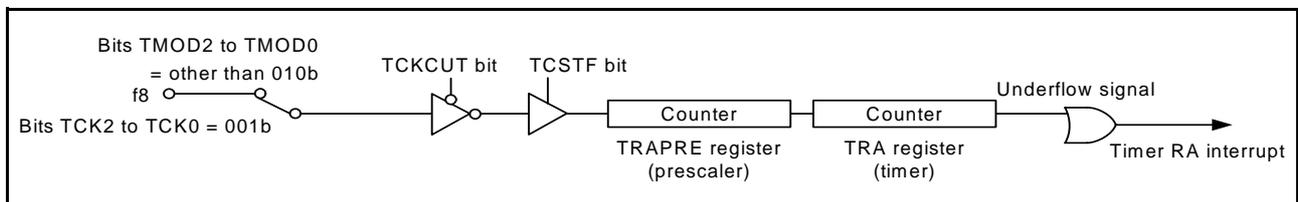


Figure 3.1 Block Diagram

3.2 Memory

Table 3.1 Memory

Memory	Size	Remarks
ROM	129 bytes	In the rej05b1289_src.c module
RAM	2 bytes	In the rej05b1289_src.c module
Maximum user stack	10 bytes	
Maximum interrupt stack	18 bytes	

Memory size varies depending on the C compiler version and compile options.

The above applies to the following conditions:

- C compiler: M16C/60, 30, 20, 10, and Tiny, and R8C/Tiny Series Compiler V.5.44 Release 00
- Compile option: -c -finfo -dir "\$(CONFIGDIR)" -R8CE

4. Software Outline

This section shows the setting procedures and values to set the example described in section 3. **Application Example.** Refer to the latest **R8C/L3AA Group Hardware Manual** for details on individual registers.

The × in the register's Setting Value represents bits not used in this application, blank spaces represent bits that do not change, and the hyphen represents reserved bits or bits that have nothing assigned.

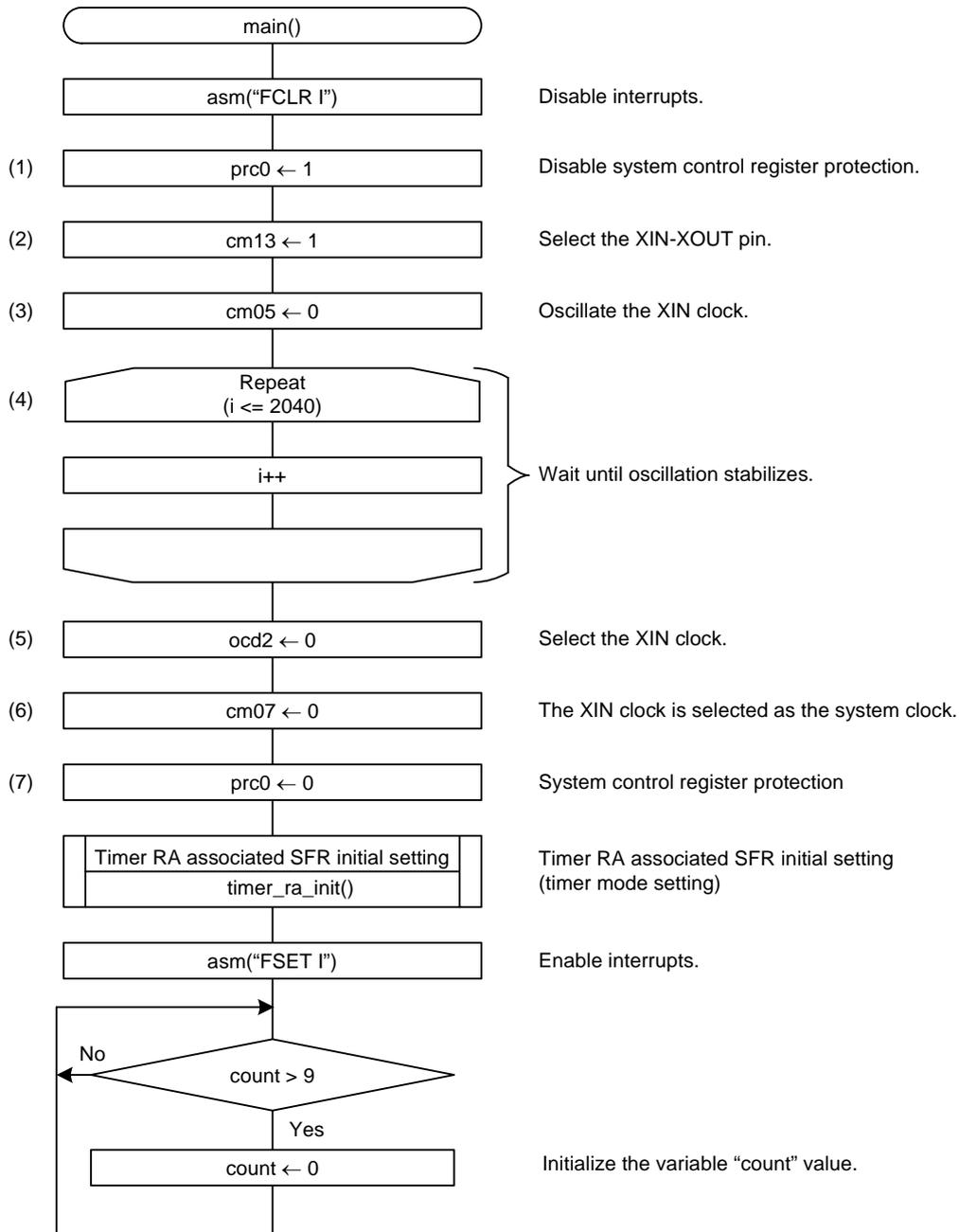
4.1 Function Tables

Declaration	void timer_ra_init(void)		
Outline	Timer RA associated SFR initial setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Timer RA associated SFR registers are initialized.		

Declaration	void timer_ra_interrupt(void)		
Outline	Timer RA interrupt handling		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	Count		Count number of timer RA interrupts generated.
Returned value	Type	Value	Meaning
	None	—	—
Function	An interrupt process in a 1 ms period which is generated by the TRA register underflow. The variable count increments by one.		

4.2 Main Function

• Flowchart



• Register Settings

(1) Enable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	—	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 1: Write enabled	R/W

(2) Select the XIN-XOUT pin.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	x	x	—	x	1	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b3	CM13	Port/XIN-XOUT switch bit	1: XIN-XOUT pin	R/W

(3) Oscillate the XIN clock.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value			0	x	x	x	x	—

Bit	Symbol	Bit Name	Function	R/W
b5	CM05	XIN clock (XIN-XOUT) stop bit	0: XIN clock oscillates	R/W

(4) Wait until oscillation stabilizes.

(5) Select the XIN clock.

Oscillation Stop Detection Register (OCD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—	—	x	0	x	x

Bit	Symbol	Bit Name	Function	R/W
b2	OCD2	On-chip oscillator clock select bit	0: XIN clock selected	R/W

(6) Select the XIN clock as the system clock.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	0			x	x	x	x	—

Bit	Symbol	Bit Name	Function	R/W
b7	CM07	System clock select bit	0: XIN clock or on-chip oscillator clock	R/W

(7) Disable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

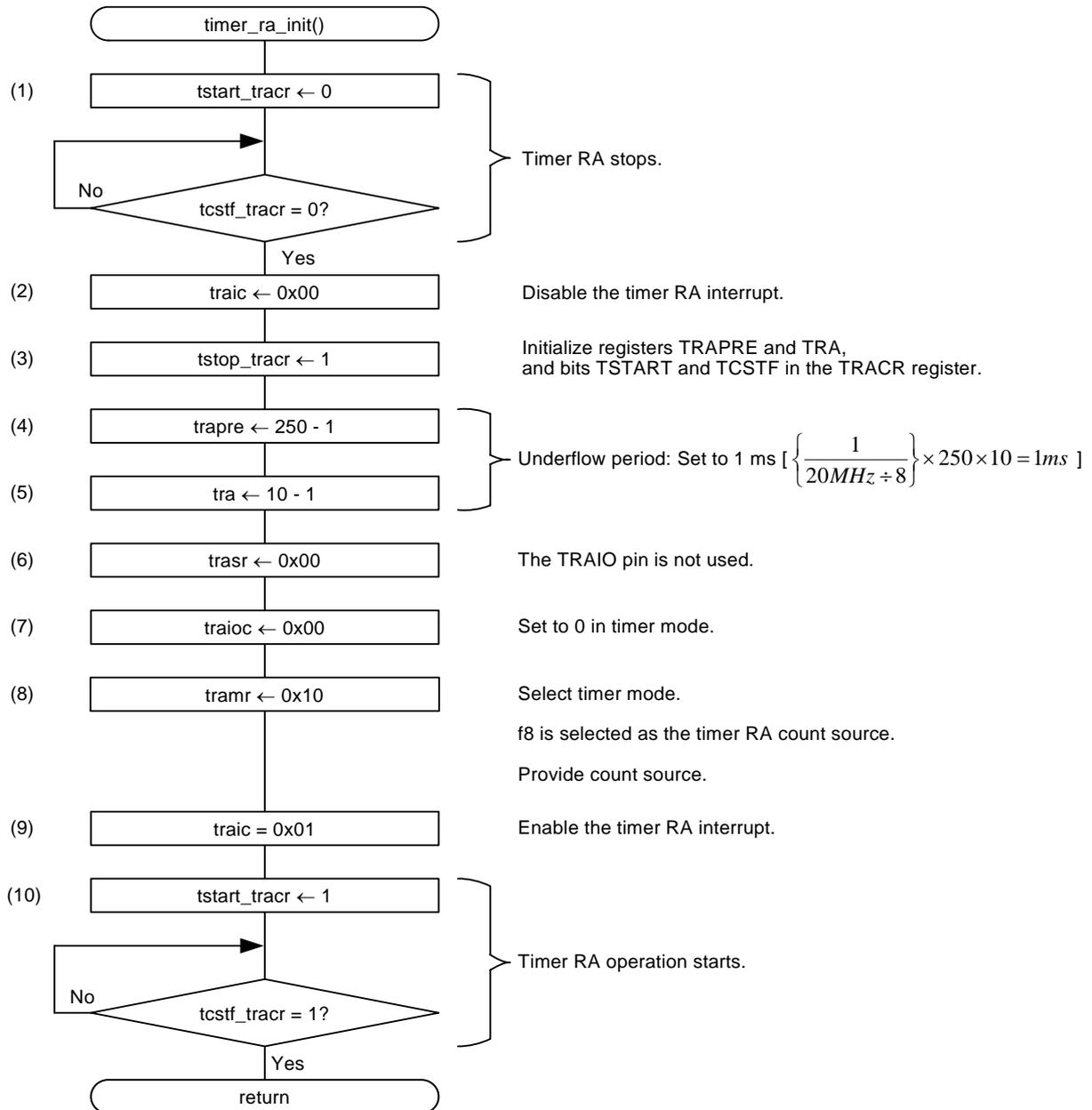
Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—	—	x	—	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write disabled	R/W

4.3 Timer RA Associated SFR Initial Setting

• Flowchart



• Register Settings

(1) Stop the timer RA count.

Timer RA Control Register (TRACR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	x	x	—		x	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RA count start bit	0: Count stops	R/W

(2) Disable the timer RA interrupt.

Interrupt Control Register (TRAIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(3) Initialize registers TRAPRE and TRA, and bits TSTART and TCSTF in the TRACR register.

Timer RA Control Register (TRACR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	x	x	—	1	x	

Bit	Symbol	Bit Name	Function	R/W
b2	TSTOP	Timer RA count forcible stop bit	1: The count is forcibly stopped. When read, the content is 0.	R/W

(4) Set the timer RA prescaler register to F9h.

Timer RA Prescaler Register (TRAPRE)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	1	1	1	1	1	0	0	1

Bit	Function	Setting Range	R/W
b7 to b0	Counts an internal count source.	00h to FFh	R/W

(5) Set the timer RA register to 09h.

Timer RA Register (TRA)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	0	0	0	0	1	0	0	1

Bit	Function	Setting Range	R/W
b7 to b0	Counts the TRAPRE register underflows.	00h to FFh	R/W

(6) Set the timer RA pin select register.

Timer RA Pin Select Register (TRASR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—	—	—	—	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRAIOSSEL0	TRAIO pin select bit	b1 b0 0 0: TRAI0 pin not used	R/W
b1	TRAIOSSEL1			R/W

(7) Set the timer RA I/O control register.

Timer RA I/O Control Register (TRAI0C) in Timer Mode

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	x	x	0	0	x	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	0: Set to 0 in timer mode.	R/W
b1	TOPCR	TRAIO output control bit		R/W
b2	TOENA	TRAO output enable bit		R/W
b4	TIPF0	TRAIO input filter select bit	0: Set to 0 in timer mode.	R/W
b5	TIPF1			R/W

(8) Set the timer RA mode register.

Timer RA Mode Register (TRAMR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	0	0	0	1	—	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RA operating mode select bit	b2 b1 b0 0 0 0: Timer mode	R/W
b1	TMOD1			R/W
b2	TMOD2			R/W
b4	TCK0	Timer RA count source select bit	b6 b5 b4 0 0 1: f8	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	TCKCUT	Timer RA count source cutoff bit	0: Count source provided	R/W

(9) Enable the timer RA interrupt.

Interrupt Control Register (TRAIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—	—	0	0	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 1: Level 1	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(10) Start the timer RA count.

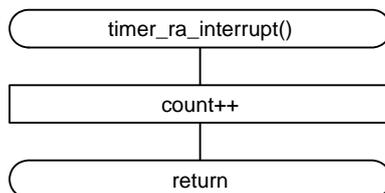
Timer RA Control Register (TRACR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	x	x	—		x	1

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RA count start bit	1: Count starts	R/W

4.4 Timer RA Interrupt

- Flowchart



5. Sample Program

A sample program can be downloaded from the Renesas Technology website.
To download, click “Application Notes” in the left-hand side menu of the R8C Family page.

6. Reference Documents

Hardware Manual

R8C/L3AA Group Hardware Manual Rev.0.30

The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Technology website.

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REVISION HISTORY	R8C/L3AA Group Timer RA (Timer Mode)
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Rev.	Date	Description	
		Page	Summary
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