R8C/38C Group

Timer RD (Complementary PWM Mode)

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1. Abstract

This document describes a setting method and an application example for timer RD in complementary PWM mode in the R8C/38C Group.

2. Introduction

The application example described in this document applies to the following microcomputer (MCU) and parameter:

- MCU: R8C/38C Group
- XIN clock frequency: 20 MHz

This application note can be used with other R8C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Application Example

3.1 Program Outline

Normal-phase and counter-phase PWM waveforms (one phase, triangular wave modulation, and dead time) with with 350 µs periods are output. Four kinds of PWM waveforms shown in Figures 3.2 to 3.5 are switched at the timings shown in Figures 3.6 to 3.10, and are repeated sequentially:
PWM waveform 1 → PWM waveform 2 → low fixed → PWM waveform 2 → high fixed → PWM waveform 1
The 350 µs PWM periods are calculated using the TRD0 setting value.
350 µs = 1/20 MHz × (TRDGRA0 + 2 – TRD0) × 2 = 50 ns × 3500 × 2

One period of normal-phase and counter-phase signals from the PWM waveform 1 output are output.
Normal-phase output: Inactive level (50 µs) → Active level (250 µs) → Inactive level (50 µs)
Counter-phase output: Active level (25 µs) → Dead time (25 µs) → Inactive level (250 µs) → Dead time (25 µs) → Active level (25 µs)
Output signals are shown below:

TRDIOB0 pin: PWM waveform 1 normal-phase output
Inactive level "H" 100 µs = 1/20 MHz × (TRDGRB0 + 1) × 2 = 50 ns × 1000 × 2
Active level "L" 250 µs = 1/20 MHz × (TRDGRA0 – TRDGRB0 – TRD0 + 1) × 2
= 50 ns × 2500 × 2
TRDIOD0 pin: PWM waveform 1 counter-phase output
Inactive level "H" 250 µs = 1/20 MHz × (TRDGRA0 – TRDGRB0 – TRD0 + 1) × 2
= 50 ns × 2500 × 2
Active level "L" 50 µs = 1/20 MHz × (TRDGRB0 + 1 – TRD0) × 2
= 50 ns × 500 × 2
Dead time "H" 25 µs = 1/20 MHz × TRD0 = 50 ns × 500

One period of normal-phase and counter-phase signals from the PWM waveform 2 output are output.
Normal-phase output: Inactive level (125 µs) → Active level (100 µs) → Inactive level (125 µs)
Counter-phase output: Active level (100 µs) → Dead time (25 µs) → Inactive level (100 µs) → Dead time (25 µs) → Active level (100 µs)
Output signals are shown below:

TRDIOB0 pin: PWM waveform 2 normal-phase output
Inactive level "H" 250 µs = 1/20 MHz × (TRDGRB0 + 1) × 2 = 50 ns × 2500 × 2
Active level "L" 100 µs = 1/20 MHz × (TRDGRA0 – TRDGRB0 – TRD0 + 1) × 2
= 50 ns × 1000 × 2
TRDIOD0 pin: PWM waveform 2 counter-phase output
Inactive level "H" 100 µs = 1/20 MHz × (TRDGRA0 – TRDGRB0 – TRD0 + 1) × 2
= 50 ns × 1000 × 2
Active level "L" 200 µs = 1/20 MHz × (TRDGRB0 + 1 – TRD0) × 2
= 50 ns × 2000 × 2
Dead time "H" 25 µs = 1/20 MHz × TRD0 = 50 ns × 500
One period of normal-phase and counter-phase signals from the low fixed output are output.
TRDIOB0 pin normal-phase output: Low output continuously
TRDIOD0 pin counter-phase output: High output continuously

One period of normal-phase and counter-phase signals from the high fixed output are output.
TRDIOB0 pin normal-phase output: High output continuously
TRDIOD0 pin counter-phase output: Low output continuously

Settings

- Use f1 (XIN clock: 20 MHz) as the count source.
- The TRD0 register is decremented at the compare match with the TRDGRA0 register when incrementing.
- Enable the compare match interrupt of registers TRD0 and TRDGRA0.
- The TRD1 register is decremented at the compare match of registers TRD0 and TRDGRA0 when incrementing.
- Transfer data from the buffer register to the general register when the TRD1 register underflows.
- Registers TRD0 and TRD1 are incremented when the TRD1 register becomes FFFFh from 0000h when decrementing.
- Select the TRDGRB0 and TRDGRD0 pin output levels as “L” active and the initial output level as inactive level “H”.
- Output an active level signal “L” from the TRDIOB0 output pin at the compare match of registers TRD1 and TRDGRB0.
- Output an active level signal “L” from the TRDIOD0 output pin at the same time the count starts.
- Invert the output level of the TRDIOD0 output pin at the compare match of registers TRD0 and TRDGRB0.
- Invert the output level of the TRDIOC0 output pin every 1/2 period of PWM.
- Use buffer operation (BFD0).
- Do not use the pulse output forced cutoff input function.
- Do not use A/D triggers.

Figure 3.1 shows a Block Diagram. Table 3.1 lists the pins used and their functions. Figures 3.2 to 3.5 show PWM waveforms, and figures 3.6 to 3.10 show waveform switching timings.

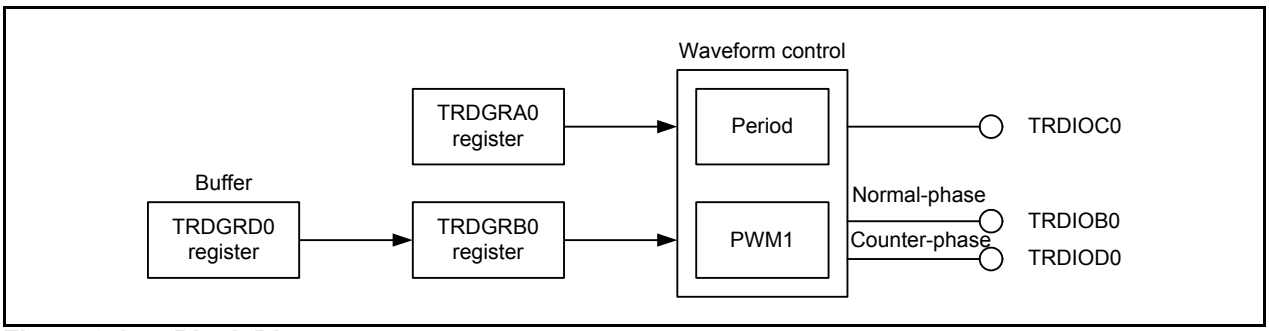


Figure 3.1 Block Diagram

Table 3.1 Pins Used and Their Functions

Pin Name	I/O	Function
P2_2/TRDIOB0	Output	PWM output 1 normal-phase output
P2_1/TRDIOC0	Output	Output inverted every 1/2 period of PWM
P2_3/TRDIOD0	Output	PWM output 1 counter-phase output

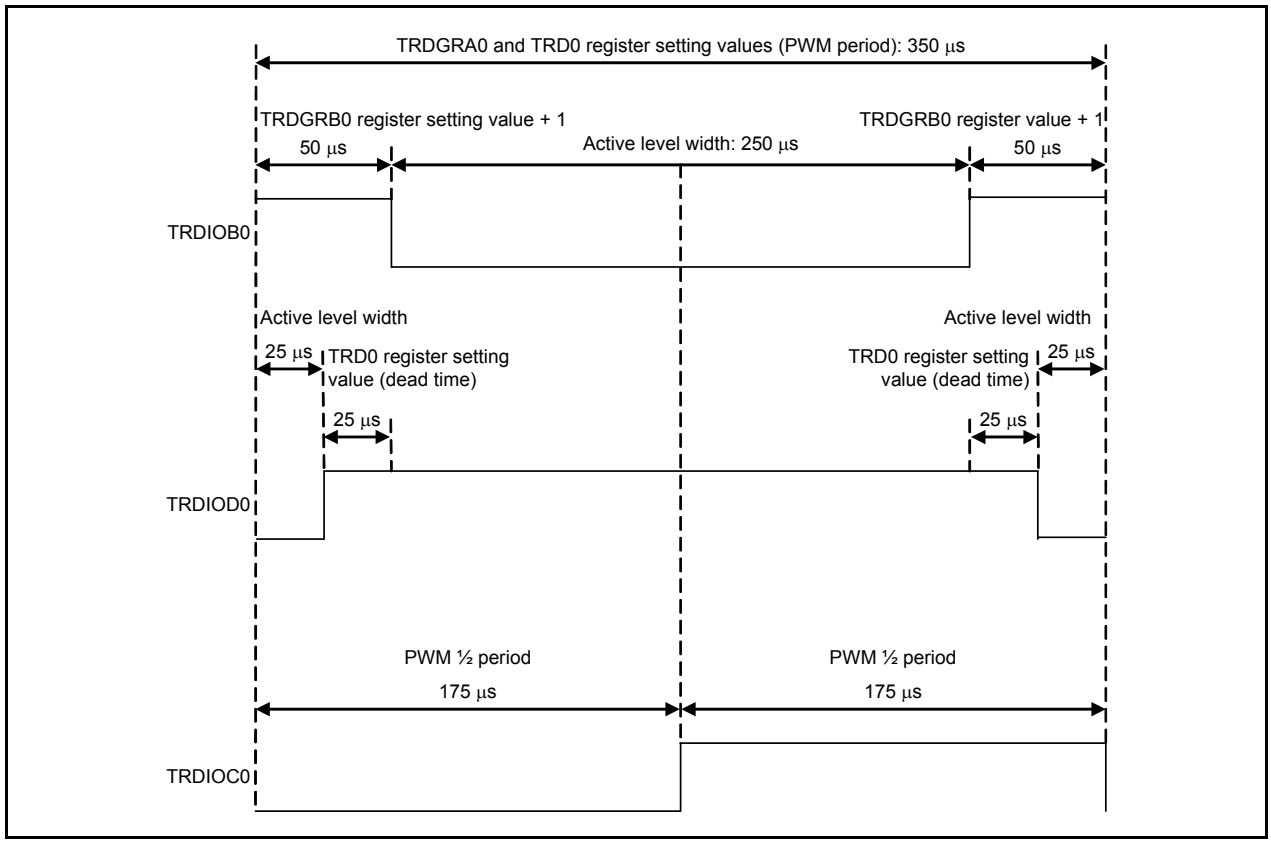


Figure 3.2 PWM Waveform 1

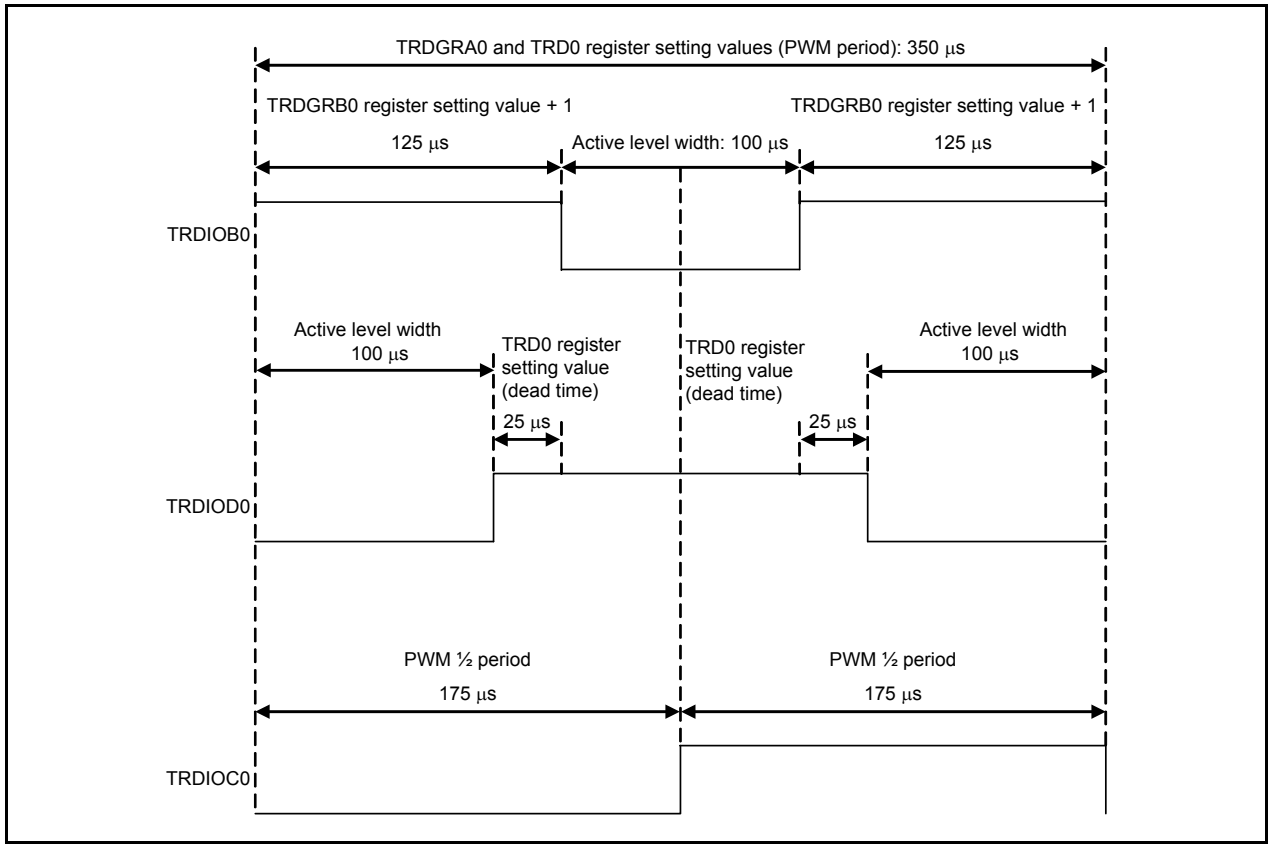


Figure 3.3 PWM Waveform 2

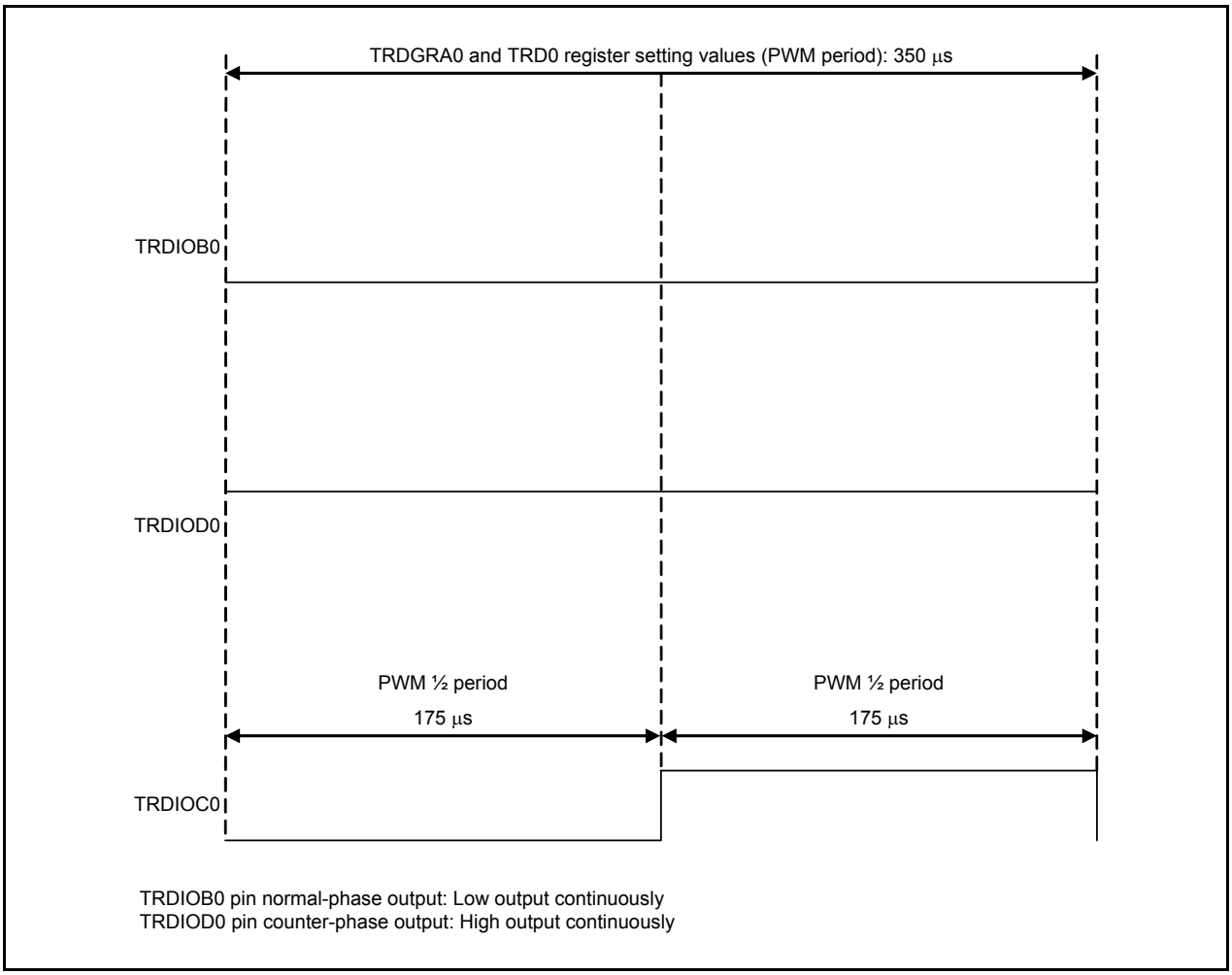


Figure 3.4 Low Fixed

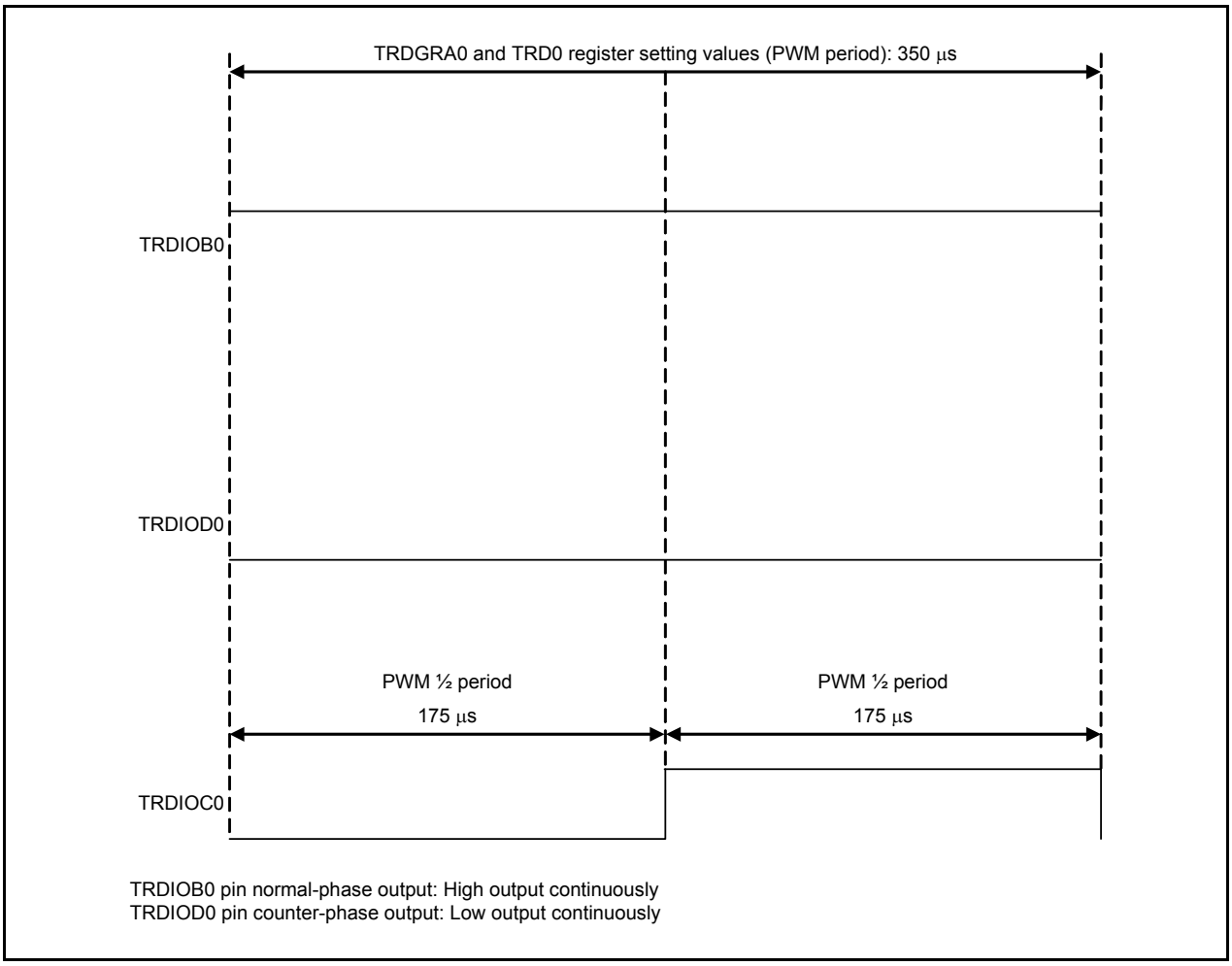
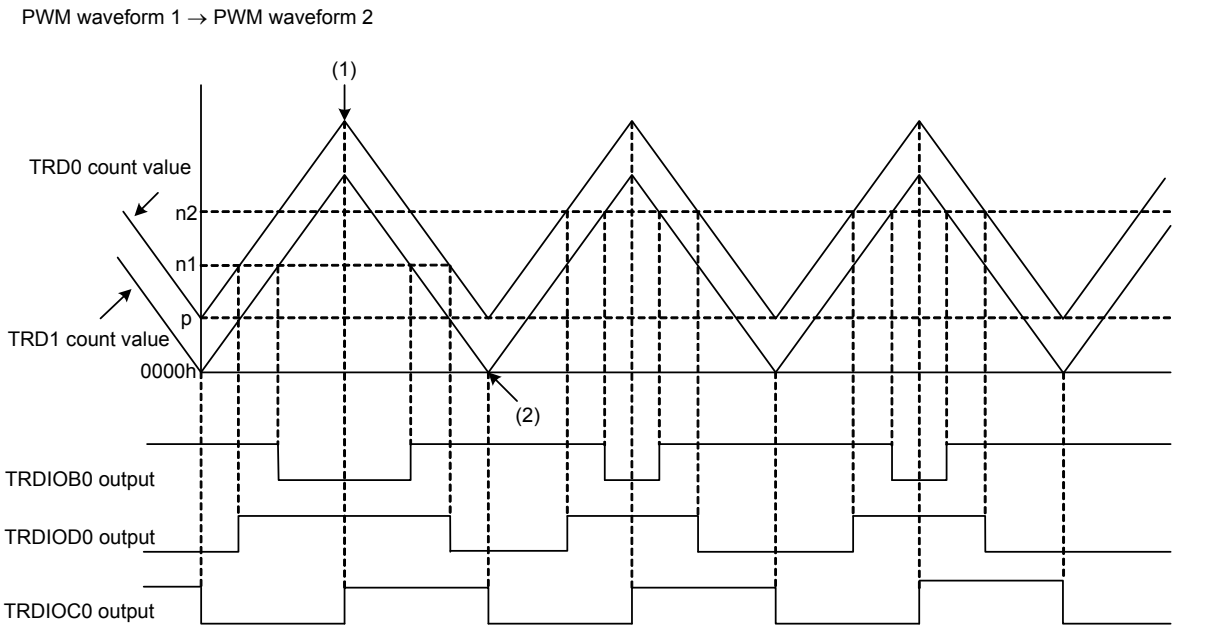


Figure 3.5 High Fixed

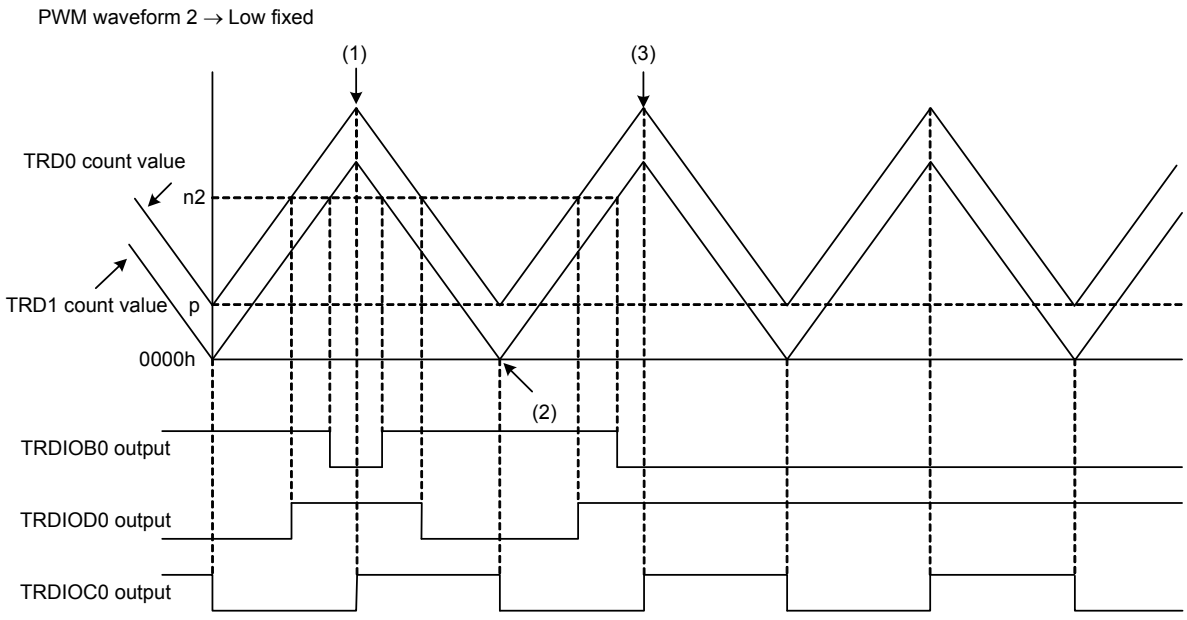


p: TRD0 register setting value (500)

n1: TRDGRD0 register setting value (999) at PWM waveform 1 output
n2: TRDGRD0 register setting value (2499) at PWM waveform 2 output

(1) Set n2 to the TRDGRD0 register at the 10th match of registers TRD0 and TRDGRA0.
(2) Data at (2) is transferred from the TRDGRD0 register to the TRDGRB0 register at the underflow of the TRD1 register.

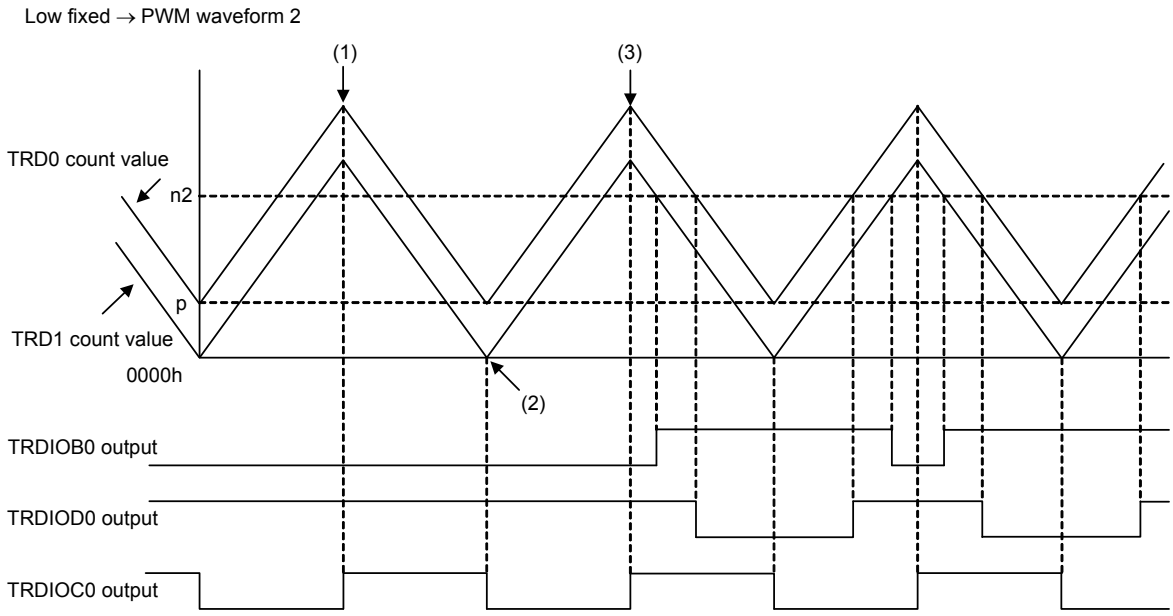
Figure 3.6 Switch Timing from PWM Waveform 1 to PWM Waveform 2



p: TRD0 register setting value (500)
n2: TRDGRD0 register setting value (2499) at PWM waveform 2 output

(1) Set 0000h to the TRDGRD0 register at the 10th match of registers TRD0 and TRDGRA0.
(2) Because the TRDGRD0 register value is 0000h at the underflow of the TRD1 register, data at (2) is not transferred from the TRDGRD0 register to the TRDGRB0 register.
(3) Because the TRDGRD0 register value is 0000h, data at (3) is transferred from TRDGRD0 reigster to TRDGRB0 register at the match of registers TRD0 and TRDGRA0.

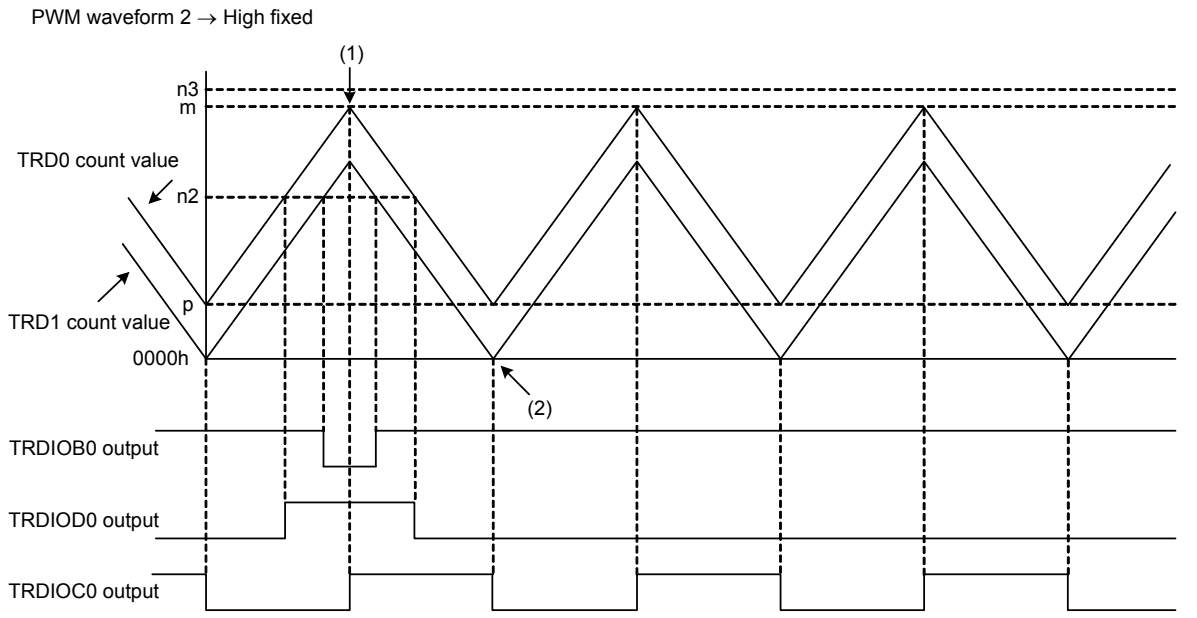
Figure 3.7 Switch Timing from PWM Waveform 2 to Low Fixed



p: TRD0 register setting value (500)
n2: TRDGRD0 register setting value (2499) at PWM waveform 2 output

(1) Set n2 to TRDGRD0 register at the 10th match of registers TRD0 and TRDGRA0.
(2) Because of the first underflow of the TRD1 register after changing the TRDGRD0 register value from 0000h to n2, data at (2) is not transferred from the TRDGRD0 register to the TRDGRB0 register.
(3) Because of the first match of registers TRD0 and TRDGRA0 after changing the TRDGRD0 register value from 0000h to n2, data at (3) is transferred from the TRDGRD0 register to the TRDGRB0 register.

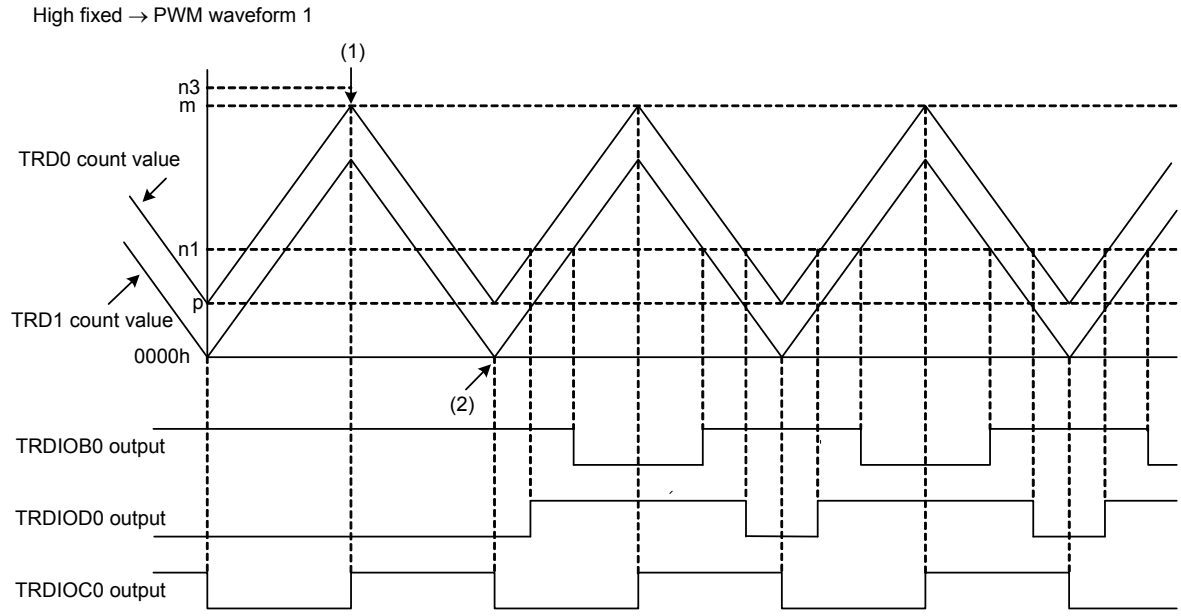
Figure 3.8 Switch Timing from Low Fixed to PWM Waveform 2



m: TRDGRA0 register setting value (3998)
p: TRD0 register setting value (500)
n2: TRDGRD0 register setting value (2499) at PWM waveform 2 output
n3: TRDGRD0 register setting value (4500) at high fixed waveform output

(1) Set n3 to the TRDGRD0 register at the 10th match of registers TRD0 and TRDGRA0.
(2) The data is transferred from the TRDGRD0 register to TRDGRB0 register at the underflow of the TRD1 register because n3 ≥ m.

Figure 3.9 Switch Timing from PWM Waveform 2 to High Fixed



m: TRDGRA0 register setting value (3998)
p: TRD0 register setting value (500)
n1: TRDGRD0 register setting value (999) at PWM waveform 1 output.
n3: TRDGRD0 register setting value (4500) at high fixed waveform output

(1) Set n1 to the TRDGRD0 register at the 10th match of registers TRD0 and TRDGRA0.
(2) Because of the first underflow of the TRD1 register after changing the TRDGRD0 register value from n3 (n3 ≥ m) to n1, data at (2) is transferred from the TRDGRD0 register to the TRDGRB0 register.

Figure 3.10 Switch Timing from High Fixed to PWM Waveform 1

3.2 Memory

Table 3.2 Memory

Memory	Size	Remarks
ROM	303 bytes	In the r01an0084_src.c module
RAM	2 bytes	In the r01an0084_src.c module
Maximum user stack	10 bytes	
Maximum interrupt stack	4 bytes	

Memory size varies depending on the C compiler version and compile options.
The above applies to the following conditions:
C compiler: M16C Series, R8C Family C Compiler V.5.45 Release 01
Compile options: -c -finfo -dir “$(CONFIGDIR)” -R8C

4. Software

This section shows the initial setting procedures and values to set the example described in section **3. Application Example**. Refer to the latest **R8C/38C Group** hardware user's manual for details on individual registers.

The × in the register's Setting Value represents bits not used in this application, blank spaces represent bits that do not change, and the dash represents reserved bits or bits that have nothing assigned.

4.1 Function Tables

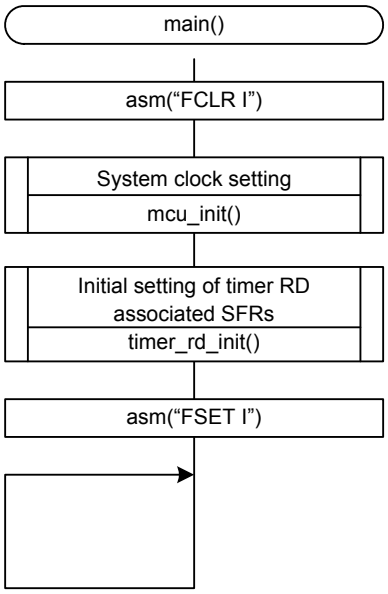
Declaration	void mcu_init(void)		
Outline	System clock setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Set the system clock (XIN clock).		

Declaration	void timer_rd_init(void)		
Outline	Initial setting of timer RD associated SFRs		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Initialize timer RD associated SFRs to use timer RD in complementary PWM mode.		

Declaration	void _timer_rd_ch0(void)		
Outline	Timer RD0 interrupt handling		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	unsigned char int_cnt		Interrupt counter
	unsigned char output_chg_mode		Output switch mode
Returned value	Type	Value	Meaning
	None	—	—
Function	Perform interrupt handling generated at the compare match of registers TRD0 and TRDGRA0. Every 10 times an interrupt is generated for each PWM waveform output, set the TRDGRD0 register to output the next PWM waveform.		

4.2 Main Function

• Flowchart



Disable interrupts.

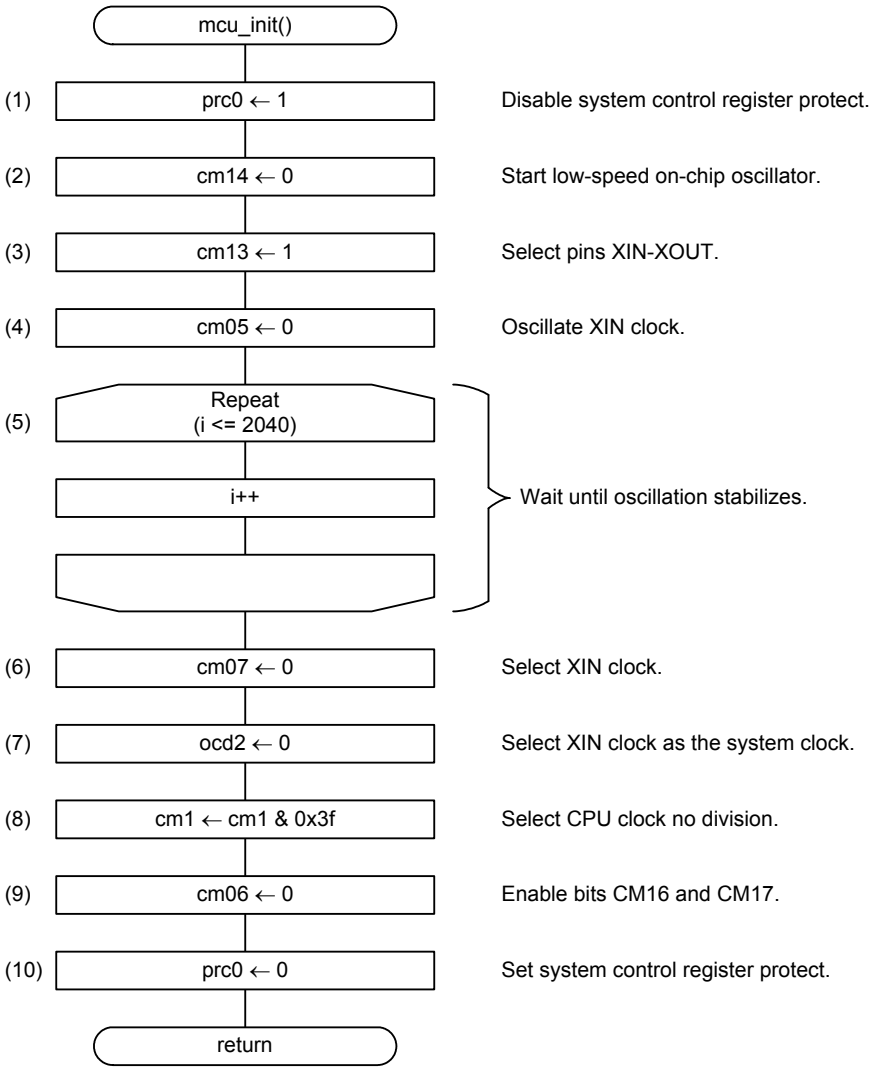
System clock setting (XIN clock setting)

Initial setting of timer RD associated SFRs (complementary PWM mode setting)

Enable interrupts.

4.3 System Clock Setting

• Flowchart



• Register settings

(1) Enable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 1: Write enabled	R/W

(2) Start the low-speed on-chip oscillator.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			—	0		x	x	x

Bit	Symbol	Bit Name	Function	R/W
b4	CM14	Low-speed on-chip oscillator stop bit	0: Low-speed on-chip oscillator on	R/W

(3) Set system clock control register 1.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			—		1	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b3	CM13	Port/XIN-XOUT switch bit	1: XIN-XOUT pin	R/W

(4) Set system clock control register 0.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			0	x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b5	CM05	XIN clock (XIN-XOUT) stop bit	0: XIN clock oscillates	R/W

(5) Wait until oscillation stabilizes.

(6) Select the XIN clock.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0			x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b7	CM07	XIN, XCIN clock select bit	0: XIN clock	R/W

(7) Select the XIN clock as the system clock.

Oscillation Stop Detection Register (OCD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	0	x	x

Bit	Symbol	Bit Name	Function	R/W
b2	OCD2	System clock select bit	0: XIN clock selected	R/W

(8) Set system clock control register 1.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	—			x	x	x

Bit	Symbol	Bit Name	Function	R/W
b6	CM16	CPU clock division select bit 1	b7 b6 0 0: No division mode	R/W
b7	CM17			R/W

(9) Set system clock control register 0.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		0		x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	CM06	CPU clock division select bit 0	0: Bits CM16 and CM17 in CM1 register enabled	R/W

(10) Disable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

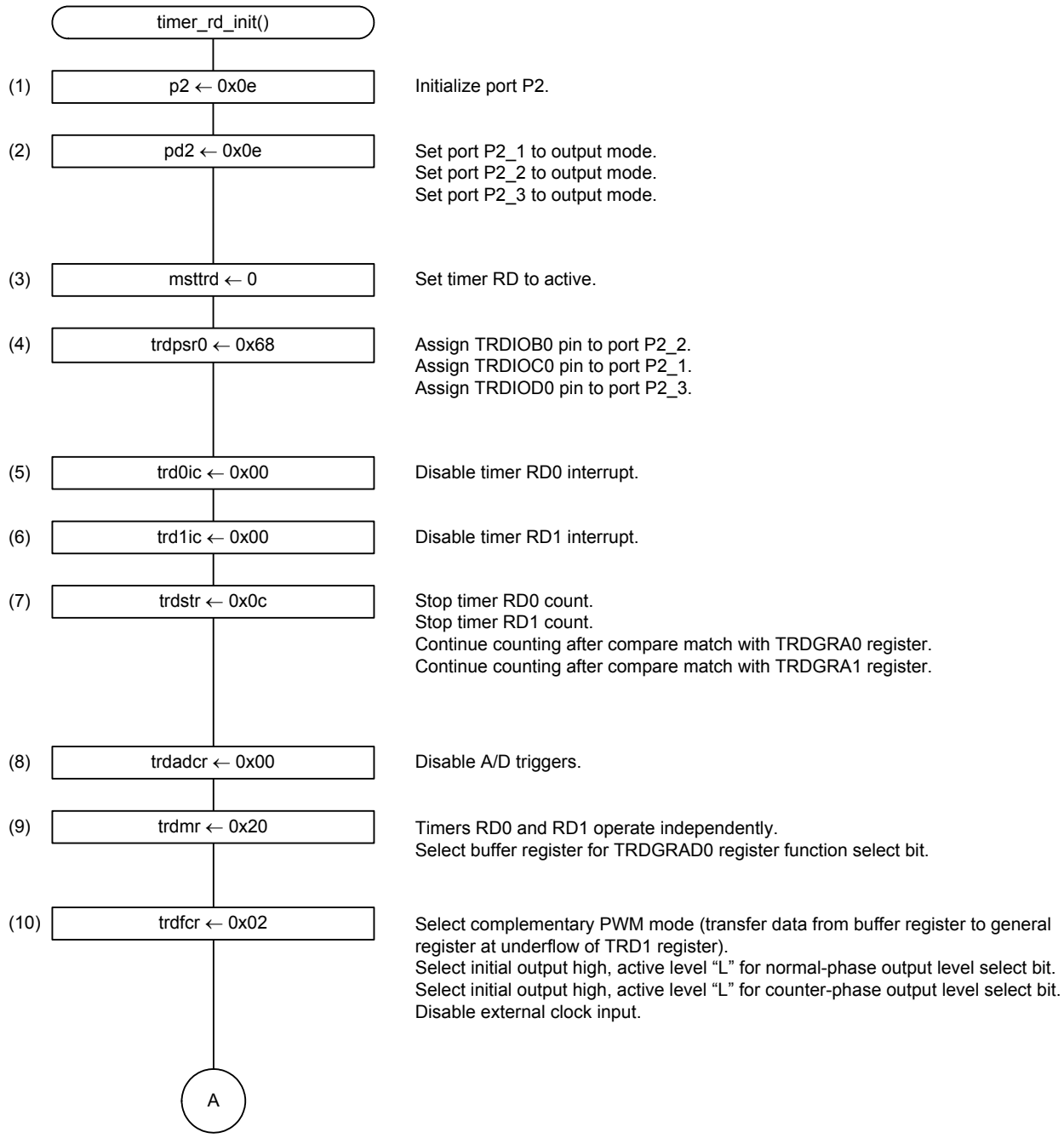
Protect Register (PRCR)

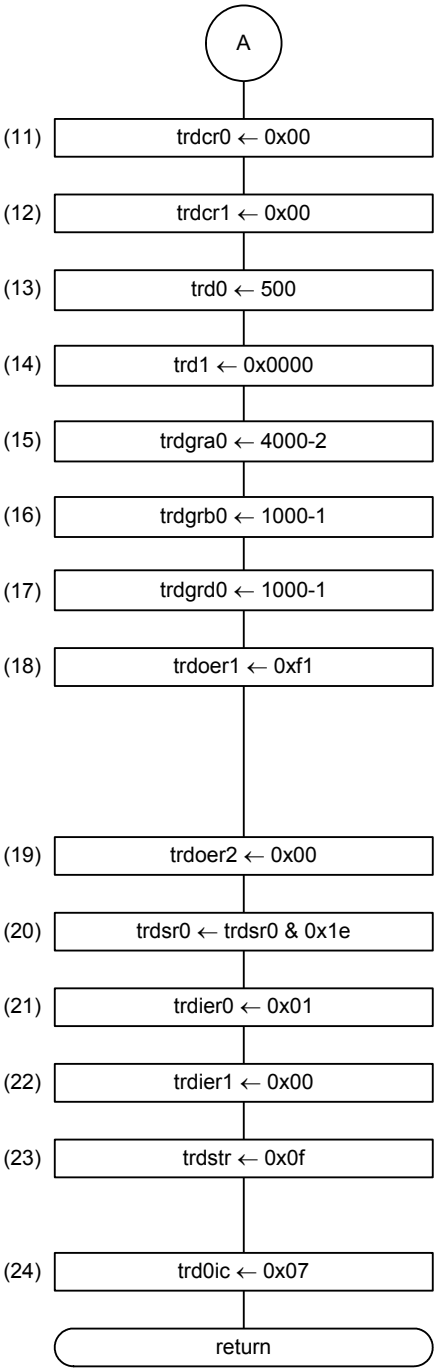
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write disabled	R/W

4.4 Initial Setting of Timer RD Associated SFRs

• Flowchart





Select f1 as the count source.

Select f1 as the cont source.

Set 25 μs for dead time.
50 ns × TRD0 = 50 ns × 500 = 25 μs

Initialize TRD1 register count value to 0000h.

Set 350 μs for PWM period.
[50 ns × (TRDGRA0 + 2 – TRD0)] × 2 = [50 ns × (3998 + 2 – 500)] × 2 = 350 μs

Set 50 μs for PWM output change point.
50 ns × (TRDGRB0 + 1) = 50 ns × (999 + 1) = 50 μs

Set TRDGRD0 register value.

Disable TRDIOA0 output.
Enable TRDIOB0 output.
Enable TRDIOC0 output.
Enable TRDIOD0 output.

Disable pulse output forced cutoff input.

Clear input capture/compare match flag A.

Set IMFA bit to enable IMIA interrupt.

Disable TRD1 interrupt.

Start timer RD0 count.
Start timer RD1 count.

Enable timer RD0 interrupt (level 7)

• Register settings

(1) Initialize port P2.

Port P2 Register (P2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	1	1	1	x

Bit	Symbol	Bit Name	Function	R/W
b1	P2_1	Port P2_1 bit	1: “H” level	R/W
b2	P2_2	Port P2_2 bit		R/W
b3	P2_3	Port P2_3 bit		R/W

(2) Set ports P2_1 to P2_3 to output mode.

Port P2 Direction Register (PD2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	1	1	1	x

Bit	Symbol	Bit Name	Function	R/W
b1	PD2_1	Port P2_1 direction bit	1: Output mode (functions as an output port)	R/W
b2	PD2_2	Port P2_2 direction bit		R/W
b3	PD2_3	Port P2_3 direction bit		R/W

(3) Set timer RD to active.

Module Standby Control Register (MSTCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	x	x	0	x	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b4	MSTTRD	Timer RD standby bit	0: Active	R/W

(4) Set timer RD pin select register 0.

Timer RD Pin Select Register 0 (TRDPSR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	1	1	0	1	0	—	x

Bit	Symbol	Bit Name	Function	R/W
b2	TRDIOB0SEL0	TRDIOB0 pin select bit	b3 b2 1 0: P2_2 assigned	R/W
b3	TRDIOB0SEL1			R/W
b4	TRDIOC0SEL0	TRDIOC0 pin select bit	b5 b4 1 0: P2_1 assigned	R/W
b5	TRDIOC0SEL1			R/W
b6	TRDIOD0SEL0	TRDIOD0 pin select bit	1: P2_3 assigned	R/W

(5) Disable the timer RD0 interrupt.

Interrupt Control Register (TRD0IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R

(6) Disable the timer RD1 interrupt.

Interrupt Control Register (TRD1IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R

(7) Stop timer RD0 and timer RD1 counts, and set timer RD0 and RD1 count operations.

Timer RD Start Register (TRDSTR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	1	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART0	TRD0 count start flag	0: Count stops	R/W
b1	TSTART1	TRD1 count start flag	0: Count stops	R/W
b2	CSEL0	TRD0 count operation select bit	1: Count continues after the compare match with the TRDGRA0 register	R/W
b3	CSEL1	TRD1 count operation select bit	1: Count continues after the compare match with the TRDGRA1 register	R/W

(8) Disable A/D triggers.

Timer RD Trigger Control Register (TRDADCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	x	x	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADTRGA0E	A/D trigger A0 enable bit	0: A/D trigger disabled	R/W
b1	ADTRGB0E	A/D trigger B0 enable bit	0: A/D trigger disabled	R/W

(9) Set the timer RD mode register.

Timer RD Mode Register (TRDMR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	1	0	—	—	—	0

Bit	Symbol	Bit Name	Function	R/W
b0	SYNC	Timer RD synchronous bit	0: Registers TRD0 and TRD1 operate independently	R/W
b4	BFC0	TRDGRC0 register function select bit	Set this bit to 0 (general register) in complementary PWM mode.	R/W
b5	BFD0	TRDGRD0 register function select bit	1: Buffer register of TRDGRB0 register	R/W

(10) Set the timer RD function control register.

Timer RD Function Control Register (TRDFCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	0	x	x	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	CMD0	Combination mode select bit	b1 b0 1 0: Complementary PWM mode (transfer from the buffer register to the general register at the underflow in the TRD1 register)	R/W
b1	CMD1			R/W
b2	OLS0	Normal-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)	0: Initial output “H”, Active level “L”	R/W
b3	OLS1	Counter-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)		R/W
b6	STCLK	External clock input select bit	0: External clock input disabled	R/W

(11) Set timer RD control register 0.

Timer RD Control Register 0 (TRDCR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	x	x	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bit	b2 b1 b0 0 0 0: f1	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b5	CCLR0	TRD0 counter clear select bit	Set to 000b (disable clearing (free-running operation)) in complementary PWM mode.	R/W
b6	CCLR1			R/W
b7	CCLR2			R/W

(12) Set timer RD control register 1.

Timer RD Control Register 1 (TRDCR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	x	x	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bit	b2 b1 b0 0 0 0: f1	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b5	CCLR0	TRD0 counter clear select bit	Set to 000b (disable clearing (free-running operation)) in complementary PWM mode.	R/W
b6	CCLR1			R/W
b7	CCLR2			R/W

(13) Set timer RD counter 0 to 500 (1F4h).

Timer RD Counter 0 (TRD0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	1	1	1	0	1	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0	0	0	0	0	0	0	1

Bit	Function	Setting Range	R/W
b15-b0	Set the dead time. Count a count source. Count operation is incremented or decremented. When an overflow occurs, the OVF bit in the TRDSR0 register is set to 1.	0000h to FFFFh	R/W

(14) Initialize timer RD counter 1 to 0000h.

Timer RD Counter 1 (TRD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15-b0	Set 0000h. Count a count source. Count operation is incremented or decremented. When an underflow occurs, the UDF bit in the TRDSR1 register is set to 1.	0000h to FFFFh	R/W

(15) Set compare value 4000 - 2 (F9Eh) of timer RD counter 0 to timer RD general register A0.

Timer RD General Register A0 (TRDGRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	0	0	1	1	1	1	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0	0	0	0	1	1	1	1

Bit	Function	R/W
b15-b0	General register. Set the PWM period at initialization. Setting range: Setting value or above in TRD0 register FFFFh - TRD0 register setting value or below	R/W

(16) Set compare value 1000 - 1 (3E7h) of timer RD counter 0 or timer RD counter 1 to timer RD general register B0.

Timer RD General Register B0 (TRDGRB0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	1	1	0	0	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0	0	0	0	0	0	1	1

Bit	Function	R/W
b15-b0	General register. Set the changing point of PWM1 output at initialization. Setting range: Setting value or above in TRD0 register TRDGRA0 register - TRD0 register setting value or below	R/W

(17) Set the same value 1000 - 1 (3E7h) of timer RD general register B0 to timer RD general register D0.

Timer RD General Register D0 (TRDGRD0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	1	1	0	0	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0	0	0	0	0	0	1	1

Bit	Function	R/W
b15-b0	Buffer register. Set the changing point of next PWM1 output Setting range: Setting value or above in TRD0 register TRDGRA0 register - TRD0 register setting value or below Set this register to the same value as the TRDGRB0 register for initialization.	R/W

(18) Set timer RD output master enable register 1.

Timer RD Output Master Enable Register 1 (TRDOER1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	0	0	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	EA0	TRDIOA0 output disable bit	Set this bit to 1 (the TRDIOA0 pin is used as a programmable I/O port) in reset synchronous PWM mode.	R/W
b1	EB0	TRDIOB0 output disable bit	0: Enable output	R/W
b2	EC0	TRDIOC0 output disable bit	0: Enable output	R/W
b3	ED0	TRDIOD0 output disable bit	0: Enable output	R/W

(19) Set to pulse output forced cutoff input disabled.

Timer RD Output Master Enable Register 2 (TRDOER2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	—	—	—	—	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b7	PTO	$\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled bit	0: Pulse output forced cutoff input disabled	R/W

(20) Initialize input capture/compare match flag A.

Timer RD Status Register 0 (TRDSR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	x	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input capture/compare match flag A	[Source for setting this bit to 0] Write 0 after read.	R/W

(21) Set the IMFA bit to enable the IMIA interrupt.

Timer RD Interrupt Enable Register 0 (TRDIER0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	x	x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input capture/compare match interrupt enable bit A	1: Enable interrupt (IMIA) by the IMFA bit	R/W

(22) Disable the timer RD1 interrupt.

Timer RD Interrupt Enable Register 1 (TRDIER1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input capture/compare match interrupt enable bit A	0: Disable interrupt (IMIA) by the IMFA bit	R/W
b1	IMIEB	Input capture/compare match interrupt enable bit B	0: Disable interrupt (IMIB) by the IMFB bit	R/W
b2	IMIEC	Input capture/compare match interrupt enable bit C	0: Disable interrupt (IMIC) by the IMFC bit	R/W
b3	IMIED	Input capture/compare match interrupt enable bit D	0: Disable interrupt (IMID) by the IMFD bit	R/W
b4	OVIE	Overflow/underflow interrupt enable bit	0: Disable interrupt (OVI) by the OVF bit	R/W

(23) Start timer RD0 and timer RD1 counts.

Timer RD Start Register (TRDSTR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—			1	1

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART0	TRD0 count start flag	1: Count starts	R/W
b1	TSTART1	TRD1 count start flag	1: Count starts	R/W

(24) Enable the timer RD0 interrupt (level 7).

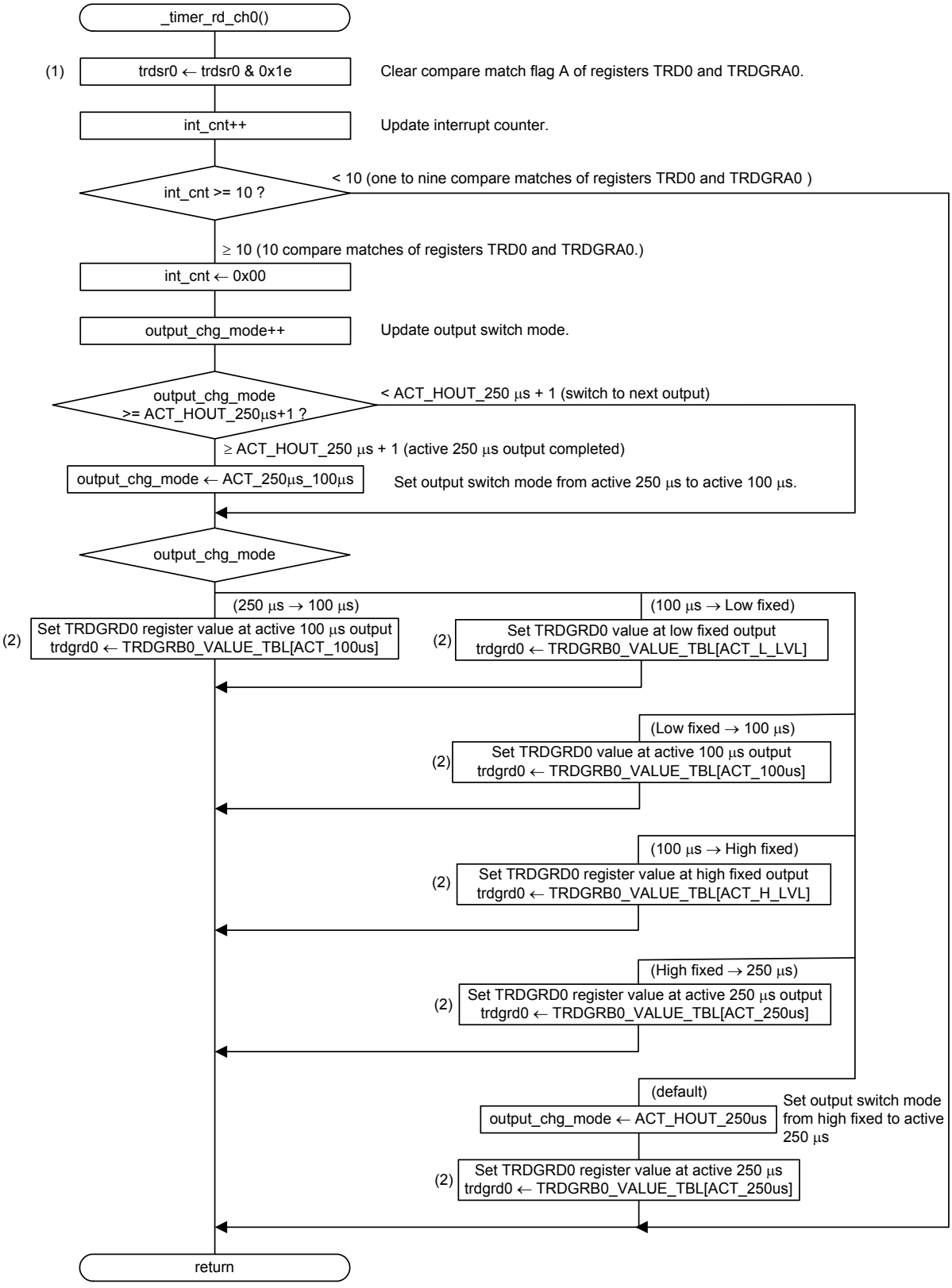
Interrupt Control Register (TRD0IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 1 1 1: Level 1	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R

4.5 Timer RD0 Interrupt Handling

• Flowchart



• Register settings

(1) Initialize input capture/compare match flag A.

Timer RD Status Register 0 (TRDSR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	x	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input capture/compare match flag A	[Source for setting this bit to 0] Write 0 after read.	R/W

(2) Store the value of the PWM output changing point to timer RD general register D0.

Timer RD General Register 0 (TRDGRD0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Bit	Function	R/W
b15 to b0	Buffer register. Set the changing point of next PWM1 output Setting range: Setting value or above in TRD0 register TRDGRA0 register - TRD0 register setting value or below Set this register to the same value as the TRDGRB0 register for initialization.	R/W

5. Sample Program

A sample program can be downloaded from the Renesas Electronics website.

6. Reference Documents

R8C/38C Group User's Manual: Hardware Rev.1.00
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

Website and Support

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Revision History	R8C/38C Group Timer RD (Complementary PWM Mode)

Rev.	Date	Description	
		Page	Summary
1.00	Oct. 25, 2010	—	First edition issued
1.01	June 1, 2012	7 to 11	Figures 3.6 to 3.10 (1) registers TRD0 and TRDGRD0 revised as registers TRD0 and TRDGRA0.

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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