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R8C/35A Group

Clock Synchronous Serial Program Downloader

1. Abstract

This documents describes the clock synchronous serial program downloader for the R8C/35A Group.

2. Introduction

The application example described in this document applies to the following MCU and parameter:

- MCU: R8C/35A Group
- XIN clock frequency: 20 MHz

The sample program may include operations of unused bit functions for the convenience of the SFR bit layout. Set the values according to the operating conditions of the user system.

3. Program Downloader Overview

3.1 Downloader Specifications

- The system program (including program downloader process) is allocated to block 0.
- The program downloader erases and writes mainly to user programs other than the user program in block 0. The program downloader ignores rewrite operations to block 0.
- EW0 mode is used by the program downloader for rewriting the CPU.
- In a reset start, the program downloader checks the state of port P1_6 and selects either to use the program downloader or the user program. The program downloader operates when port P1_6 is high, and the user program operates when port P1_6 is low.
- The virtual fixed vector table is allocated to block 1 to use the fixed vector table interrupt in the user program.
- UART0 clock synchronous serial I/O is used to communicate with a programmer.
- An external clock (input from the CLK0 pin) is selected for the transfer clock.
- CMOS output is selected for the TXD0 pin.
- Refer to 4. Downloader Communication Protocol for the communication protocol.

Figure 3.1 shows an example of a Connection, Figure 3.2 shows the Transfer Format, Figure 3.3 shows the Memory Map (32 Kbyte ROM MCU), and Figure 3.4 shows an example of the System Interrupt Operation (Overflow Interrupt).

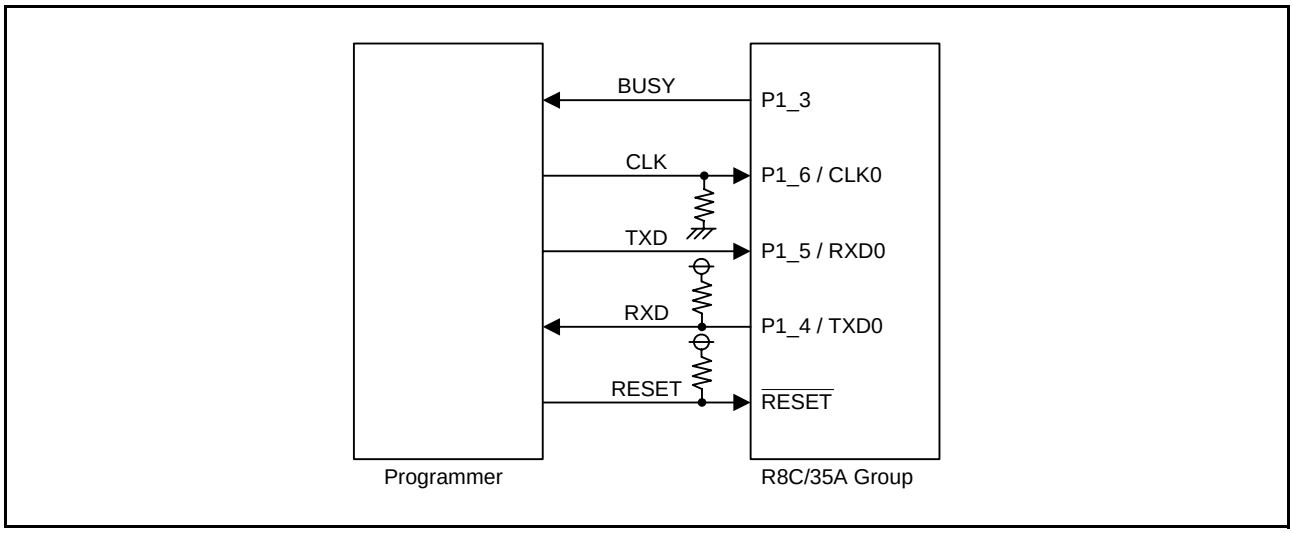


Figure 3.1 Connection

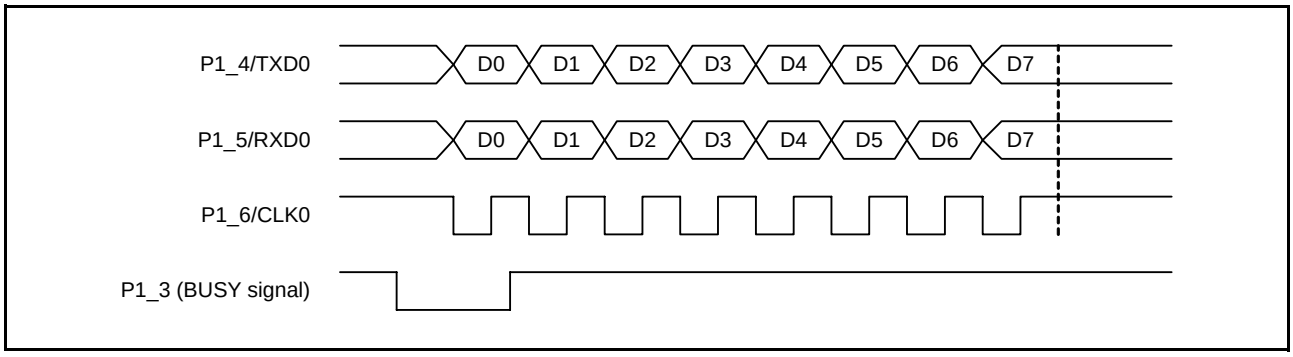
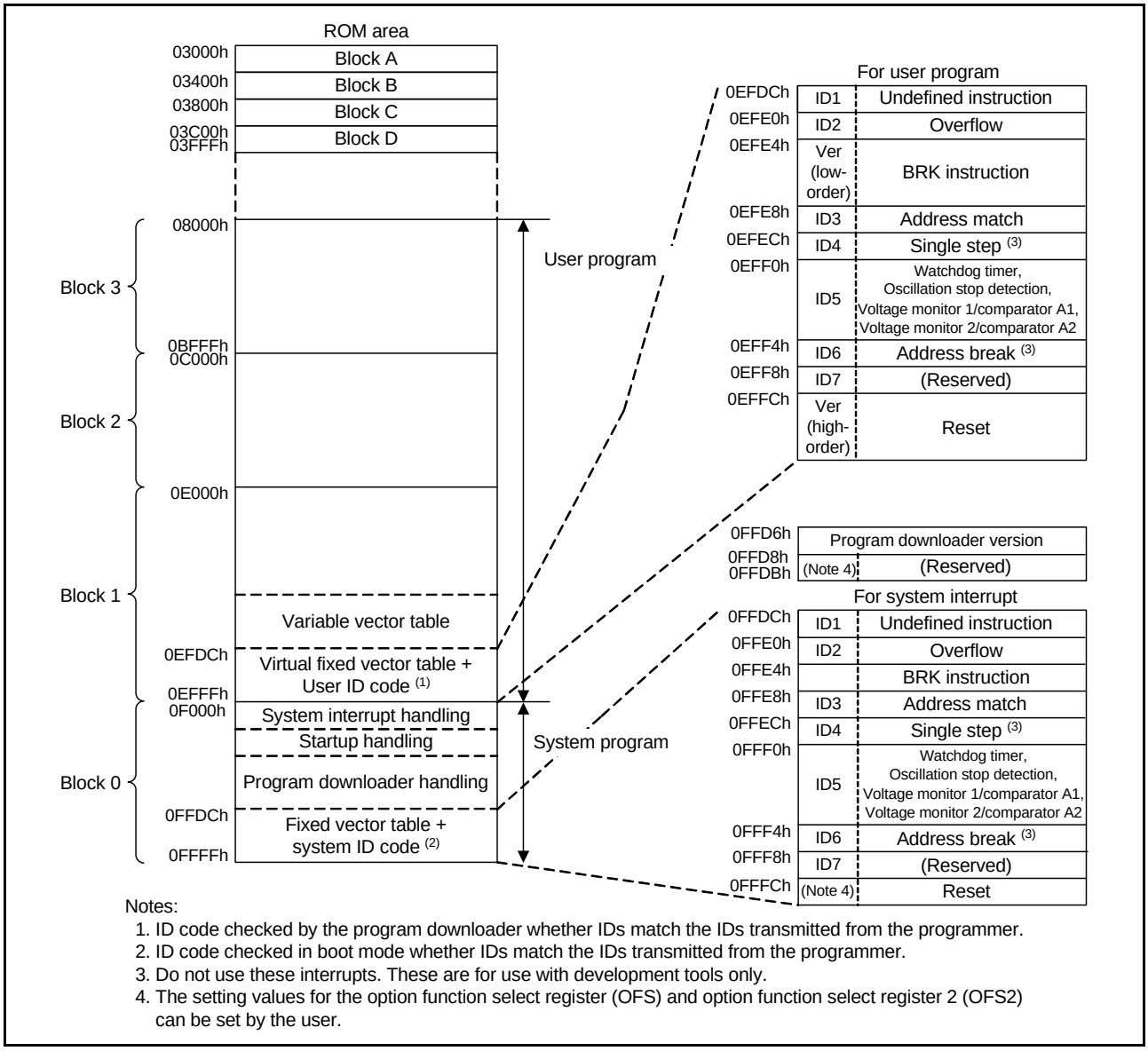


Figure 3.2 Transfer Format



Notes:
1. ID code checked by the program downloader whether IDs match the IDs transmitted from the programmer.
2. ID code checked in boot mode whether IDs match the IDs transmitted from the programmer.
3. Do not use these interrupts. These are for use with development tools only.
4. The setting values for the option function select register (OFS) and option function select register 2 (OFS2) can be set by the user.

Figure 3.3 Memory Map (32 Kbyte ROM MCU)

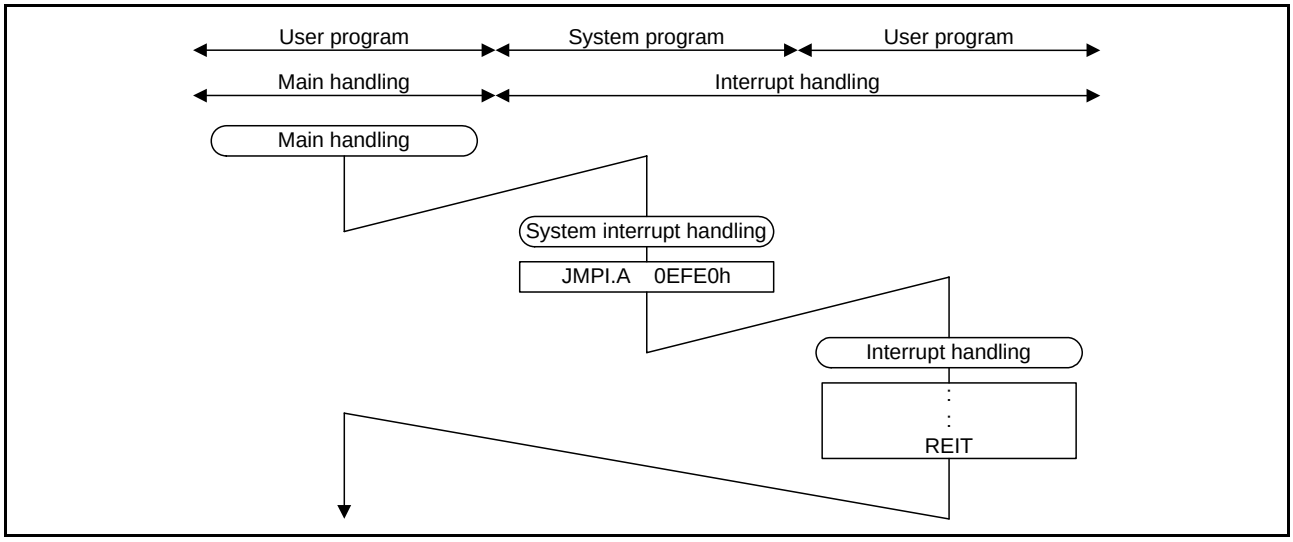
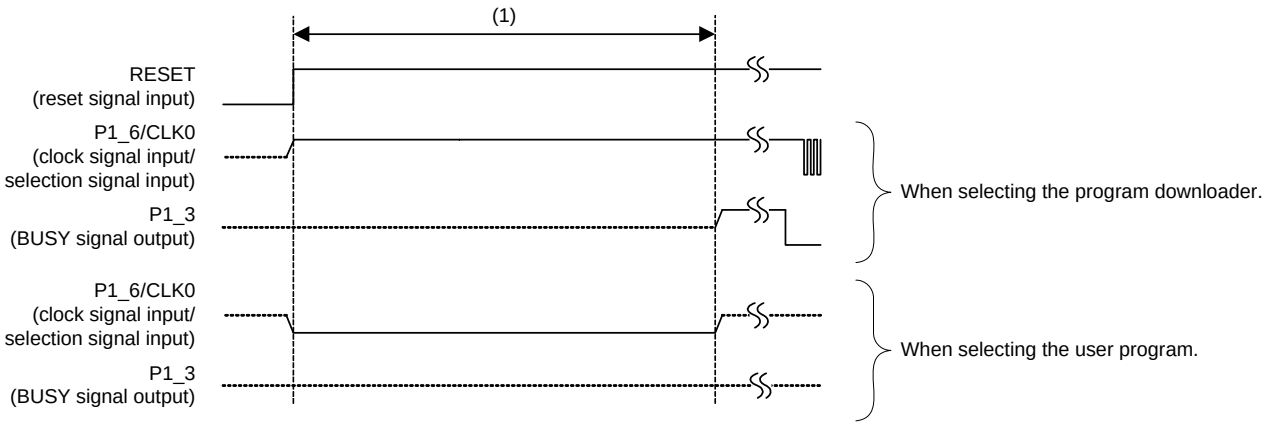


Figure 3.4 System Interrupt Operation (Overflow Interrupt)

3.2 Timing after Reset

The operating program after reset chooses either the program downloader or the user program. The MCU enters either program according to the P1_6/CLK0 pin level applied to the MCU during (1). Before reset is deasserted, a programmer must determine the input level of the P1_6/CLK0 pin, and hold that level during (1).



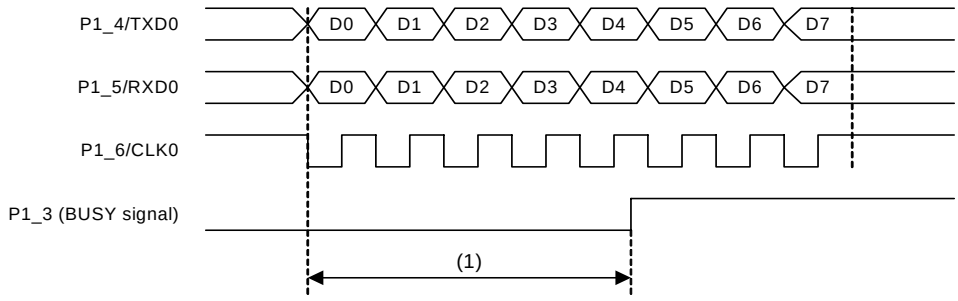
(1) While the program downloader or user program selection signal is held and the BUSY signal output starts:
Approximately 4.5 ms. (1)
The reset sequence is included in above time.

Note:
1. Time when the low-speed on-chip oscillator (60 kHz (min)) operates.

Figure 3.5 Signal Control Timing after Reset

3.3 BUSY Signal Output Timing from Clock Input

The BUSY signal output from the program downloader matches the transfer timing when communicating with the programmer and program downloader. Output the clock signal and start communication after the programmer confirms that the BUSY signal is low. Figure 3.6 shows the Timing until Timing between Transfer Clock Input and the BUSY Signal Becoming High.



(1) Maximum delay time between the external clock input and BUSY signal high output (theoretical value) (1)
- When the watchdog timer reset handling is disabled (WDT_USE is not defined): 2.20 µs
  Maximum transfer clock (theoretical value): 3.4 MHz
- When the watchdog timer reset handling is enabled (WDT_USE is defined): 2.85 µs
  Maximum transfer clock (theoretical value): 2.6 MHz

(For details on enabling/disabling the watchdog timer reset handling, refer to (3) Watchdog Timer Reset in section 3.4 Initial Settings.)

Note:
1. Time when the XIN clock (20 MHz) operates.

Figure 3.6 Timing between Transfer Clock Input and the BUSY Signal Becoming High

3.4 Initial Settings

(1) Option function select register (OFS)
The OFS register is assigned to the highest-order address 0FFFFh in the fixed vector table. Set the OFS register by a program of the program downloader.

(2) Option function select register 2 (OFS2)
The OFS2 register is assigned to 0FFDBh in the reserved area. Set the OFS2 register by a program of the program downloader.

(3) Watchdog timer
When using the watchdog timer, enable the WDT_USE definition in the fla_r835a.inc file.

3.5 Registers

Port P1 Register P1 [address 00E1h]

b7							b0
0	0	0	1	0/1	0	0	0

Port P1_3 bit
0: Low level
1: High level

Port P1_4 bit
1: High level

Port P1 Direction Register PD1 [address 00E3h]

b7							b0
0	0	0	1	1	0	0	0

Port PD1_3 bit
1: Output mode

Port PD1_4 bit
1: Output mode (functions as TXD0 pin)

Port PD1_5 bit
0: Input mode (functions as RXD0 pin)

Port PD1_6 bit
0: Input mode (functions as CLK0 pin)

Watchdog Timer Reset Register WDTR [address 000Dh]

b7							b0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Writing 00h and then FFh to this register initializes the watchdog timer.

Note:
1. This setting is unnecessary when the watchdog timer is not used.

UART0 Pin Select Register U0SR [address 0188h]

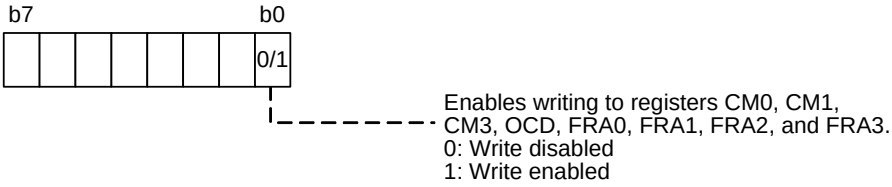
b7							b0
0	0	0	1	0	1	0	1

TXD0 pin select bit
1: P1_4 assigned

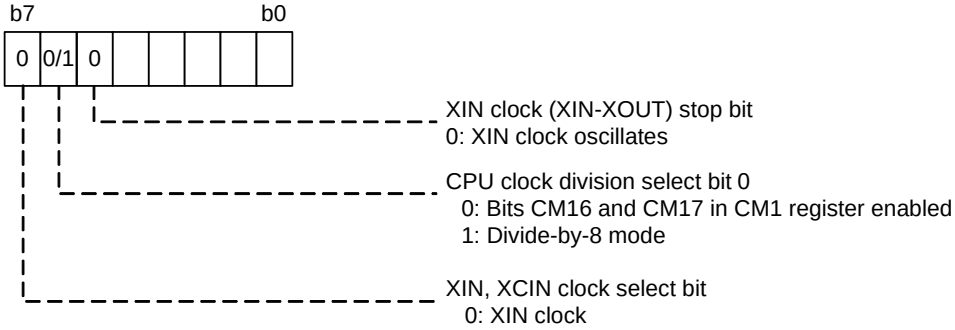
RXD0 pin select bit
1: P1_5 assigned

CLK0 pin select bit
1: P1_6 assigned

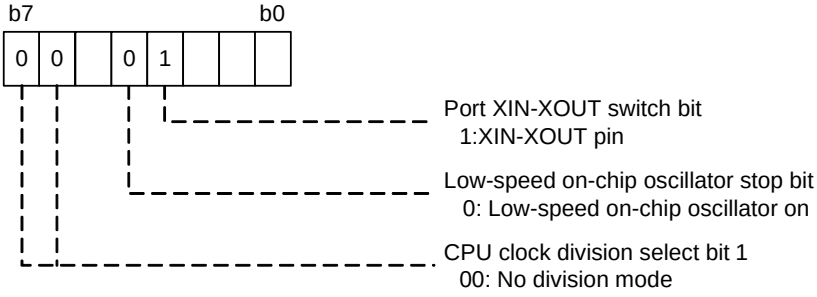
Protect Register PRCR [address 000Ah]



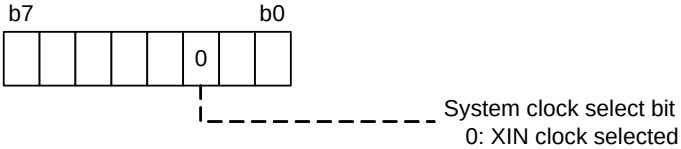
System Clock Control Register 0 CM0 [address 0006h]



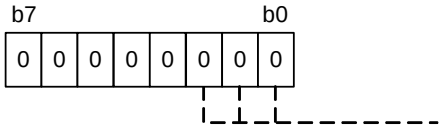
System Clock Control Register 1 CM1 [address 0007h]



Oscillation Stop Detection Register OCD [address 000Ch]

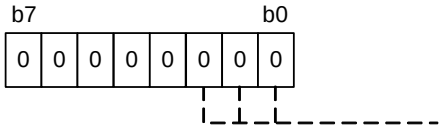


Interrupt Control Register S0TIC [address 0051h]



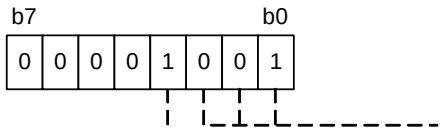
Interrupt priority level select bit
000: Level 0 (interrupt disabled)

Interrupt Control Register S0RIC [address 0052h]



Interrupt priority level select bit
000: Level 0 (interrupt disabled)

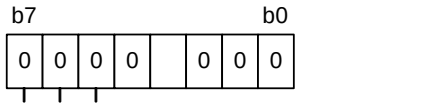
UART0 Transmit/Receive Mode Register U0MR [address 00A0h]



Serial I/O mode select bit
001: Clock synchronous serial I/O mode

Internal/external clock select bit
1: External clock

UART0 Transmit/Receive Control Register 0 U0C0 [address 00A4h]



Data output select bit
0: TXD0 pin set to CMOS output

CLK polarity select bit
0: Transmit data output at the falling edge and receive data input at the rising edge of the transfer clock

Transfer format select bit
0: LSB first

UART0 Transmit/Receive Control Register 1 U0C1 [address 00A5h]

b7							b0
0	0	0	0		0/1		0/1

Transmit enable bit
0: Transmission disabled
1: Transmission enabled

Transmit buffer empty flag
0: Data in the U0TB register
1: No data in the U0TB register

Receive enable bit
0: Reception disabled
1: Reception enabled

Receive complete flag
0: No data in the U0RB register
1: Data in the U0RB register

UART0 continuous receive mode enable bit
0: Continuous receive mode disabled

UART0 transmit buffer register U0TB [addresses 00A3h to 00A2h]

b15							b8	b7							b0
0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Transmit data

UART0 receive buffer register U0RB [addresses 00A7h to 00A6h]

b15							b8	b7							b0

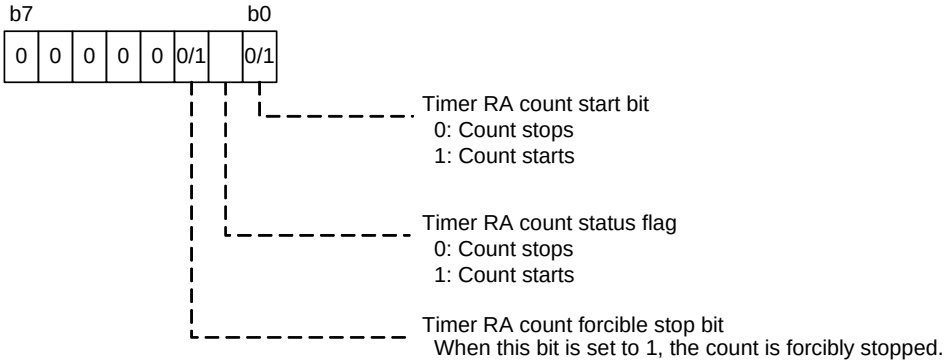
Receive data

Interrupt Control Register TRAIC [address 0056h]

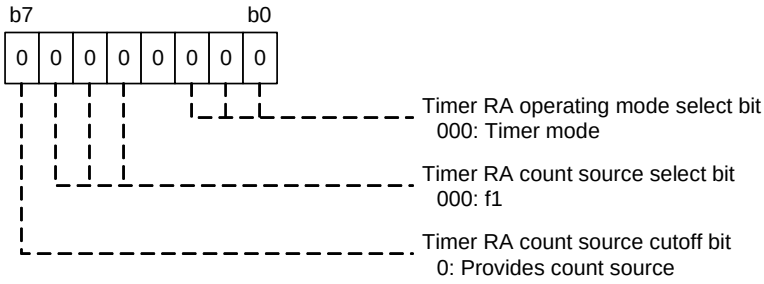
b7							b0
0	0	0	0	0	0	0	0

Interrupt priority level select bit
000: Level 0 (interrupt disabled)

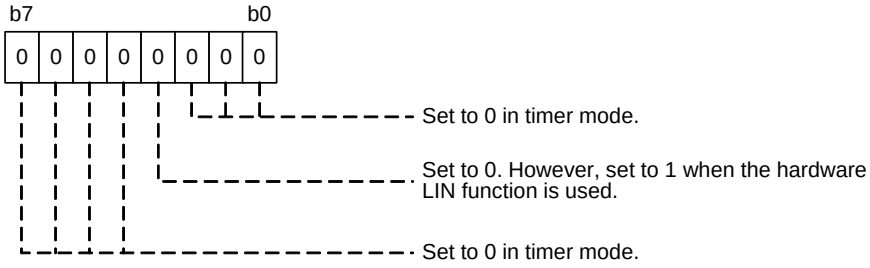
Timer RA Control Register TRACR [address 0100h]



Timer RA Mode Register TRAMR [address 0102h]

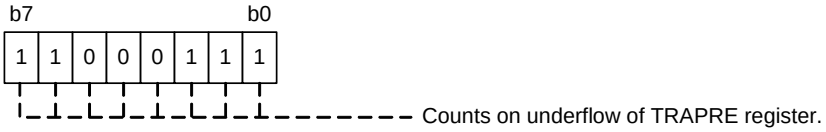


Timer RA I/O Control Register TRAIOC [address 0101h]

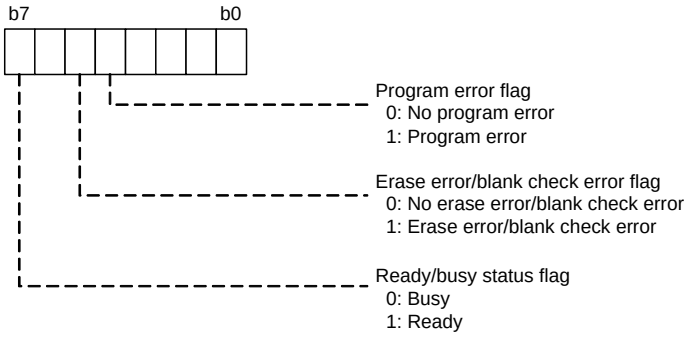


Timer RA Prescaler Register TRAPRE [address 0103h]

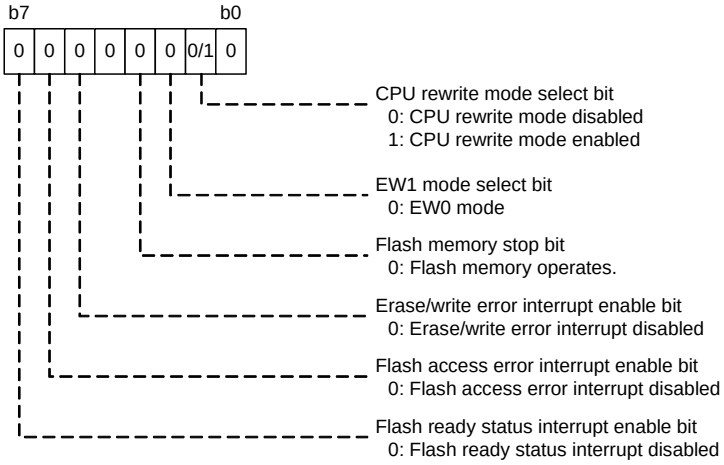
Timer RA Register TRA [address 0104h]



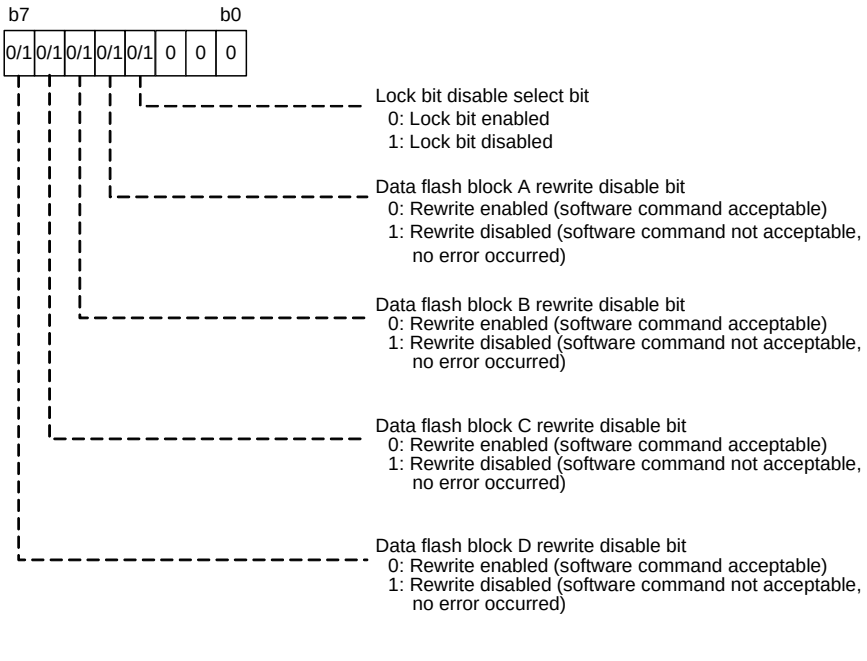
Flash Memory Status Register FST [address 01B2h]



Flash Memory Control Register 0 FMR0 [address 01B4h]



Flash Memory Control Register 1 FMR1 [address 01B5h]



3.6 Memory

Table 3.1 Memory

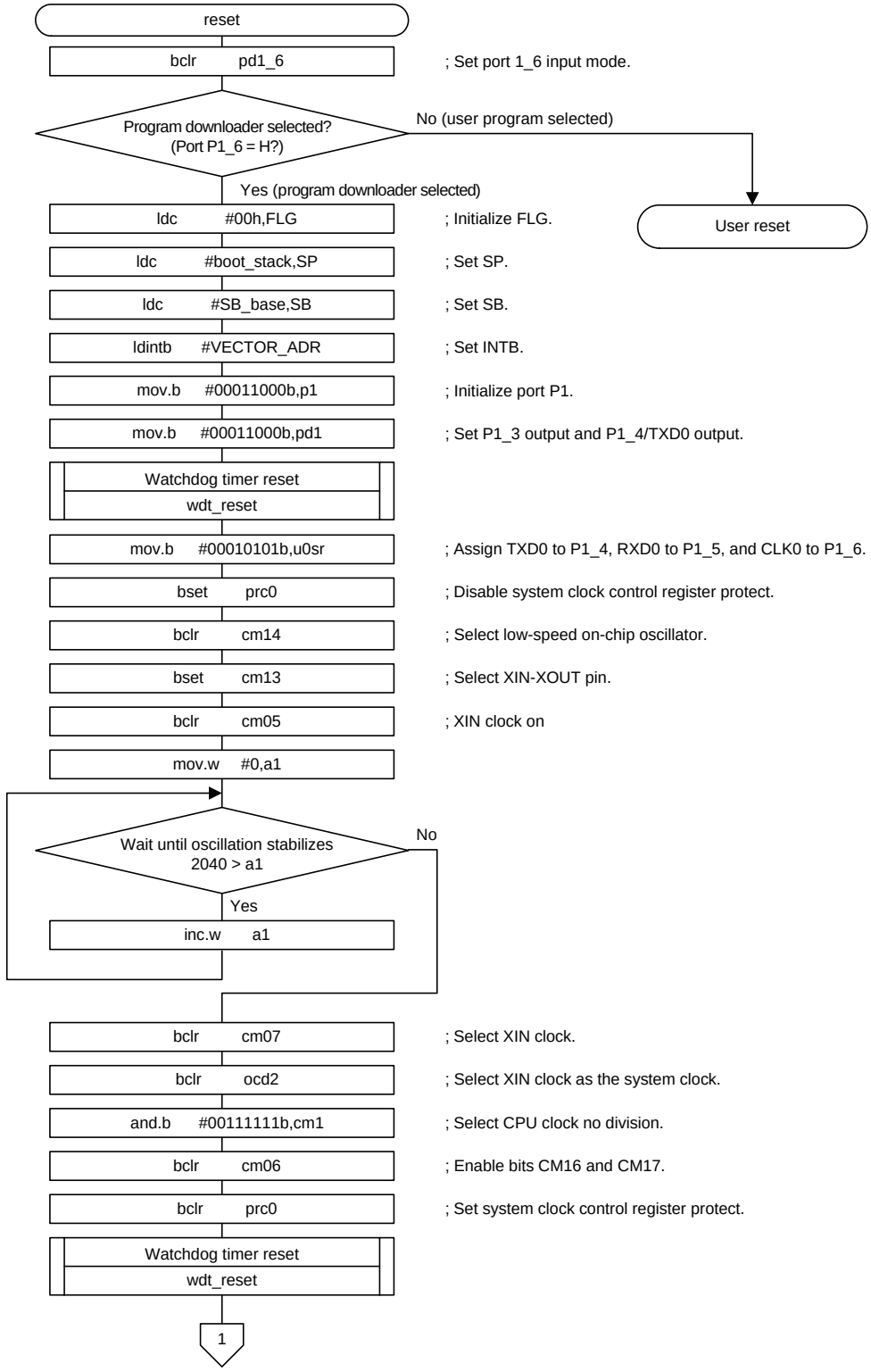
Assigned Memory	Size	Remarks
ROM	1330 bytes	System program only (including fixed vector and variable vector table)
RAM	427 bytes	System program only

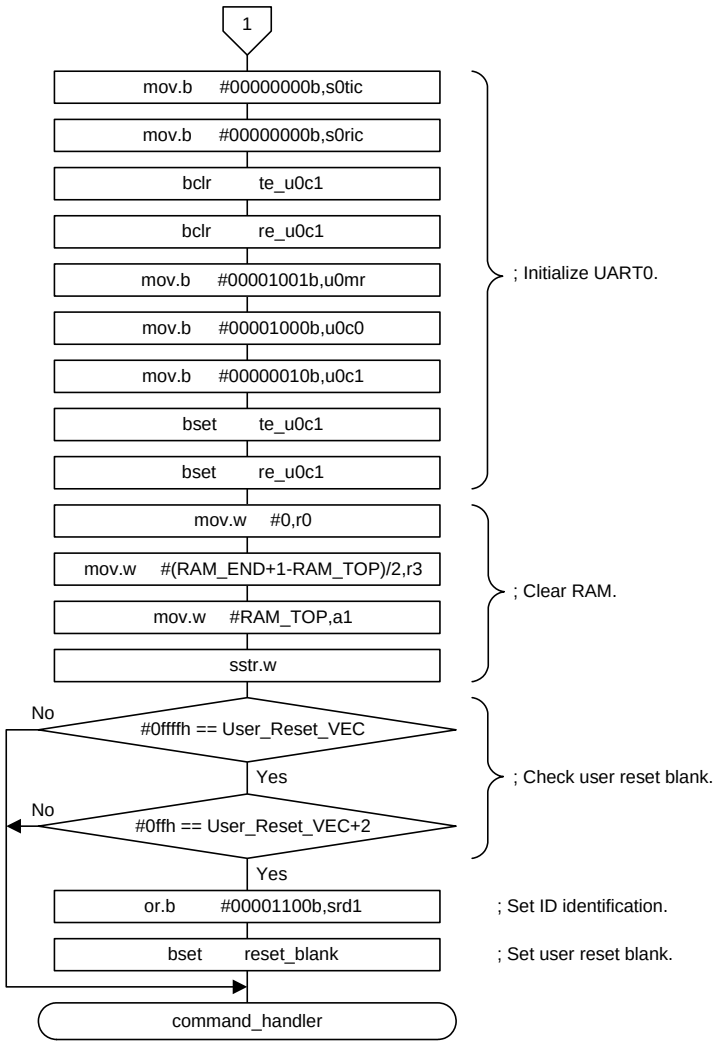
Table 3.2 RAM and Definitions

Symbol	Size	Description
ram_execute	128 bytes	EW0 mode program area
status_flags	1 byte	Serial flag area
reset_blank	–	User program blank flag
srd1	1 byte	SRD1 register
srd08	–	SR8 bit
srd09	–	SR9 bit
srd10	–	SR10 bit
srd11	–	SR11 bit
srd12	–	SR12 bit
srd13	–	SR13 bit
srd14	–	SR14 bit
srd15	–	SR15 bit
srd	1 byte	SRD register
address	4 bytes	Address data
temp	32 bytes	Temporary (used with the stack area)
rx_data	2 bytes	Receive data
tx_data	1 byte	Transmit data
page_buffer	256 bytes	Page buffer

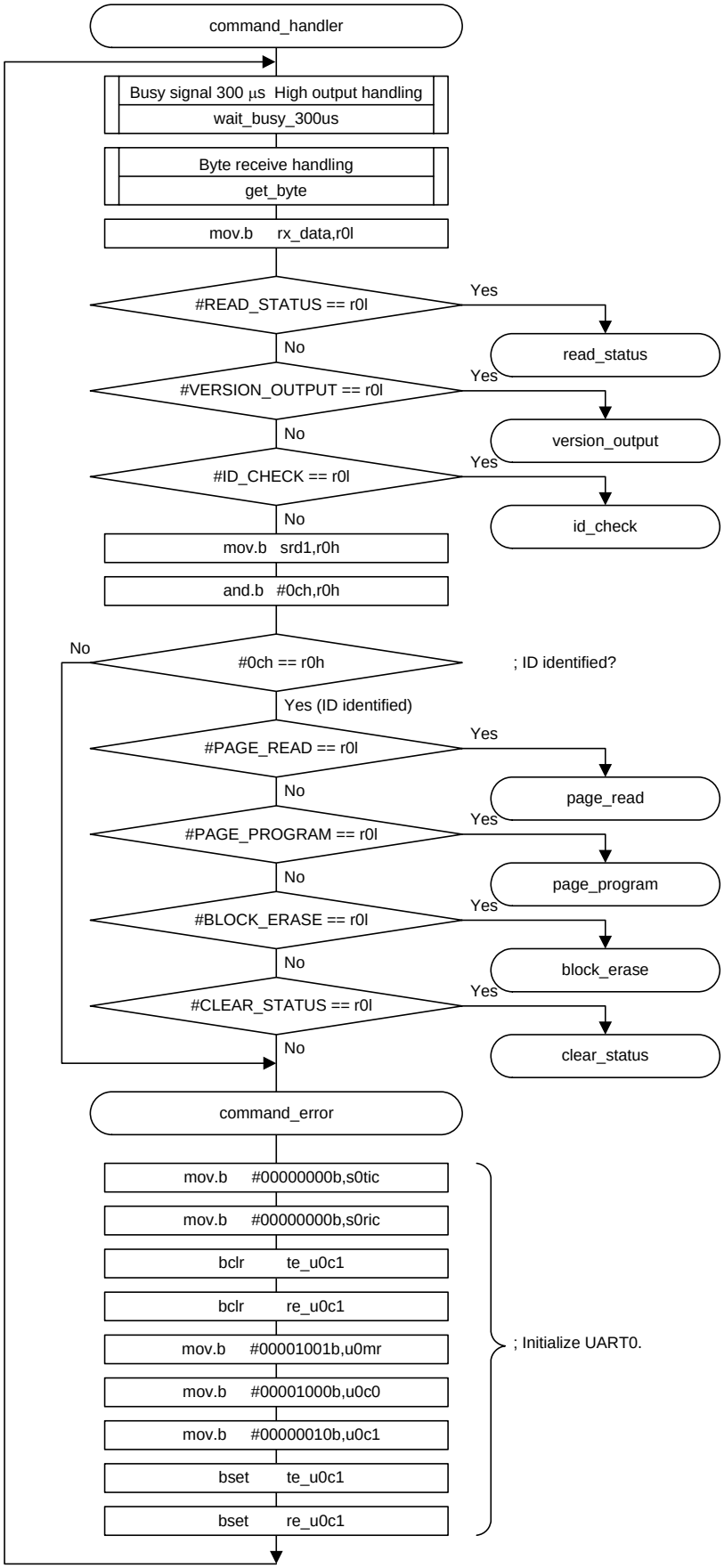
3.7 Flowchart

(1) Startup handling

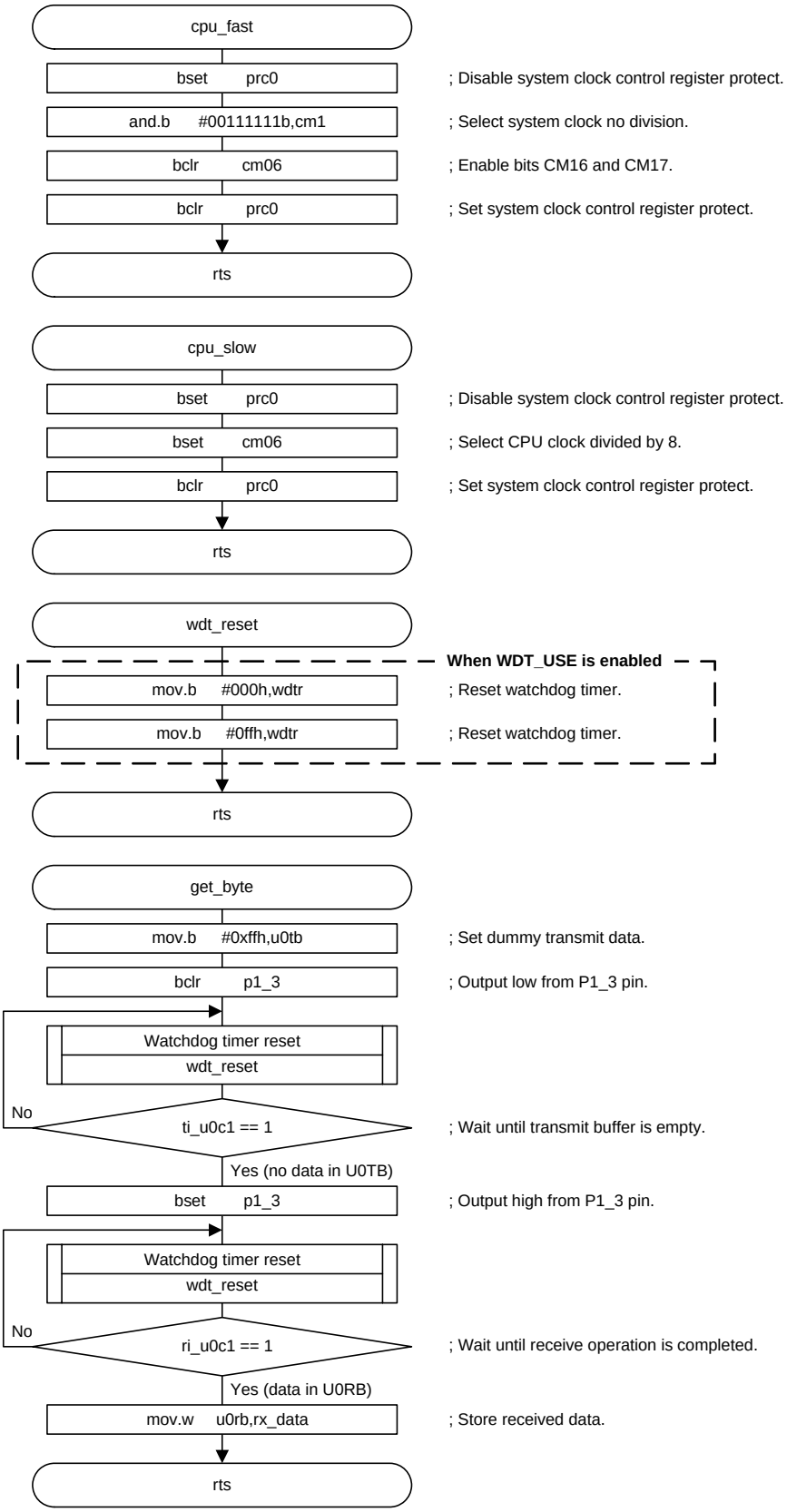



1
mov.b #00000000b,s0tic
mov.b #00000000b,s0ric
bclr te_u0c1
bclr re_u0c1
mov.b #00001001b,u0mr
mov.b #00001000b,u0c0
mov.b #00000010b,u0c1
bset te_u0c1
bset re_u0c1
; Initialize UART0.
mov.w #0,r0
mov.w #(RAM_END+1-RAM_TOP)/2,r3
mov.w #RAM_TOP,a1
sstr.w
; Clear RAM.
No
#0ffffh == User_Reset_VEC
Yes
No
#0ffh == User_Reset_VEC+2
Yes
; Check user reset blank.
or.b #00001100b,srd1
; Set ID identification.
bset reset_blank
; Set user reset blank.
command_handler

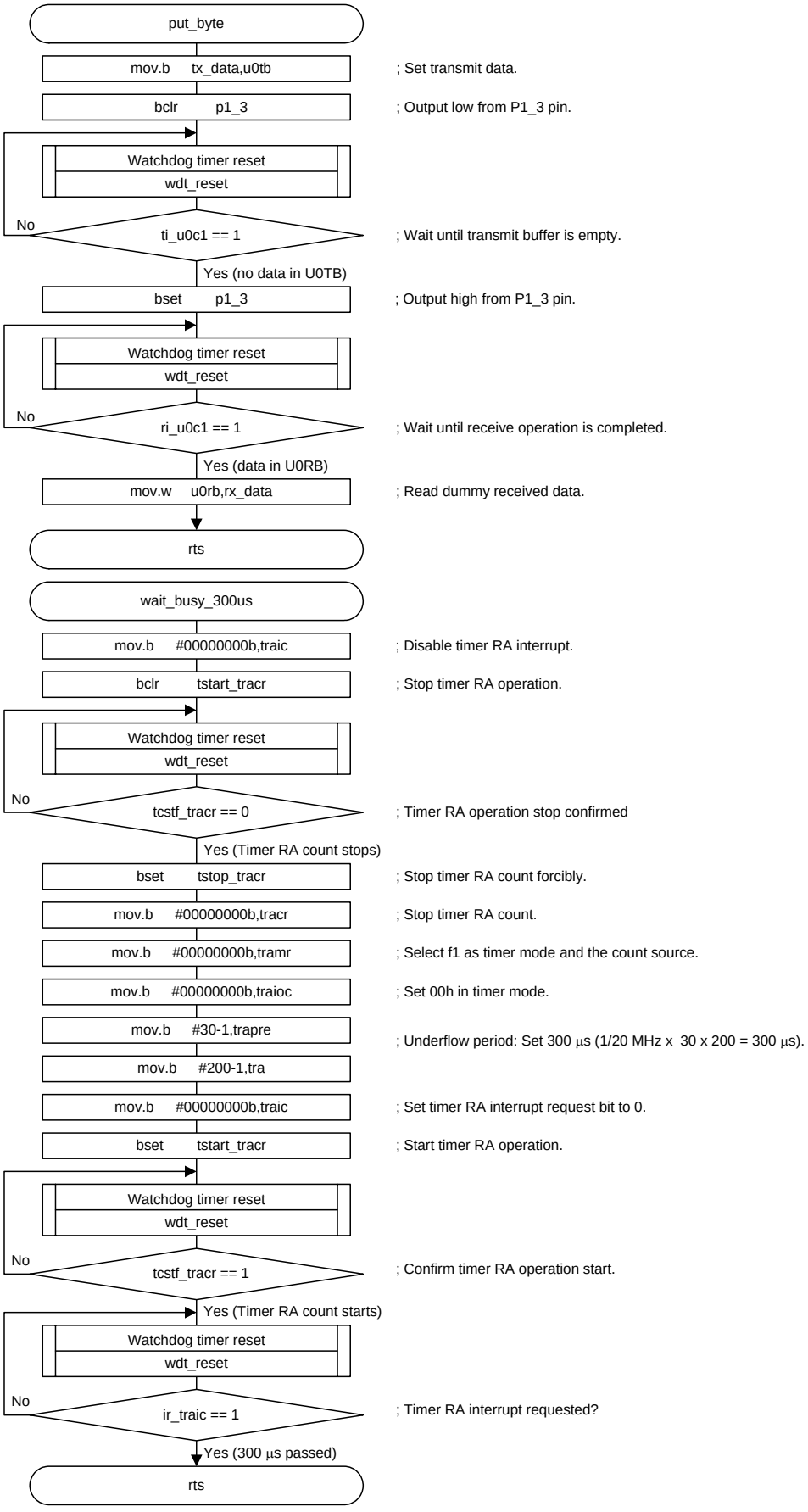
(2) Command handler



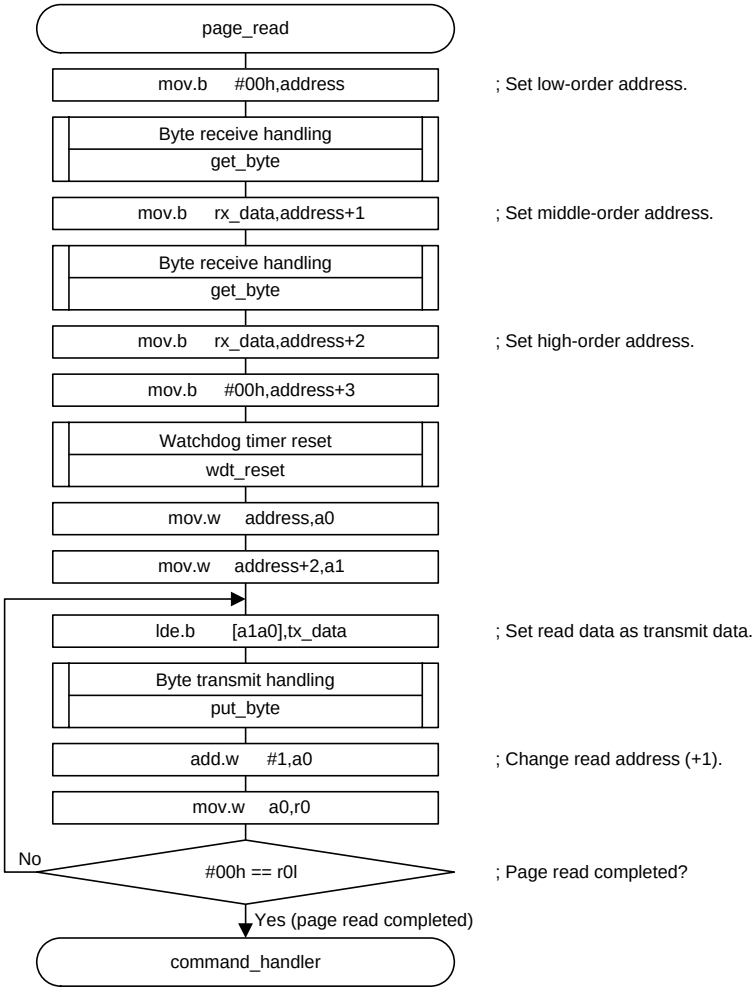
(3) Subroutine 1



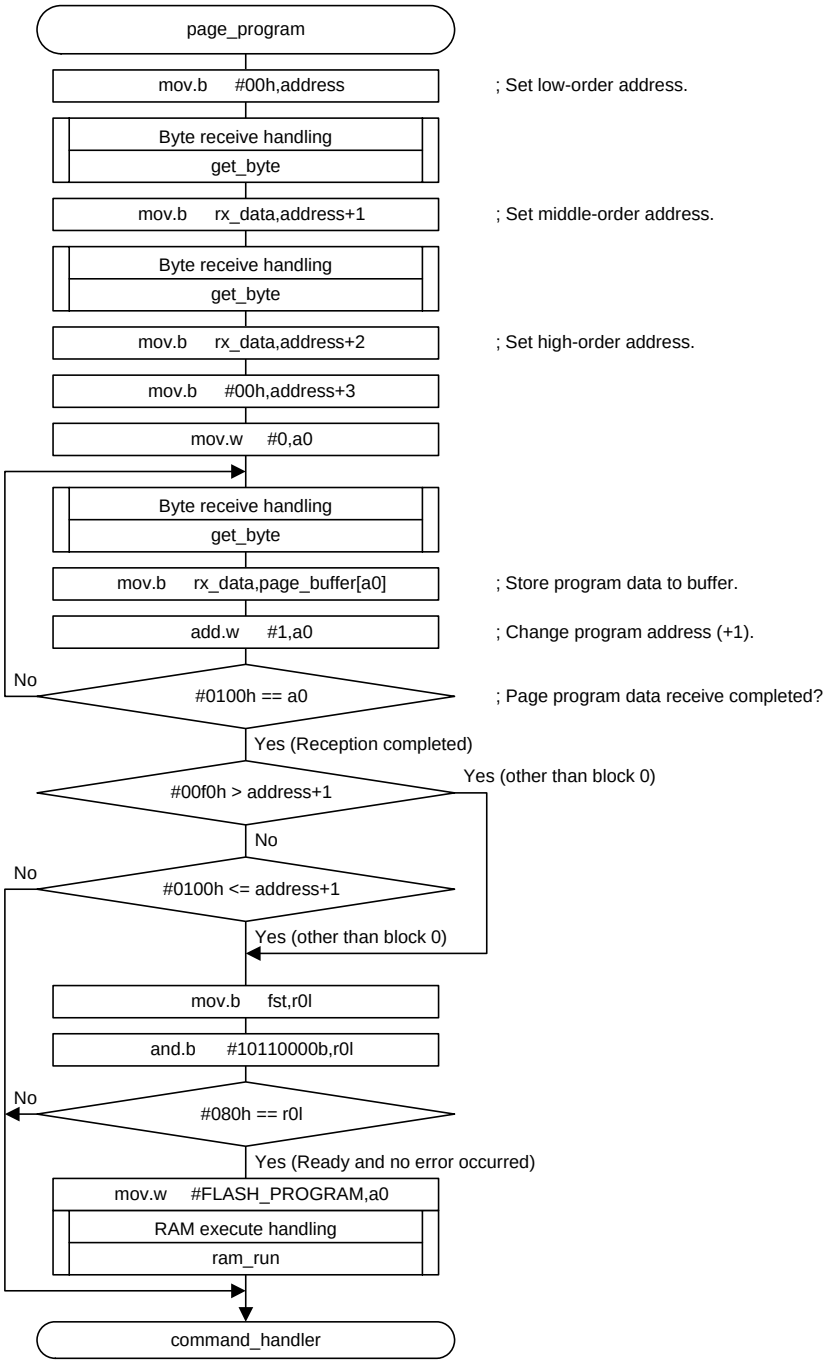
(4) Subroutine 2



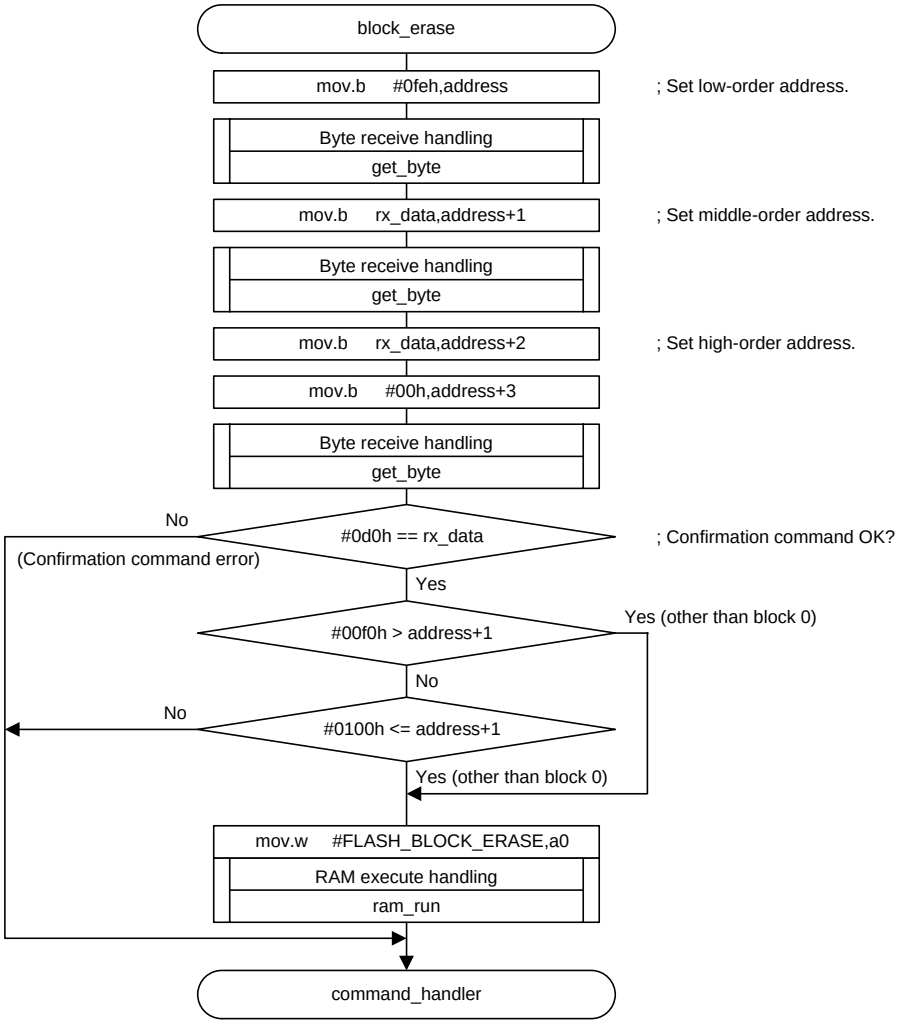
(5) Page read


page_read
mov.b #00h,address
; Set low-order address.
Byte receive handling
get_byte
mov.b rx_data,address+1
; Set middle-order address.
Byte receive handling
get_byte
mov.b rx_data,address+2
; Set high-order address.
mov.b #00h,address+3
Watchdog timer reset
wdt_reset
mov.w address,a0
mov.w address+2,a1
lde.b [a1a0],tx_data
; Set read data as transmit data.
Byte transmit handling
put_byte
add.w #1,a0
; Change read address (+1).
mov.w a0,r0
No
#00h == r0l
; Page read completed?
Yes (page read completed)
command_handler

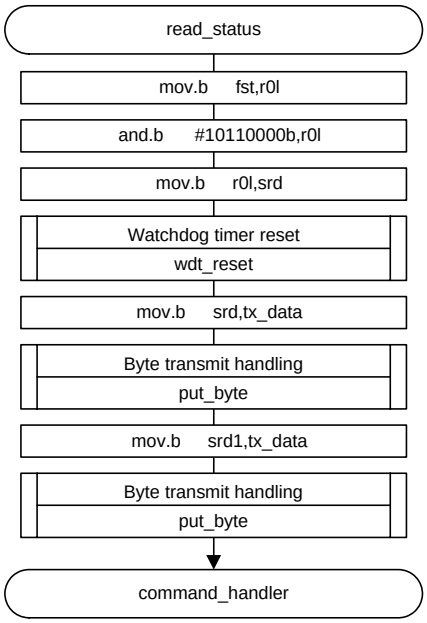
(6) Page program



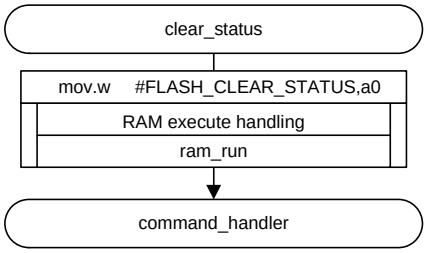
(7) Block erase



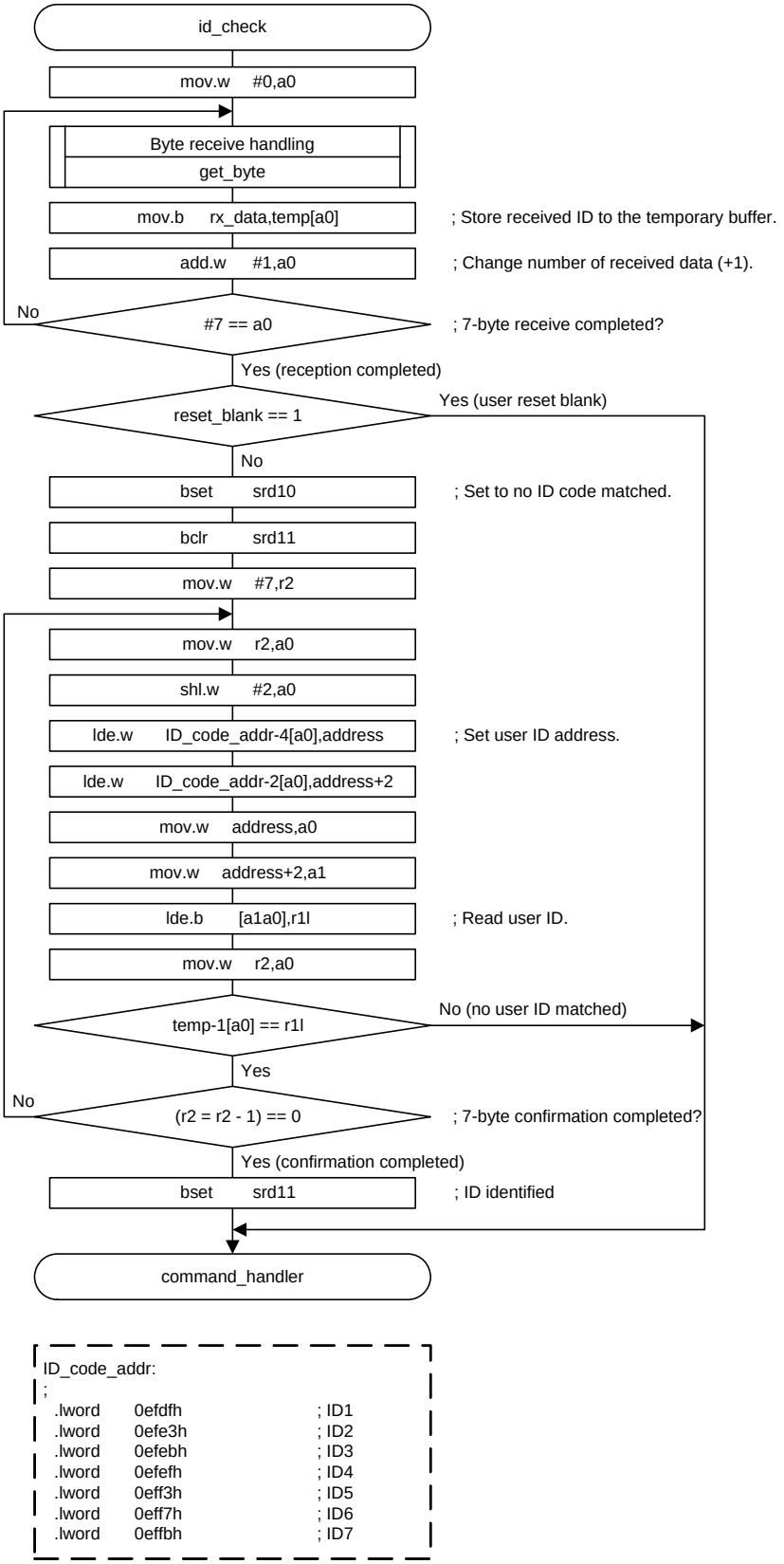
(8) Read status register



(9) Clear status register

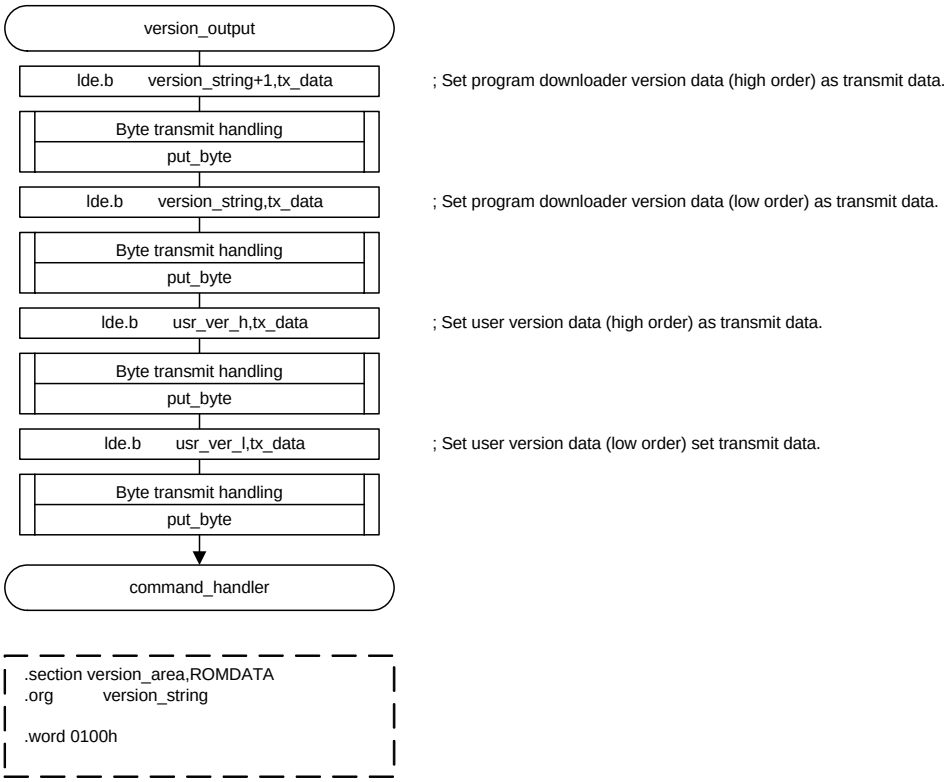


(10) ID check



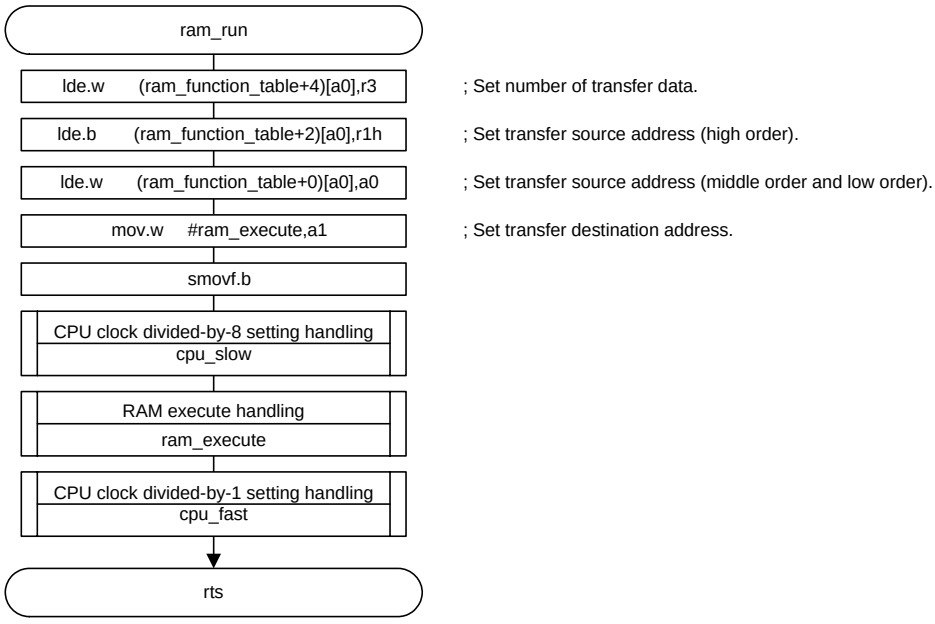

```
ID_code_addr:
;
  .lword    0efdfh          ; ID1
  .lword    0efe3h          ; ID2
  .lword    0efebh          ; ID3
  .lword    0efefh          ; ID4
  .lword    0eff3h          ; ID5
  .lword    0eff7h          ; ID6
  .lword    0effbh          ; ID7
```

(11) Version output function



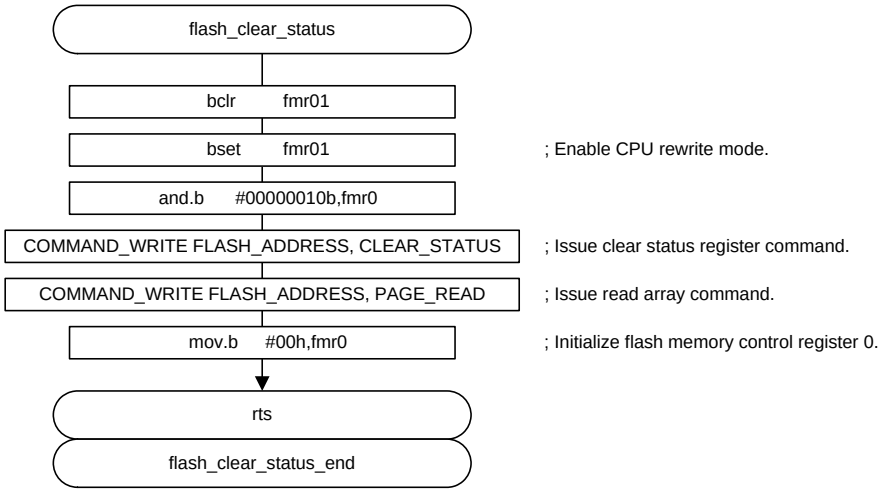

```
.section version_area,ROMDATA
.org          version_string

.word 0100h
```

(12) RAM execute routine

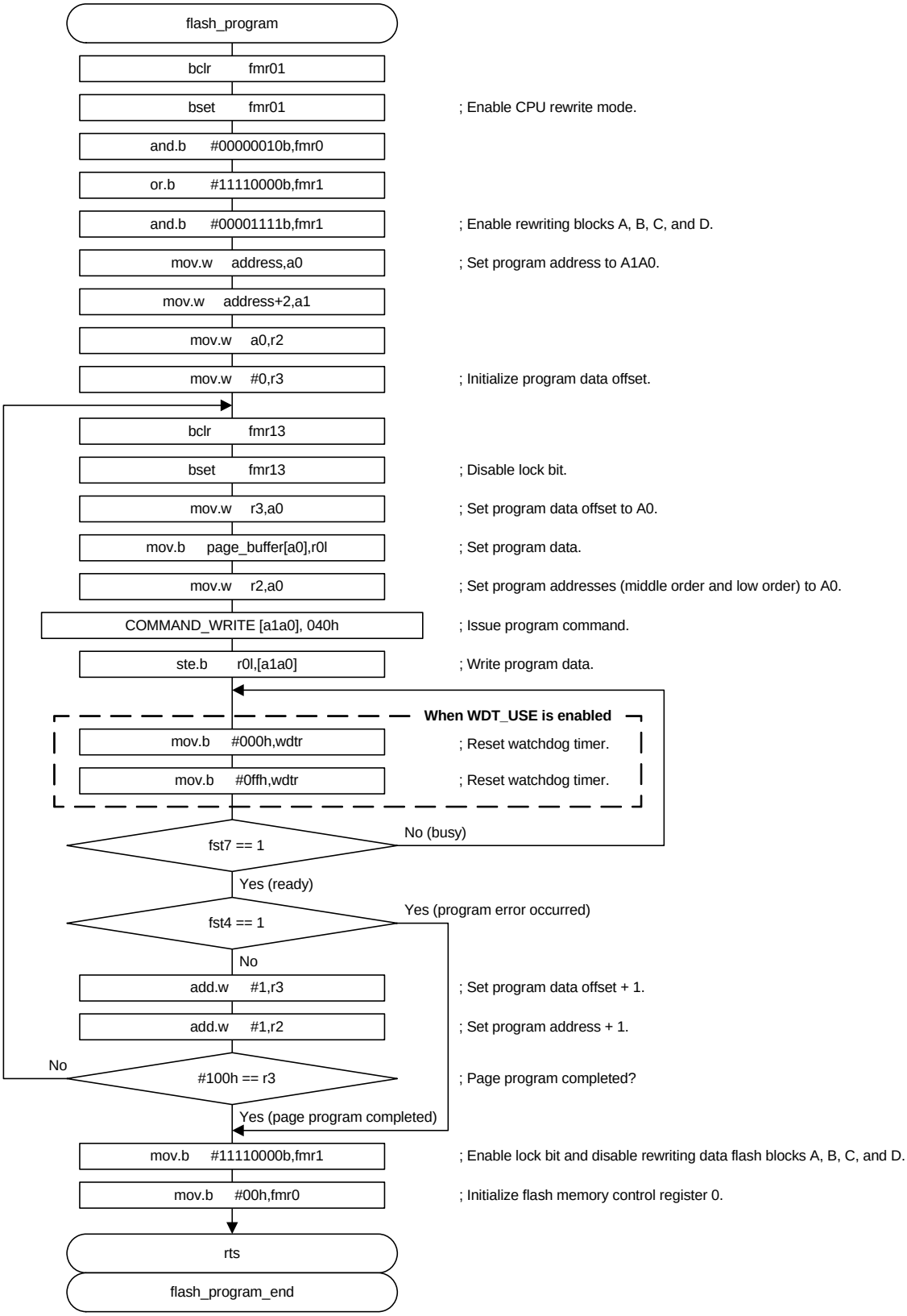



```
ram_function_table:
;
  .lword flash_clear_status
  .word  flash_clear_status_end - flash_clear_status

  .lword flash_program
  .word  flash_program_end - flash_program

  .lword flash_block_erase
  .word  flash_block_erase_end - flash_block_erase
```

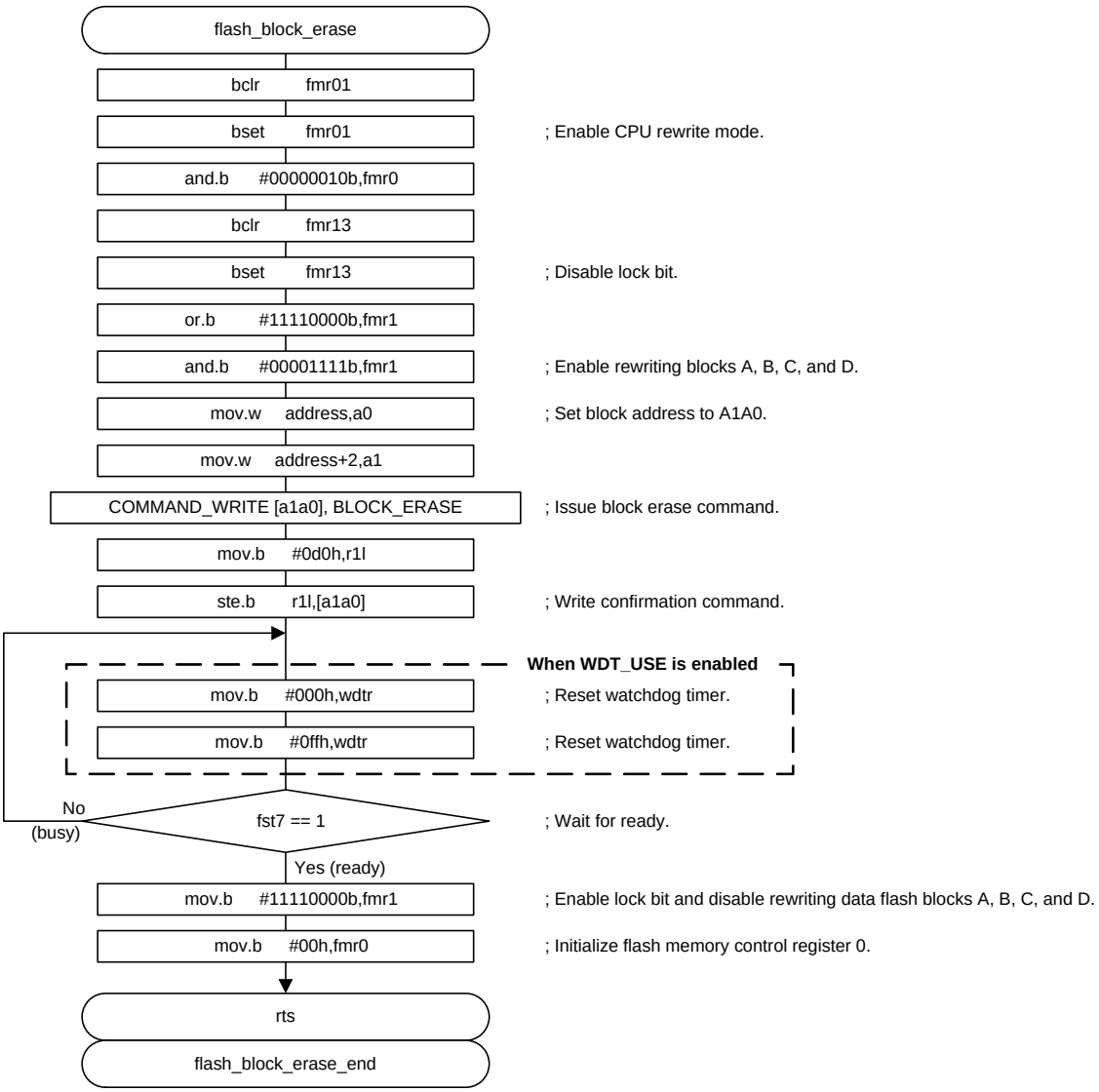
(13) Clear status register to flash memory (execute in RAM)



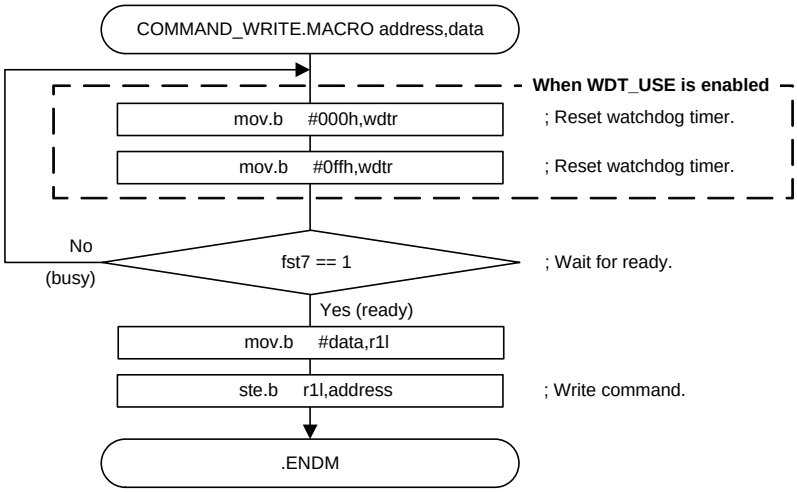
(14) Page program to flash memory (execute in RAM)



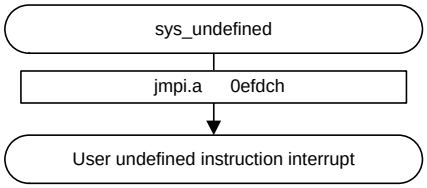
(15) Block erase to flash memory (execute in RAM)

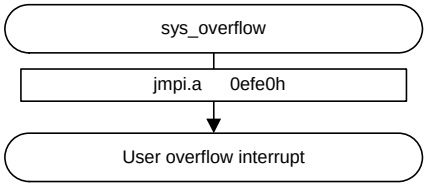


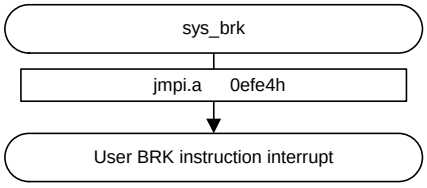
(16) Command write macro

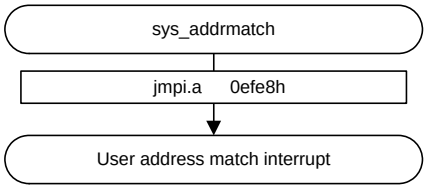


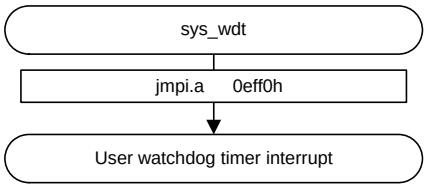
(17) System interrupt handling











4. Downloader Communication Protocol

4.1 Commands

4.1.1 Control Command List

Control commands are listed below.

Control Command	1 Byte	2 Bytes	3 Bytes	4 Bytes	5 Bytes	6 Bytes	7 Bytes or More	ID Unchecked
Page read	FFH	Middle-order address	High-order address	Data	Data	Data	Up to data	Not acceptable
Page program	41H	Middle-order address	High-order address	Data	Data	Data	Up to data	Not acceptable
Block erase	20H	Middle-order address	High-order address	D0H				Not acceptable
Read status register	70H	SRD	SRD1					Acceptable
Clear status register	50H							Not acceptable
ID check function	F5H	ID1	ID2	ID3	ID4	ID5	Up to ID7	Acceptable
Version information output function	FBH	Program downloader version		User version				Acceptable

SRD: Status register data
SRD1: Status register data 1

Notes:
1. The shadowed areas show a transfer from the MCU (program downloader) to a programmer, the rest show a transfer from a programmer to the MCU (program downloader).
2. User program area blank product IDs are identified and all commands can be accepted.
3. The number of receive data is not checked and the timeout error is not processed in the downloader. When transmitting a command, make sure there is no excess or shortage of data.

4.2 Page Read

4.2.1 Operation

The page read command reads the specified user ROM area in the flash memory in units of 256 bytes. Specify the area to be read by the high-order addresses (A16 to A23) and middle-order addresses (A8 to A15). The target bytes are the 256 bytes from addresses xxxx00h to xxxxFFh.

4.2.2 Packet

	1st byte	2nd byte	3rd byte	4th byte	Up to 259th byte
	Command	Address		Data	Up to data
Programmer to MCU	FFh	Middle-order address	High-order address		
MCU to Programmer				Data 0	Up to Data 255

Data 0: Low-order address is 00h
Data 255: Low-order address is FFh

4.2.3 Procedure

(1) The page read command FFh is received at the first byte.
(2) The middle-order address is received at the second byte and the high-order address is received at the third byte.
(3) The content in the low-order address 00h is sequentially transmitted from the fourth byte.

4.3 Page Program

4.3.1 Operation

The page program command programs the data to the specified user ROM area in the flash memory in units of 256 bytes. Specify the area to be programmed by the high-order addresses (A16 to A23) and middle-order addresses (A8 to A15). The target bytes are the 256 bytes from addresses xxxx00h to xxxxFFh.

4.3.2 Packet

	1st byte	2nd byte	3rd byte	4th byte	Up to 259th byte
	Command	Address		Data	Up to data
Programmer to MCU	41h	Middle-order address	High-order address	Data 0	Up to Data 255
MCU to Programmer					

Data 0: Low-order address is 00h
Data 255: Low-order address is FFh

4.3.3 Procedure

(1) The page program command 41h is received at the first byte.
(2) The middle-order address is received at the second byte and the high-order address is received at the third byte.
(3) The programming data to the low-order address 00h is received from the fourth byte.

When the programming data is less than 256 bytes, transmit FFh for the shortage. When programming data is more than 257 bytes, the data at the 257th byte is considered to be the data in the next command. If an error occurs during programming, SR4 becomes 1 (program status ends in error).

After executing this command, confirm the status of the flash memory with the read status register command.

4.4 Block Erase

4.4.1 Operation

The block erase command erases a specified block area in the user ROM area of the flash memory. Specify a block area by the eight high-order bits (A16 to A23) and eight middle-order bits (A8 to A15) at a given address of the block to be erased.

4.4.2 Packet

	1st byte	2nd byte	3rd byte	4th byte	Up to 259th byte
	Command	Block address		Confirmation command	
Programmer to MCU	20h	Middle-order address	High-order address	D0h	
MCU to Programmer					

4.4.3 Procedure

(1) The block erase command 20h is received at the first byte.
(2) The middle-order address is received at the second byte and the high-order address is received at the third byte.
(3) The confirmation command D0h is received at the fourth byte.

After receiving the confirmation command D0h, erasing to the specified block starts. The erase operation sets the contents of the flash memory to FFh. If an error occurs, SR5 becomes 1 (erase status ends in error).

After executing this command, confirm the status of the flash memory with the read status register command.

4.5 Read Status Register

4.5.1 Operation

The read status register command confirms the operating status of the flash memory.

4.5.2 Packet

	1st byte	2nd byte	3rd byte	4th byte	Up to 259th byte
	Command	SRD			
Programmer to MCU	70h				
MCU to Programmer		SRD output	SRD1 output		

SRD: Status register data
SRD1: Status register data 1

4.5.3 Procedure

(1) The read status register command 70h is received at the first byte.
(2) SRD is transmitted at the second byte.
(3) SRD1 is transmitted at the third byte.

4.5.4 SRD Register

Each Bit of SRD	Status Name	Definition	
		1	0
SR7 (bit 7)	Sequencer status	Ready	Busy
SR6 (bit 6)	Reserved		
SR5 (bit 5)	Erase status	Error	Completed normally
SR4 (bit 4)	Program status	Error	Completed normally
SR3 (bit 3)	Reserved		
SR2 (bit 2)	Reserved		
SR1 (bit 1)	Reserved		
SR0 (bit 0)	Reserved		

(1) Sequencer status
The sequencer status shows the operating status of the flash memory. This bit becomes 0 (busy) during auto-programming or auto-erasing. This bit becomes 1 (ready) during auto-programming or auto-erasing.
(2) Erase status
The erase status shows the erase operating status. If an error occurs, this bit becomes 1. This bit is set to 0 when the clear status register command is executed.
(3) Program status
The program status shows the programming status. If an error occurs, this bit becomes 1. This bit is set to 0 when the clear status register command is executed.

Both SR5 and SR4 become 1 in the following cases:
- The defined command is not written correctly.
- Data other than values which can be written to the second bus cycle data of the block erase command (D0h or FFh) is written in the cycle to input the block erase confirmation command. When FFh is written, the MCU enters read array mode and the command is canceled.

(4) Reserved bit
When read, the content is undefined.

4.5.5 SRD1 Register

Each Bit of SRD1	Status Name	Definition	
		1	0
SR15 (bit 7)	Reserved		
SR14 (bit 6)	Reserved		
SR13 (bit 5)	Reserved		
SR12 (bit 4)	Reserved		
SR11 (bit 3)	ID check	00: Not checked 01: ID Not matched 10: Reserved 11: Checked	
SR10 (bit 2)			
SR9 (bit 1)	Reserved		
SR8 (bit 0)	Reserved		

(1) ID check
These bits indicate the ID check results.

(2) Reserved bit
When read, the content is undefined.

4.6 Clear Status Register

4.6.1 Operation

The clear status register command initializes a status register. Initialize the status register before executing the erase or the page program to the flash memory.

4.6.2 Packet

	1st byte	2nd byte	3rd byte	4th byte	Up to 259th byte
	Command				
Programmer to MCU	50h				
MCU to Programmer					

4.6.3 Procedure

(1) The clear status register command 50h is received at the first byte.

4.7 ID Check Function

4.7.1 Operation

This function compares the ID received from the programmer and the user ID code stored in the virtual fixed vector address. The ID check results are stored in SR11 to SR10 in the SRD1 register.

4.7.2 Packet

	1st Byte	2nd Byte	3rd Byte	4th Byte	Up to 8th Byte
	Command	ID			
Programmer to MCU	F5h	ID1	ID2	ID3	Up to ID7
MCU to Programmer					

4.7.3 Procedure

(1) The ID check function command F5h is received at the first byte.
(2) ID1 to ID7 are received from the second byte to the eighth byte, respectively.

After receiving the ID, the ID check starts. However, a user program area blank product returns the wait state for the control command from the programmer without performing ID check. When ID1 to ID7 all match, SR11 to SR10 become 11b (verified). If any of the IDs do not match, SR11 to SR10 become 01b (verify not matched).

4.8 Version Information Output Function

4.8.1 Operation

This function transmits version information of the program downloader and user program.

4.8.2 Packet

	1st Byte	2nd Byte	3rd Byte	4th Byte	5th Byte	Up to 259th Byte
	Command	Version				
Programmer to MCU	F8h					
MCU to Programmer		Program downloader		User		

4.8.3 Procedure

(1) The version information output function command FBh is received at the first byte.
(2) The program downloader version is transmitted at the high-order second byte first and then the low-order third byte.
(3) The user program version is transmitted at the high-order fourth byte first and then low-order fifth byte.

4.8.4 Version Data

For the example shown below, the program download version is transmitted after 01h is set to the high order and 00h to the low order of the program downloader version, and 00h is set to the high order and 10h to the low order of the user version.

When the program downloader version is Ver.1.00 and the user version is Ver.0.10:

Program downloader version data
(in the bt_r835a.a30 file)

```
  .org        version_string

  .word       0100h                ; Program Downloader version (Ver.1.00)
```

User version data
(in the sect30.inc file for 6. User Program Example)

```
User_Ver   .equ        0010h     ; User version (Ver.0.10)
```

5. Error Handling

5.1 Serial Transmit and Receive

(1) If the P1_3 pin does not become low during a 300 µs period, the flash MCU is in a command wait state.
(2) If the received data does not match the first byte of the control command, the flash MCU determines that a receive error has occurred. After outputting high to the P1_3 pin for 300 µs, the flash MCU enters a command wait state.

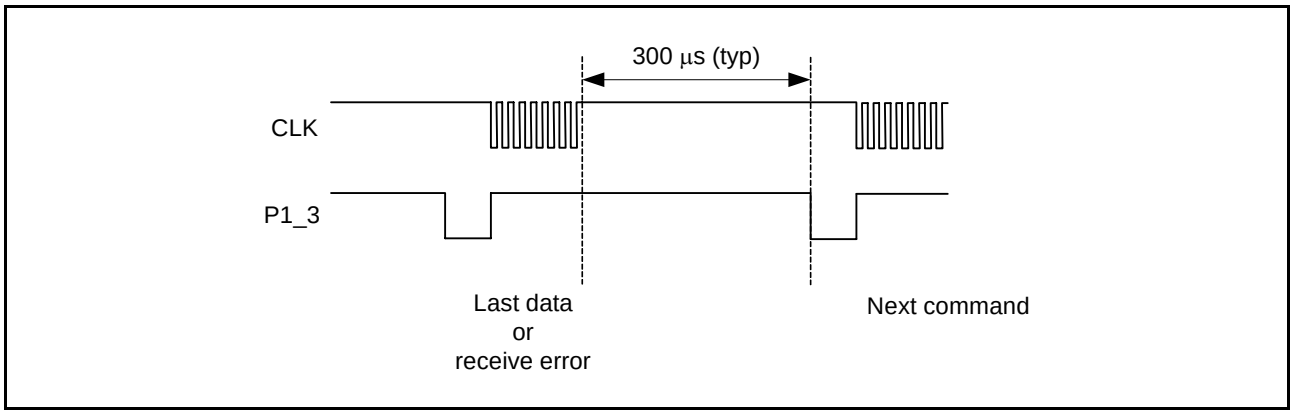


Figure 5.1 Serial Communication Provision

6. User Program Example

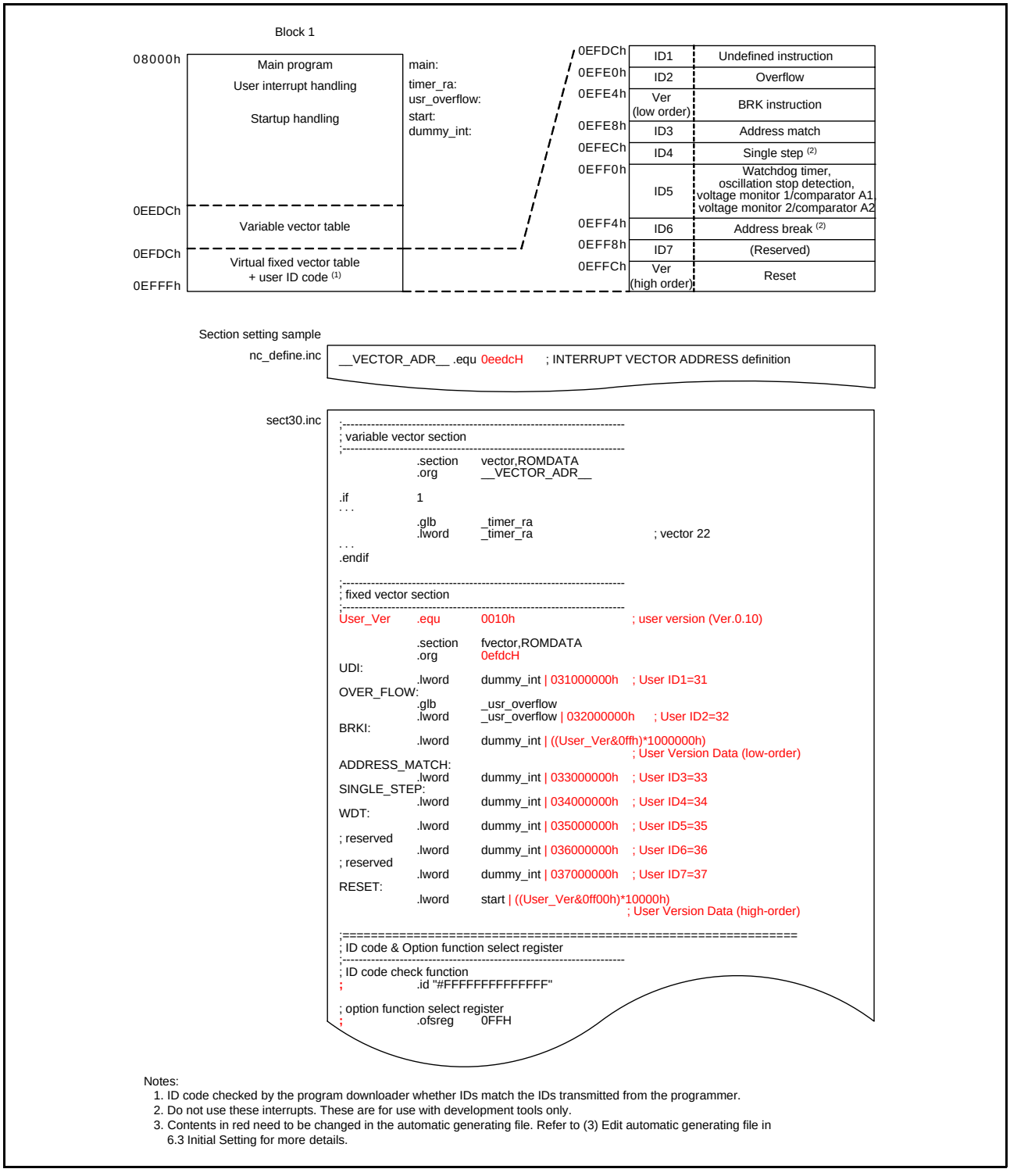
The program downloader rewrites the user programs other than the user program in block 0 according to the programmer. An example of the user program is shown below.

6.1 Function

The LEDs connected to I/O ports P3_1, P3_3, P3_4, and P3_6 light.

6.2 Memory Map

Figure 6.1 shows a User Program Memory Map.



Notes:
1. ID code checked by the program downloader whether IDs match the IDs transmitted from the programmer.
2. Do not use these interrupts. These are for use with development tools only.
3. Contents in red need to be changed in the automatic generating file. Refer to (3) Edit automatic generating file in 6.3 Initial Setting for more details.

Figure 6.1 User Program Memory Map

6.3 Initial Settings

(1) Vector table

Allocate the virtual fixed vector table to block 1 to use an interrupt by the user program.

(2) ID code

Set an ID code in the virtual fixed vector table. Do not opt to generate an ID code file when compiling.

(3) Edit automatic generating file

When the project type is made in the Application and the initial setting file is automatically generated by the High-performance Embedded Workshop (HEW), change the sect30.inc file and nc_define.inc file as follows (see Figure 6.1):

- Change the allocation address of the locatable table to 0EEDCh, and the virtual fixed vector table to 0EFDCh.
- Set an additional ID code to the virtual fixed vector table.
- Add the symbol definition of the user version data and user version data setting to the virtual fixed vector table.
- Comment out the assembler expansion function direction instructions ".ID" (set an ID code) and ".OFSREG" (set a value to the OFS register).

7. Programmer Example

7.1 Control Pins

(1) Pins TXD, RXD, and CLK

These pins are for transmitting and receiving in clock synchronous serial I/O mode. The CLK pin is shared with the selection pin of the program downloader or the user program.

(2) P1_3 pin

This pin is the BUSY signal for the transmit and receive control.

(3) $\overline{\text{RESET}}$ pin

This pin controls an MCU reset from the programmer.

(4) Pins VCC and VSS

Adjust high level from the programmer to the MCU's VCC level and low level from the programmer to the MCU's VSS level, respectively.

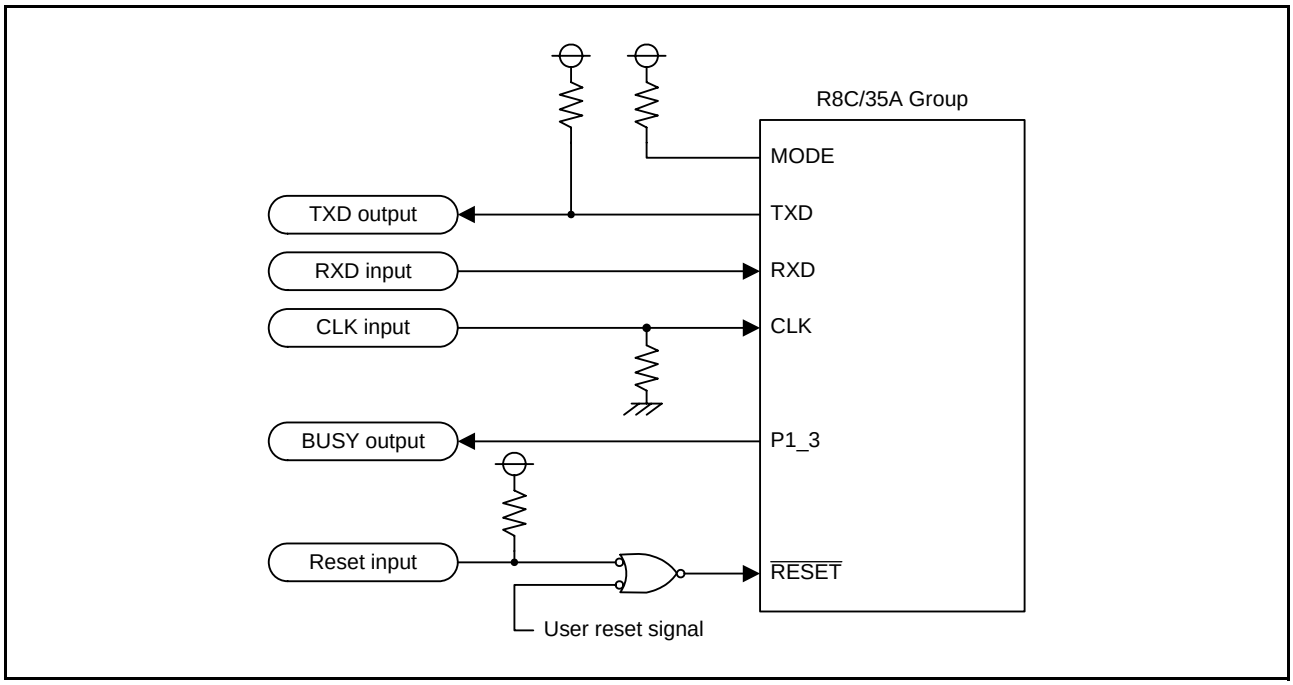


Figure 7.1 Programmer Configuration

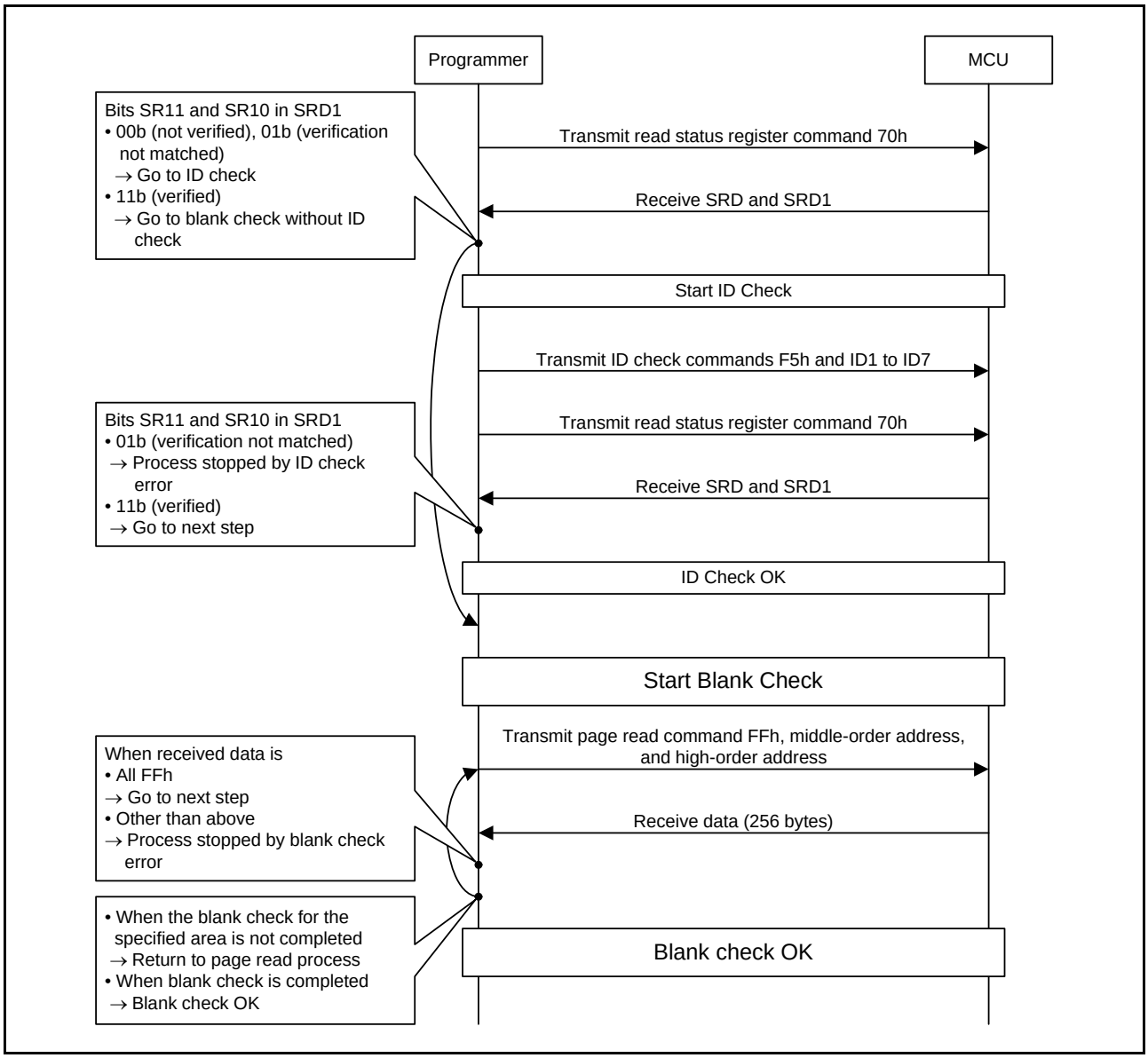
7.2 Programmer Functions

The following are the functions necessary for the programmer:

- Blank Check
- Erase
- Program
- Verify
- Read

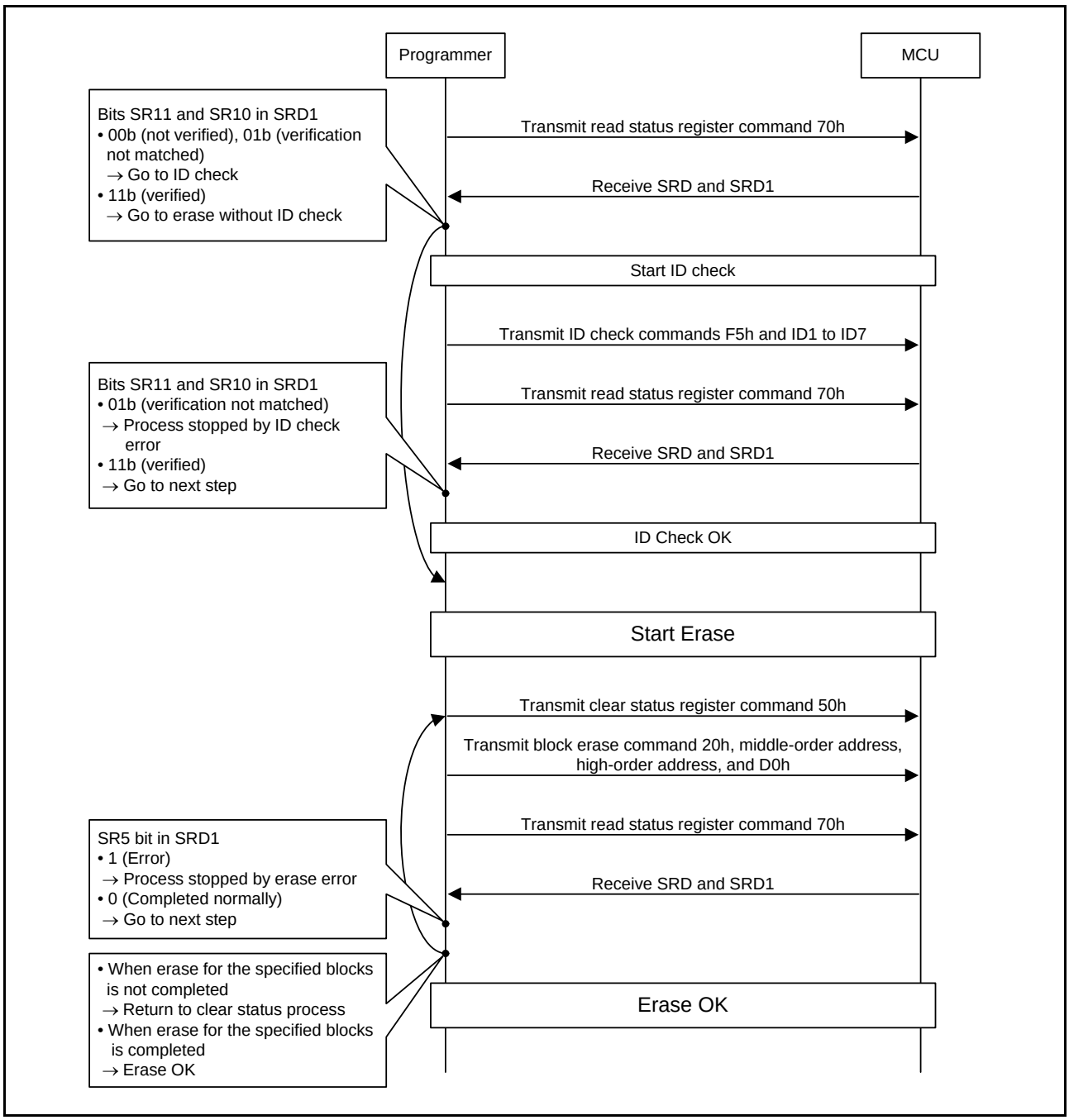
7.3 Blank Check

Data (program) in the specified area automatically or manually is read from the MCU's on-chip flash memory. The programmer confirms that all read data is blank (FFh).



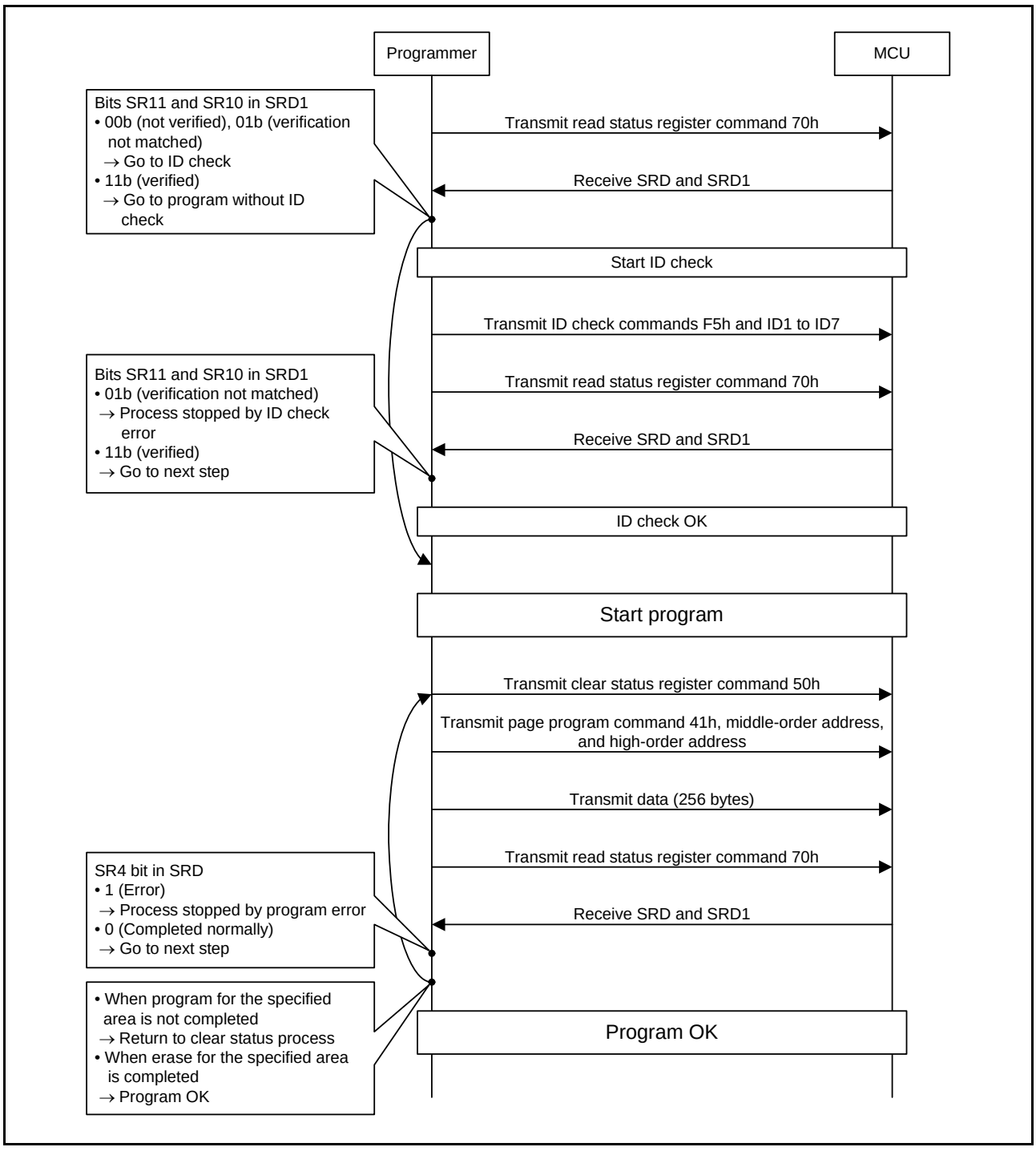
7.4 Erase

Data (program) in the MCU's specified on-chip flash memory blocks automatically or manually is erased.



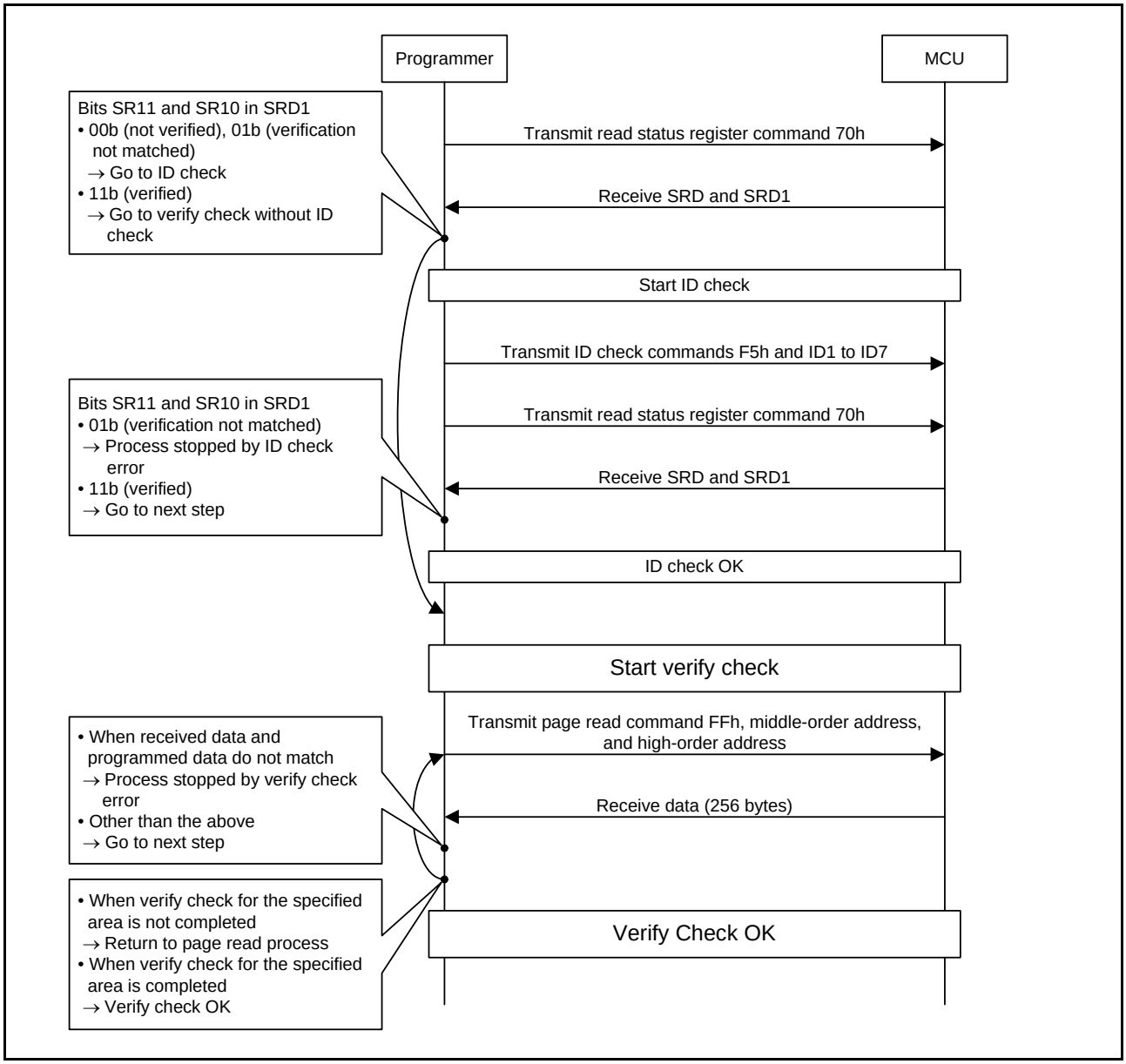
7.5 Program

Data (program) in the MCU's specified on-chip flash memory area automatically or manually is programmed.



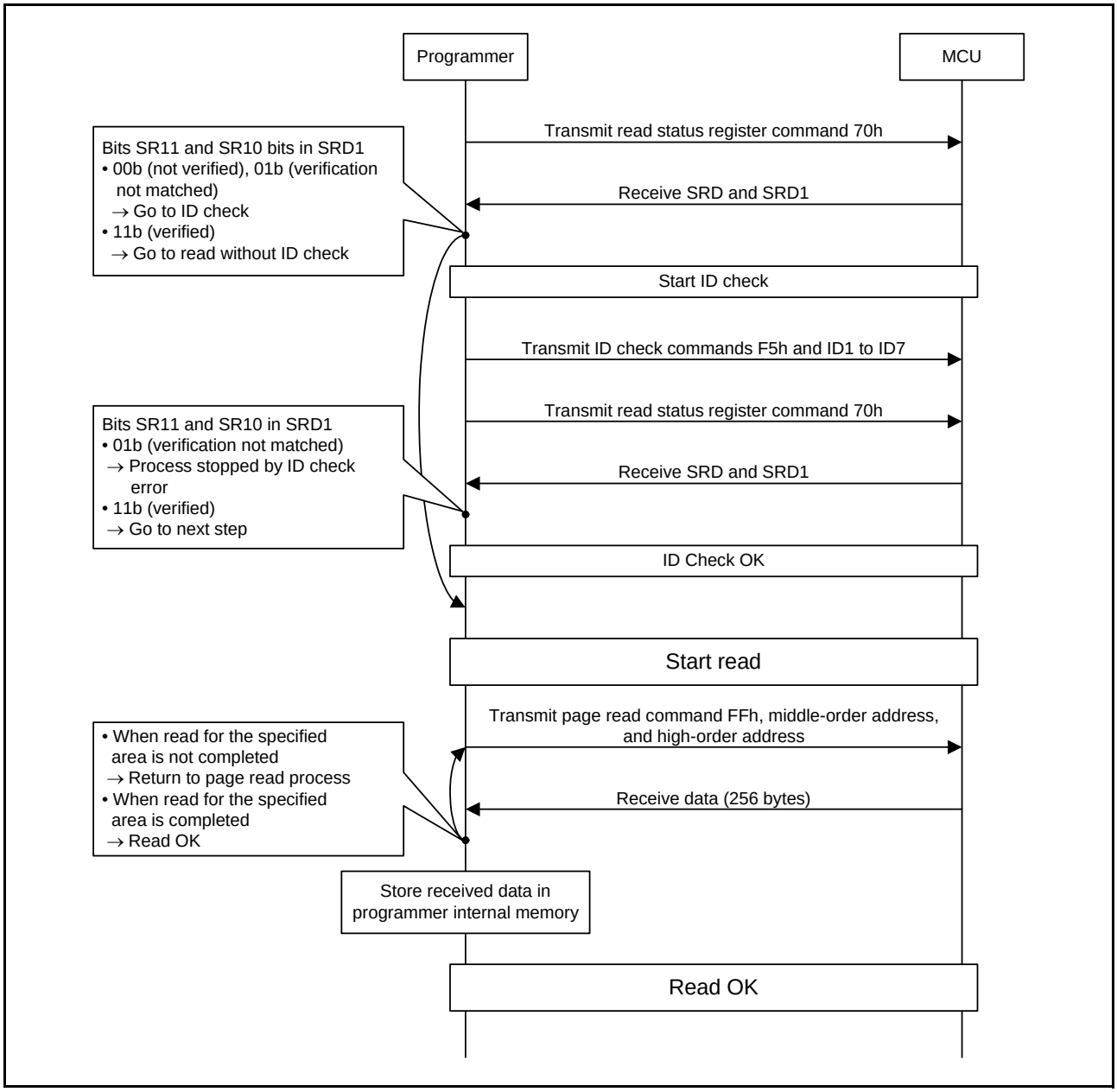
7.6 Verify

Data (program) in the specified area automatically or manually is read from the MCU's on-chip flash memory. The programmer compares the read data with the memory data (program) in the programmer to confirm that they match.



7.7 Read

This function allows reading the data (program) in the automatically or manually specified area from the MCU with on-chip flash memory.
The programmer stores the read data in its internal memory



8. Sample Programming Code

A sample program can be downloaded from the Renesas Technology website.
To download, click “Application Notes” in the left-hand side menu on the R8C/35A Group page.

9. Reference Documents

Hardware Manual
R8C/35A Group Hardware Manual Rev.0.40
The latest version can be downloaded from the Renesas Technology website.

Technical News/Technical Update
The latest information can be downloaded from the Renesas Technology website.

Website and Support

Renesas Technology website
http://www.renesas.com/

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REVISION HISTORY	R8C/35A Group Clock Synchronous Serial Program Downloader

Rev.	Date	Description	
		Page	Summary
1.00	Dec 29, 2009	–	First Edition issued

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   (3) healthcare intervention (e.g., excision, administration of medication, etc.)
   (4) any other purposes that pose a direct threat to human life
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