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## R8C/33T Group

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### Note of the touch detection with the Watchdog Timer processing

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May 23 2013

#### Introduction

Touch panel microcomputer R8C/33T group builds hardware (SCU: sensor control unit) that perceives the contact of the human body by measuring the stray capacity generated between the touch electrode and the human body into.

In this application note, it explains notes when the touch detection is used together with the Watchdog Timer interrupt.

#### Target Device

R8C/33T group

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## 1. Non-maskable interrupt and Touch detecting

### 1.1 Outline

R8C/33T series have the touch detection circuit SCU (sensor control unit) and the DTC (data transfer controller) for transmitting the measurement data on RAM, and these are used for the measurement of touch.

Because DTC stops the data transfer by the interrupts of Watchdog Timer, overflow and the other non-maskable interrupts, the touch measurement may be stopped when the non-maskable interrupts is generated while measuring touch.

In this application note, it explains the method of continuing the touch detection even the non-maskable interrupts is generated while touch measurement.

### 1.2 Flow of SCU hang-up by non-maskable interrupt (Image)

Figure 1-1 shows flow of SCU hang-up by non-maskable interrupt.

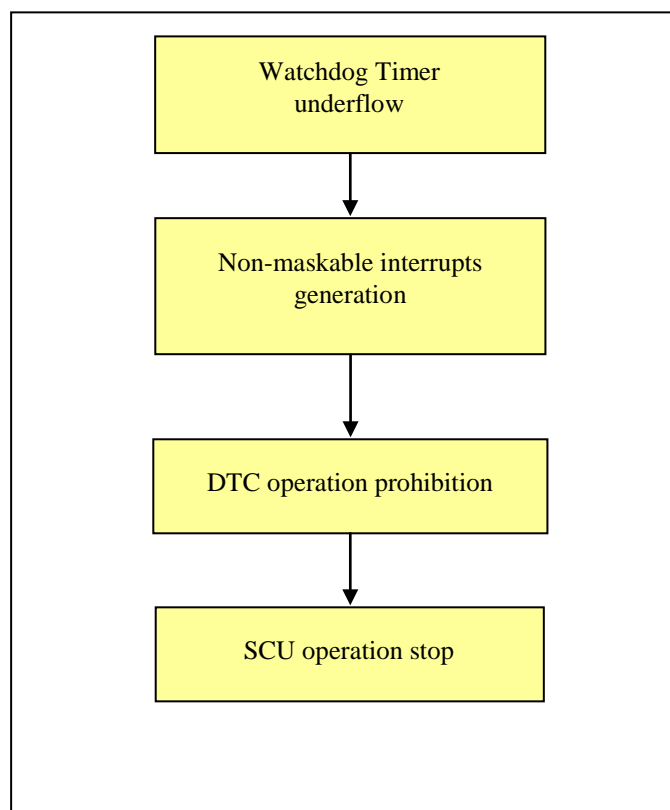


Figure 1-1 flow of SCU hang-up by non-maskable interrupt

### 1.3 Countermeasure

If the touch detects by SCU with non-maskable interrupts, it is necessary to do as follows;

- Just after the non-maskable interrupt is generated, the Non-maskable Interrupt generation Bit (NMIF) in DTC Activation Control Register (DTCTL) sets to '0'.
- The Watchdog Timer operation selects that it is to be able to select "Watchdog Timer reset" by it when the count source protection mode is invalid.

**2. Related register and it's operation**

**2.1 Specification of the Watchdog Timer**

- The operation when you select Count Source Protection Mode Disable and flowing under can select "Watchdog Timer interrupt" and "Watchdog Timer reset".
- "Watchdog Timer interrupt" is "Non-maskable interrupt ". (Refer to clause 2.4. )

Table 2-1 Watchdog Timer Specifications (Quotation from R8C/33T hardware manual)

Item	Count Source Protection Mode Disabled	Count Source Protection Mode Enabled
Count source	CPU clock	Low-speed on-chip oscillator clock for the watchdog timer
Count operation	Decrement	
Count start condition	Either of the following can be selected: • After a reset, count starts automatically. • Count starts by writing to the WDTS register.	
Count stop condition	Stop mode, wait mode	None
Watchdog timer initialization conditions	<ul style="list-style-type: none"> <li>• Reset</li> <li>• Write 00h and then FFh to the WDTR register (with acknowledgement period setting). (1)</li> <li>• Underflow</li> </ul>	
Operations at underflow	Watchdog timer interrupt or watchdog timer reset	Watchdog timer reset
Selectable functions	<ul style="list-style-type: none"> <li>• Division ratio of the prescaler Selected by the WDTC7 bit in the WDTC register.</li> <li>• Count source protection mode Whether count source protection mode is enabled or disabled after a reset can be selected by the CSPROINI bit in the OFS register (flash memory). If count source protection mode is disabled after a reset, it can be enabled or disabled by the CSPRO bit in the CSPR register (program).</li> <li>• Start or stop of the watchdog timer after a reset Selected by the WDTON bit in the OFS register (flash memory).</li> <li>• Initial value of the watchdog timer Selectable by bits WDTUFS0 and WDTUFS1 in the OFS2 register.</li> <li>• Refresh acknowledgement period for the watchdog timer Selectable by bits WDTRCS0 and WDTRCS1 in the OFS2 register.</li> </ul>	

## 2.2 The specification of DTC

Table 2-2 shows the DTC Activation Control Register. When the non-maskable interrupt is generated, NMIF bit sets to '1' and DTC is stopped. It is possible that NMIF bit set '0' by the user firmware.

Table 2-2 DTC Activation Control Register (Quotation from R8C/33T hardware manual)

**15.2.8 DTC Activation Control Register (DTCTL)**

Address 0080h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	NMIF	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bit	Set to 0.	R/W
b1	NMIF	Non-maskable interrupt generation bit (1)	0: Non-maskable interrupts not generated 1: Non-maskable interrupts generated	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Note:

- This bit is set to 0 when the read result is 1 and 0 is written to the same bit. This bit remains unchanged even if the read result is 0 and 0 is written to the same bit. This bit remains unchanged if 1 is written to it.

The DTCTL register controls DTC activation when a non-maskable interrupt (an interrupt by the watchdog timer, oscillation stop detection, voltage monitor 1, or voltage monitor 2) is generated.

### NMIF Bit (Non-Maskable Interrupt Generation Bit)

The NMIF bit is set to 1 when a watchdog timer interrupt, an oscillation stop detection interrupt, a voltage monitor 1 interrupt, or a voltage monitor 2 interrupt is generated.

When the NMIF bit is 1, the DTC is not activated even if the interrupt which enables DTC activation is generated. If the NMIF bit is changed to 1 during DTC transfer, the transfer is continued until it is completed.

When an interrupt source is the watchdog timer, wait for the following cycles before writing 0 to the NMIF bit:  
 If the WDTC7 bit in the WDTC register is set to 0 (divide-by-16 using the prescaler), wait for 16 cycles of the CPU clock after the interrupt source is generated.  
 If the WDTC7 bit is set to 1 (divide-by-128 using the prescaler), wait for 128 cycles of the CPU clock after the interrupt source is generated.

When an interrupt source is oscillation stop detection, set to the OCD1 bit in the OCD register to 0 (oscillation stop detection interrupt disabled) before writing 0 to the NMIF bit.

### 2.3 Relation of measurement by SCU and DTC data transfer

Table 2-3 shows Data destruction protect function. SCU scans automatically all CH, but it can not scan next CH without finishing recent data transfer by DTC. Because if SCU starts measurement before the register data transfers to RAM by DTC, the register data will be clear and the fail data will transfer to RAM.

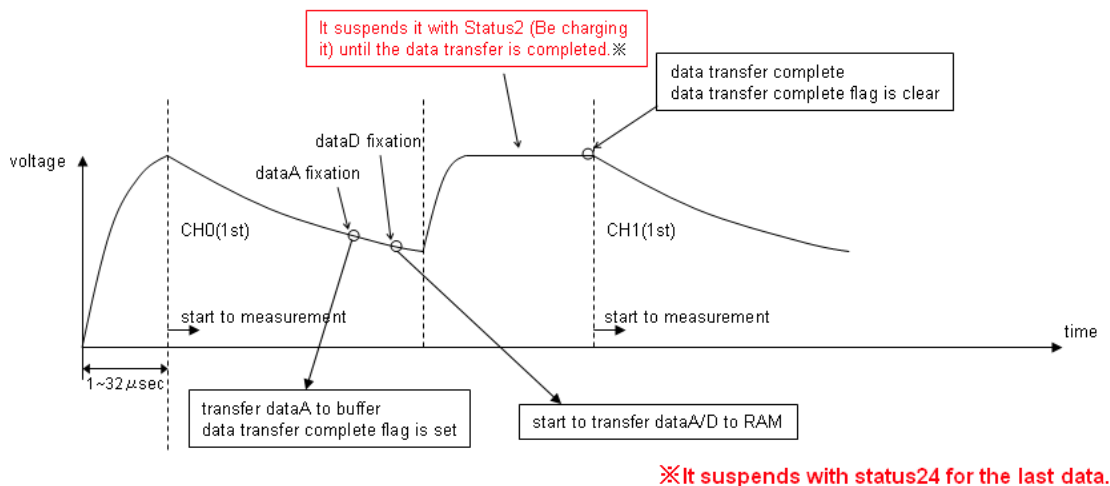
Table 2-3 Data destruction protect function (Quotation from R8C/33T professional manual)

#### Data destruction protect function

Short cycle from data D fixation to a primary counter value clearness (status3) is seven of the SCU operation clocks cycle. (When a section 1uSec.)  
 ⇒The following measurement starts before completing the data transfer to RAM, and there is a possibility that the primary counter value (value of dataD) is cleared.

<Data destruction prevention measures>

- It suspends in the state of status2 (Be charging it) when the data transfer to RAM is not completed and the forwarding completion is waited for.  
 =charge time is CPU cycle(20~30cycle). These cycle is the number of DTC Execution Cycles.
- After forwarding is completed (The transfer completion flag is cleared), the measurement is restarted.



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## Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	May 23 2013	—	Numbering change(Content is as same as R01AN0344EJ0100)

## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

### 1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

### 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

### 3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

### 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

### 5. Differences between Products

Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.



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