RX130 Group, RX230/RX231 Group

Points of Difference Between RX130 Group and RX230/RX231 Group

Introduction

This application note is intended as a reference for confirming the points of difference between the overview of functions, the I/O registers, the pin functions of the RX130 Group and RX230/RX231 Group, and notes on migration.

- 100-pin, 64-pin, and 48-pin packages

The RX231 Group is available in three chip versions: A, B, and C. The differences between these three versions are summarized below.

Peripheral Module	Chip Version A	Chip Version B	Chip Version C
CAN module (RSCAN)	Yes	Yes	No
SD host interface (SDHIa)	No	Yes*1	No
Security functions	No	Yes	No

Note 1. No 48-pin package available.

Unless specifically otherwise noted, the information in this application note applies to the 100 pin LFQFP package version of the RX130 Group, the 100 pin LFQFP package version of the RX230 Group, the 100 pin LFQFP package version and chip version B of the RX231 Group.To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the user's manuals of the products in question.

Target Device

RX130 Group, RX231 Group, and RX230 Group.

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Comparison of Functions of RX130 Group and RX230/RX231 Group

A comparison of the functions of the RX130 Group and RX230/RX231 Group is provided below. For details of the functions, see 2, Comparative Overview of Functions, and 5, Reference Documents.

Table 1.1 is a comparative listing of the functions of the RX130 and RX230/RX231.

Table 1.1 Comparison of Functions of RX130, RX230, and RX231

Module or Function Name	RX230	RX231	RX130
CPU	△	△	△
Operating Modes	△	△	△
Address Space	△	△	△
Resets	△	△	△
Option-setting memory	△	△	△
Voltage detection circuit (LVDAb)	△	△	△
Clock generation circuit	△	△	△
Clock frequency accuracy measurement circuit (CAC)	○	○	○
Low power consumption	△	△	△
Battery backup function	○	○	×
Register write protection function	△	△	△
Exception Handling	△	△	△
Interrupt controller (ICUb)	△	△	△
Buses	△	△	△
Memory protection unit (MPU)	○	○	×
DMA controller (DMACA)	○	○	×
Data transfer controller (DTCa)	○	○	○
Event link controller (ELC)	△	△	△
I/O ports	△	△	△
Multi-function pin controller (MPC)	△	△	△
Multi-function timer pulse unit 2 (MTU2a)	○	○	○
Port output enable 2 (POE2a)	△	△	△
16-bit timer pulse unit (TPUa)	○	○	×
8-Bit Timer	△	△	△
Compare match timer (CMT)	△	△	△
Realtime clock (RTCe) :RX230/RX231, (RTCc) :RX130	△	△	△
Low-power timer (LPT)	○	○	○
Watchdog timer (WDTA)	○	○	×
Independent Watchdog Timer (IWDTa)	△	△	△
USB 2.0 host/function module (USBd)	×	○	×
Serial communications interface (SCIg, SCIh)	○	○	○
Remote control receiver function (REMC)	×	×	○ 100-pin only
IrDA interface	○	○	×
I^2C bus interface (RIICa)	○	○	○
CAN module (RSCAN)	×	○	×
Serial sound interface (SSI)	○	○	×
Serial peripheral interface (RSPIa)	△	△	△
CRC calculator (CRC)	○	○	○
SD host interface (SDHIa)	×	○	×
Security functions	×	○	×

Module or Function Name	RX230	RX231	RX130
Capacitive touch sensing unit (CTSU) :RX230/RX231, (CTSUa) :RX130	△	△	△
12-bit A/D converter (S12ADE)	△	△	△
12-bit D/A converter (R12DAA):RX230/RX231 D/A converter (DAa):RX130	△	△	△
Temperature sensor (TEMPSA)	○	○	○
Comparator B (CMPBa)	△	△	△
Data operation circuit (DOC)	○	○	○
RAM	△	△	△
Flash Memory (ROM)	△	△	△
Flash Memory (E2 DataFlash)	○	○	○
Package (LQFP100 / 64 / 48)	○	○	○

Note: ○: Function implemented, ×: Function not implemented, △: Differences exist between implementation of function on RX230/RX231 and RX130.

2. Comparative Overview of Functions

This section lists points of difference between the peripheral functions of the RX130 and RX230/RX231 groups, comparing each function in overview and the registers of each function. Specifications implemented only on one Group are shown in red, specifications that exist on both groups but with points of difference are shown in red, and specifications that exist on both groups are shown in black.

2.1 CPU

Table 2.1 shows a Comparative Listing of CPU Specifications, and Table 2.2 shows a Comparative Listing of CPU Registers.

Table 2.1 Comparative Listing of CPU Specifications

Item	RX230/RX231	RX130
CPU	• Maximum operating frequency: 54 MHz • 32-bit RX CPU (RX v2) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4-Gbyte linear • Register set General purpose: Sixteen 32-bit registers Control: Ten 32-bit registers Accumulator: Two 72-bit registers • Basic instructions: 75 (variable-length instruction format) • Floating-point instructions: 11 • DSP instructions: 23 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32-bit × 32-bit → 64-bit • On-chip divider: 32-bit ÷ 32-bit → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)	• Maximum operating frequency: 32 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per clock cycle • Address space: 4-Gbyte linear • Register set General purpose: Sixteen 32-bit registers Control: Eight 32-bit registers Accumulator: One 64-bit registers • Basic instructions: 73 (variable-length instruction format) • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32-bit × 32-bit → 64-bit • On-chip divider: 32-bit ÷ 32-bit → 32 bits • Barrel shifter: 32 bits
FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard	—

Table 2.2 Comparative Listing of CPU Registers

Item	RX230/RX231	RX130
EXTB	Exception Table Register	—
FPSW	Floating-Point Status Word	—
ACC	ACC0: 72-bit register (DSP, multiply, and multiply-and-accumulate instruction) ACC1: 72-bit register (DSP)	ACC: 64-bit register (DSP, multiply, and multiply-and-accumulate instructions)

2.2 Operating Modes

Table 2.3 shows a comparative listing of the operating modes specifications, and Table 2.4 shows a comparative listing of the operating modes registers.

Table 2.3 Comparative Listing of Operating Modes Specifications

Item	RX230/RX231	RX130
Operating mode	Single-chip mode	Single-chip mode
	Boot mode (SCI interface)	Boot mode (SCI interface)
	Boot mode (USB interface)*1	—
Mode pins	MD, UB	MD

Note 1. Implemented on the RX231 Group only. Not implemented on the RX230 Group.

Table 2.4 Comparative Listing of Operating Mode Registers

Register	Bit	RX230/RX231	RX130
SYSCR0	—	System control register 0	—

2.3 Address Space

Figure 2.1 shows the memory map.

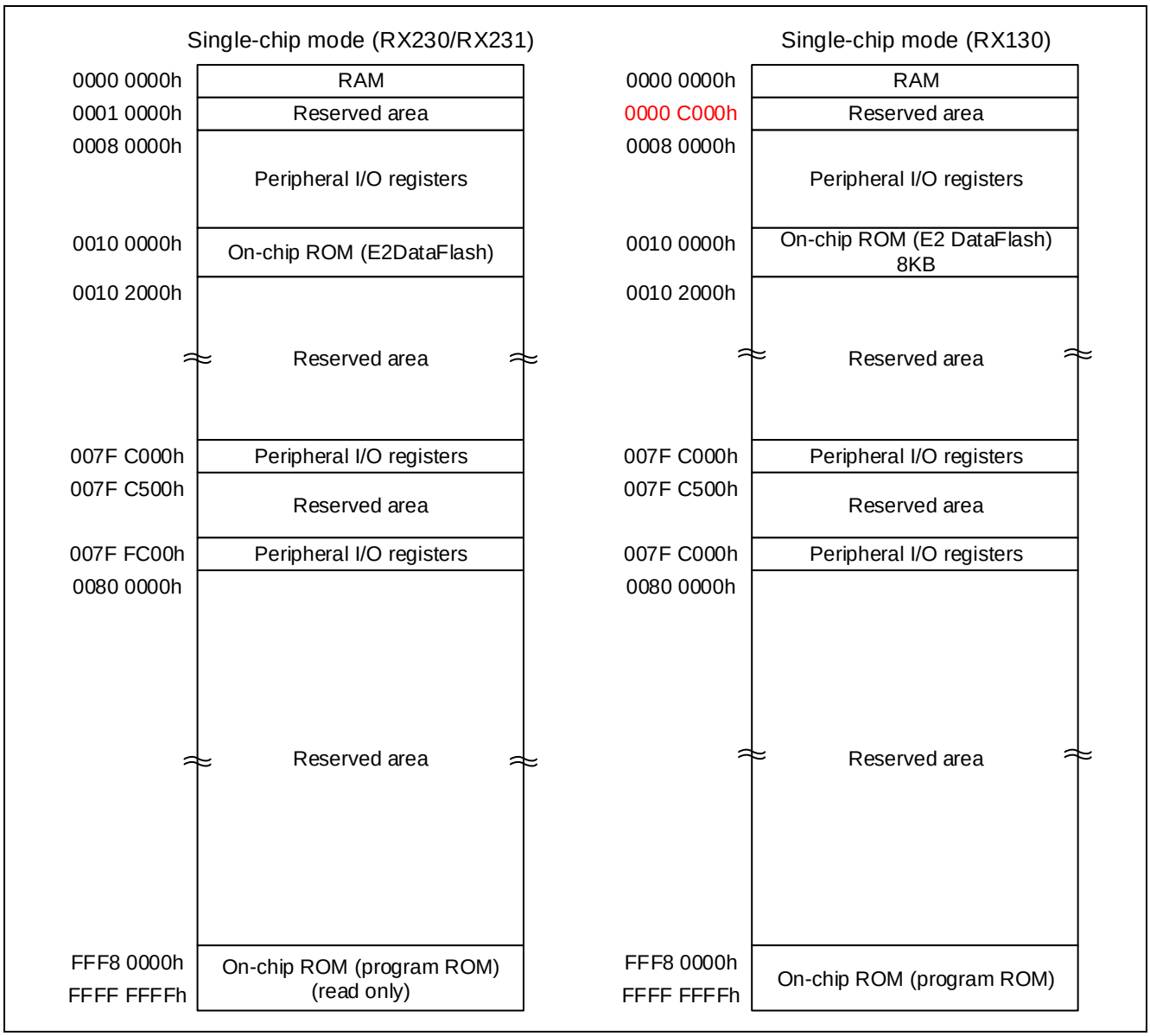

Figure 2.1 Memory Map (Single-chip mode)

2.4 Resets

Table 2.5 shows a comparative listing of the reset specifications, and Table 2.6 shows a comparative listing of the reset registers.

Table 2.5 Comparative Listing of Reset Specifications

Reset Name	RX230/RX231	RX130
Name of reset	RES# pin reset	RES# pin reset
	Power-on reset	Power-on reset
	Voltage monitoring 0 reset	Voltage monitoring 0 reset
	Voltage monitoring 1 reset	Voltage monitoring 1 reset
	Voltage monitoring 2 reset	Voltage monitoring 2 reset
	Independent watchdog timer reset	Independent watchdog timer reset
	Watchdog timer reset	—
	Software reset	Software reset

Table 2.6 Comparative Listing of Reset Registers

Register	Bit	RX230/RX231	RX130
RSTSR2	WDTRF	Watchdog timer reset detection flag	—

2.5 Option-Setting Memory

Table 2.7 shows a comparative listing of the option-setting memory registers, and Figure 2.2 shows a comparative of the option-setting memory.

Table 2.7 Comparative Listing of Option-Setting Memory Registers

Register	Bit	RX230/RX231	RX130
OFS0	WDTSTRT	WDT start mode select bit	—
	WDTTOPS[1:0]	WDT timeout period select bits	—
	WDTCKS[3:0]	WDT clock frequency division ratio select bits	—
	WDTRPES[1:0]	WDT window end position select bits	—
	WDTRPSS[1:0]	WDT window start position select bits	—
	WDTRSTIRQS	WDT reset interrupt request select bit	—

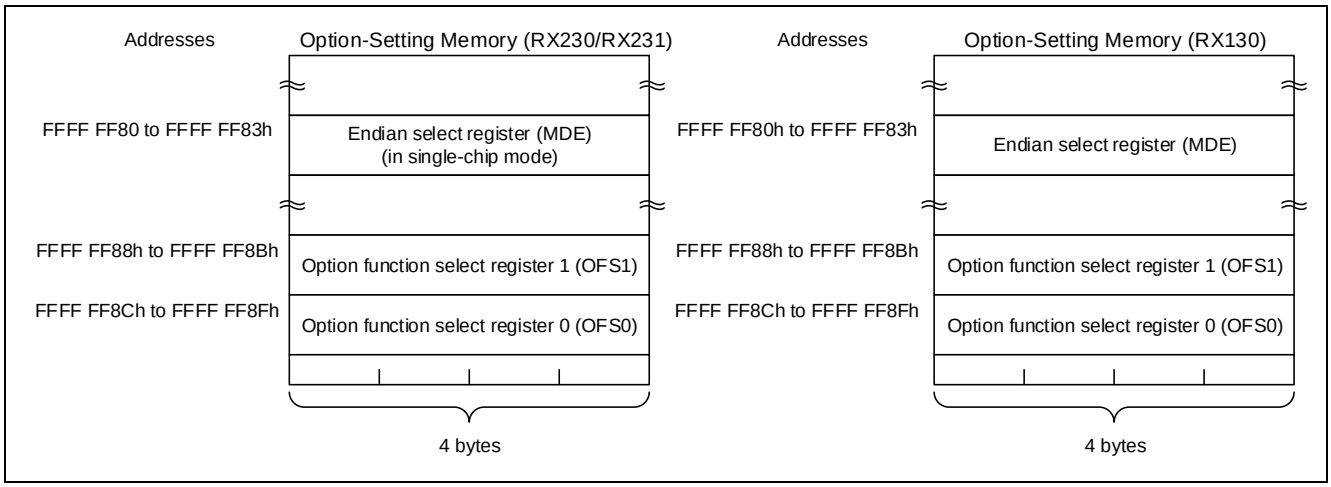

Figure 2.2 Comparative of Option-Setting Memory

2.6 Voltage Detection Circuit

Table 2.8 shows a comparative listing of the voltage detection circuit specifications.

Table 2.8 Comparative Listing of Voltage Detection Circuit Specifications

		RX230/RX231 (LVDAb)			RX130 (LVDAb)		
Item		**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	Voltage falls lower than Vdet0.	Voltage rises or falls past Vdet1.	Voltage rises or falls past Vdet2.	Voltage falls lower than Vdet0.	Voltage rises or falls past Vdet1.	Voltage rises or falls past Vdet2.
				The EXVCCINP2 bit in LVCMPCR can be used to select between VCC and the voltage input to the CMPA2 pin.			The EXVCCINP2 bit in LVCMPCR can be used to select between VCC and the voltage input to the CMPA2 pin.
	Detection voltage	Selectable from four levels using OFS1 register.	Selectable from 14 levels using LVDLVLR.LVD1LVL[3:0] bits	Selectable from four levels using LVDLVLR.LVD2LVL[1:0] bits	Selectable from four levels using OFS1 register.	Selectable from 14 levels using LVDLVLR.LVD1LVL[3:0] bits.	Selectable from four levels using LVDLVLR.LVD2LVL[1:0] bits.
	Monitor flag	—	LVD1SR.LVD1MON flag: Monitors if higher or lower than Vdet1.	LVD2SR.LVD2MON flag: Monitors if higher or lower than Vdet2.	—	LVD1SR.LVD1MON flag: Monitors if higher or lower than Vdet1.	LVD2SR.LVD2MON flag: Monitors if higher or lower than Vdet2.
			LVD1SR.LVD1DET flag: Detects rise or fall past Vdet1.	LVD2SR.LVD2DET flag: Detects rise or fall past Vdet2.		LVD1SR.LVD1DET flag: Detects rise or fall past Vdet1.	LVD2SR.LVD2DET flag: Detects rise or fall past Vdet2.
Voltage detection processing	Reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC: CPU operation restarts a fixed period of time after VCC > Vdet0.	Reset when Vdet1 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet1 and CPU operation restarts a fixed period of time after Vdet1 > VCC.	Reset when Vdet2 > VCC or CMPA2 pin voltage: Selectable between CPU operation restarts a fixed period of time after VCC or CMPA2 pin voltage > Vdet2 and CPU operation restarts a fixed period of time after Vdet2 > VCC or CMPA2 pin voltage.	Reset when Vdet0 > VCC: CPU operation restarts a fixed period of time after VCC > Vdet0.	Reset when Vdet1 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet1 and CPU operation restarts a fixed period of time after Vdet1 > VCC.	Reset when Vdet2 > VCC or CMPA2 pin voltage: Selectable between CPU operation restarts a fixed period of time after VCC or CMPA2 pin voltage > Vdet2 and CPU operation restarts a fixed period of time after Vdet2 > VCC or CMPA2 pin voltage.

Item		RX230/RX231 (LVDAb) Voltage Monitoring 0	RX230/RX231 (LVDAb) Voltage Monitoring 1	RX230/RX231 (LVDAb) Voltage Monitoring 2	RX130 (LVDAb) Voltage Monitoring 0	RX130 (LVDAb) Voltage Monitoring 1	RX130 (LVDAb) Voltage Monitoring 2
Voltage detection processing	Interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Selectable between non-maskable interrupt and interrupt.	Selectable between non-maskable interrupt and interrupt.		Selectable between non-maskable interrupt and interrupt.	Selectable between non-maskable interrupt and interrupt.
			Interrupt request generated both when Vdet1 > VCC and when VCC > Vdet1, or one or the other.	Interrupt request generated both when Vdet2 > VCC or CMPA2 pin voltage and when VCC or CMPA2 pin voltage > Vdet2, or one or the other.		Interrupt request generated both when Vdet1 > VCC and when VCC > Vdet1, or one or the other.	Interrupt request generated both when Vdet2 > VCC or CMPA2 pin voltage and when VCC or CMPA2 pin voltage > Vdet2, or one or the other.
Event link function		—	Available: Vdet1 pass-through detection event output	Available: Vdet2 pass-through detection event output	—	Available: Vdet1 pass-through detection event output	—

2.7 Clock Generation Circuit

Table 2.9 shows a comparative listing of the clock generation circuit specifications, and Table 2.10 shows a comparative listing of the clock generation circuit registers.

Table 2.9 Comparative Listing of Clock Generation Circuit Specifications

Item	RX230/RX231(LVDAb)	RX130(LVDAb)
Uses	• Generates the system clock (ICLK) supplied to the CPU, DMAC, DTC, ROM, and RAM. • Generates the peripheral module clocks (PCLKA, PCLKB, PCLKD) supplied to the peripheral module clocks. Peripheral module clock PCLKA is used as the operating clock for MTU2, peripheral module clock PCLKD is used as the operating clock for S12AD, and peripheral module clock PCLKB is used as the operating clock for the modules other than MTU2 and S12AD. • Generates the FlashIF clock (FCLK) supplied to the FlashIF. • Generates the external bus clock (BCLK) supplied to the external bus. • Generates the USB clock (UCLK) supplied to the USB.*1 • Generates the CAC clock (CACCLK) supplied to the CAC. • Generates the RTC-dedicated sub clock (RTCSCLK) supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) supplied to the IWDT. • Generates the CAN clock (CANCLK) supplied to the CAN.*1 • Generates the SSI clock (SSISCK) supplied to the SSI.*1 • Generates the LPT clock (LPTCLK) supplied to the LPT.	• Generates the system clock (ICLK) supplied to the CPU, DTC, ROM, and RAM. • Generates the peripheral module clocks (PCLKB, PCLKD) supplied to the peripheral module clocks. Peripheral module clock PCLKD is used as the operating clock for S12AD, and peripheral module clock PCLKB is used as the operating clock for the modules other than S12AD. • Generates the FlashIF clock (FCLK) supplied to the FlashIF. • Generates the CAC clock (CACCLK) supplied to the CAC. • Generates the RTC-dedicated sub clock (RTCSCLK) supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) supplied to the IWDT. • Generates the LPT clock (LPTCLK) supplied to the LPT. • Generates the REMC clock (REMCLK) supplied to the REMC.

Item	RX230/RX231(LVDAb)	RX130(LVDAb)
Operating frequencies	• ICLK: 54 MHz (max.) • PCLKA: 54 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 54 MHz (max.) • FCLK: 1 MHz to 32 MHz (for programming and erasing the ROM and E2 data flash) 32 MHz (max.): (for reading from the E2 data flash) • BCLK: 32 MHz (max.) • BCLK pin output: 16 MHz (max.) • UCLK: 48 MHz*1 • CACCLK: Same frequency as each oscillator • RTCSCLK: 32.768 kHz • IWDTCLK: 15 kHz • CANCLK: 20 MHz (max.)*1 • SSISCK: 20 MHz (max.)*1 • LPTCLK: Same as selected oscillator clock	• ICLK: 32 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 32 MHz (max.) • FCLK: 1 MHz to 32 MHz (for programming and erasing the ROM and E2 data flash) 32 MHz (max.): (for reading from the E2 data flash) • CACCLK: Same frequency as each oscillator • RTCSCLK: 32.768 kHz • IWDTCLK: 15 kHz • LTPCLK: Same as selected oscillator clock • REMCLK: Same frequency as each oscillator

Item	RX230/RX231(LVDAb)	RX130(LVDAb)
Main clock oscillator	• Resonator frequency: 1 MHz to 20 MHz (VCC ≥ 2.4 V) 1 MHz to 8 MHz (VCC < 2.4 V) • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop of the main clock is detected, the system clock source is switched to LOCO, and MTU output can be forcedly driven to high-impedance. • Drive capacity switching function	• Resonator frequency: 1 MHz to 20 MHz (VCC ≥ 2.4 V) 1 MHz to 8 MHz (VCC < 2.4 V) • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop of the main clock is detected, the system clock source is switched to LOCO, and MTU output can be forcedly driven to high-impedance. • Drive capacity switching function
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT • Drive capacity switching function	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT • Drive capacity switching function
PLL	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 12.5 MHz • Frequency multiplication ratio: Selectable within range from 4 to 13.5 (increments of 0.5) • Oscillation frequency: 24 MHz to 54 MHz (VCC ≥ 2.4 V)	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 8 MHz • Frequency multiplication ratio: Selectable within range from 4 to 8 (increments of 0.5) • Oscillation frequency: 24 MHz to 32 MHz (VCC ≥ 2.4 V)
USB-dedicated PLL circuit	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz, 6 MHz, 8 MHz, 12 MHz • Frequency multiplication ratio: Selectable within range from 4, 6, 8, 12 • Oscillation frequency: 48 MHz (VCC ≥ 2.4 V)	—
High-speed on-chip oscillator (HOCO)	Oscillation frequency: 32 MHz, 54 MHz	Oscillation frequency: 32 MHz
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 4 kHz	Oscillation frequency: 4 MHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 15 kHz	Oscillation frequency: 15 kHz

Note 1. Implemented on the RX231 Group only. Not implemented on the RX230 Group.

Table 2.10 Comparative Listing of Clock Generation Circuit Registers

Register	Bit	RX230/RX231	RX130
SCKCR	PCKA[3:0]	Peripheral module clock A (PCLKA) select bits Value after a reset is different.	—
	BCK[3:0]	External bus clock (BCLK) select bits Value after a reset is different.	—
	PSTOP1	BCLK pin output control bit	—
PLLCR	STC[5:0]	Frequency multiplication factor setting bits b13 b8 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 0 0 1 0 1 0: ×5.5 0 0 1 0 1 1: ×6 0 0 1 1 0 0: ×6.5 0 0 1 1 0 1: ×7 0 0 1 1 1 0: ×7.5 0 0 1 1 1 1: ×8 0 1 0 0 0 0: ×8.5 0 1 0 0 0 1: ×9 0 1 0 0 1 0: ×9.5 0 1 0 0 1 1: ×10 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12 0 1 1 0 0 0: ×12.5 0 1 1 0 0 1: ×13 0 1 1 0 1 0: ×13.5 Do not set to values other than the above.	Frequency multiplication factor setting bits b13 b8 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 0 0 1 0 1 0: ×5.5 0 0 1 0 1 1: ×6 0 0 1 1 0 0: ×6.5 0 0 1 1 0 1: ×7 0 0 1 1 1 0: ×7.5 0 0 1 1 1 1: ×8 Do not set to values other than the above.
UPLLCR	—	USB-dedicated PLL control register*1	—
UPLLCR2	—	USB-dedicated PLL control register 2*1	—
BCKCR	—	External bus clock control register	—
HOCOCR2	—	High-speed on-chip oscillator control register 2	—
OSCOVFSR	UPLOVF	USB-dedicated PLL clock oscillation stabilization flag*1	—
HOFCR	—	High-speed on-chip oscillator forced oscillation control register	—
MEMWAIT	—	Memory wait cycle setting register	—
HOCOTRRn	—	High-speed on-chip oscillator trimming register n (n = 0 or 3)	High-speed on-chip oscillator trimming register n (n = 0)

Note 1. Implemented on the RX231 Group only. Not implemented on the RX230 Group.

2.8 Low Power Consumption Functions

Table 2.11 shows a comparative listing of the low power consumption specifications, Table 2.12 to Table 2.14 shows a Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode, and Table 2.15 shows a comparative listing of the low power consumption function registers.

Table 2.11 Comparative Listing of Low Power Consumption Functions Specifications

Item	RX230/RX231	RX130
Reduction of power consumption by clock switching	The frequency division ratio can be set independently for the system clock (ICLK), high-speed peripheral module clock (PCLKA), peripheral module clock (PCLKB), S12AD clock (PCLKD), external bus clock (BCLK), FlashIF clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).
Module stop function	Each peripheral module can be stopped independently.	Each peripheral module can be stopped independently.
Function for transition to low power consumption mode	It is possible to transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped.	It is possible to transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped.
Low power consumption modes	• Sleep mode • Deep sleep mode • Software standby mode	• Sleep mode • Deep sleep mode • Software standby mode
Operating power reduction function	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage. • Operating power control modes: 3 — High-speed operating mode — Middle-speed operating mode — Low-speed operating mode	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage. • Operating power control modes: 3 — High-speed operating mode — Middle-speed operating mode — Low-speed operating mode

Table 2.12 Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (Sleep Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX230/RX231	RX130
	Sleep Mode	Sleep Mode
Entry trigger	Control register + instruction	Control register + instruction
Exit trigger	Interrupt	Interrupt
After exiting from each mode, CPU begins from	Interrupt handling	Interrupt handling
Main clock oscillator	Operating possible	Operating possible
Sub-clock oscillator	Operating possible	Operating possible
High-speed on-chip oscillator	Operating possible	Operating possible
Low-speed on-chip oscillator	Operating possible	Operating possible
IWDT-dedicated on-chip oscillator	Operating possible	Operating possible
PLL	Operating possible	Operating possible
USB-dedicated PLL	Operating possible	—
CPU	Stopped (Retained)	Stopped (Retained)
RAM (0000 0000h to 0000 FFFFh)	Operating possible (Retained)	—
RAM0 (0000 0000h to 0000 BFFFh)	—	Operating possible (Retained)
DMAC	Operating possible	—
DTC	Operating possible	Operating possible
Flash memory	Operating	Operating
Watchdog timer (WDT)	Stopped (Retained)	—
Independent watchdog timer (IWDT)	Operating possible	Operating possible
Remote control signal receiver (REMC)	—	Operating possible
Realtime clock (RTC)	Operating possible	Operating possible
Low power timer (LPT)	Operating possible	Operating possible
Voltage detection circuit (LVD)	Operating possible	Operating possible
Power-on reset circuit	Operating	Operating
Peripheral modules	Operating possible	Operating possible
I/O ports	Operating	Operating
RTCOUT	Operating possible	Operating possible
CLKOUT	Operating possible	Operating possible
Comparator B	Operating possible	Operating possible

Table 2.13 Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (Deep Sleep Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX230/RX231	RX130
	Deep Sleep Mode	Deep Sleep Mode
Entry trigger	Control register + instruction	Control register + instruction
Exit trigger	Interrupt	Interrupt
After exiting from each mode, CPU begins from	Interrupt handling	Interrupt handling
Main clock oscillator	Operating possible	Operating possible
Sub-clock oscillator	Operating possible	Operating possible
High-speed on-chip oscillator	Operating possible	Operating possible
Low-speed on-chip oscillator	Operating possible	Operating possible
IWDT-dedicated on-chip oscillator	Operating possible	Operating possible
PLL	Operating possible	Operating possible
USB-dedicated PLL	Operating possible	—
CPU	Stopped (Retained)	Stopped (Retained)
RAM (0000 0000h to 0000 FFFFh)	Stopped (Retained)	—
RAM0 (0000 0000h to 0000 BFFFh)	—	Stopped (Retained)
DMAC	Stopped (Retained)	—
DTC	Stopped (Retained)	Stopped (Retained)
Flash memory	Stopped (Retained)	Stopped (Retained)
Watchdog timer (WDT)	Stopped (Retained)	—
Independent watchdog timer (IWDT)	Operating possible	Operating possible
Remote control signal receiver (REMC)	—	Operating possible
Realtime clock (RTC)	Operating possible	Operating possible
Low power timer (LPT)	Operating possible	Operating possible
Voltage detection circuit (LVD)	Operating possible	Operating possible
Power-on reset circuit	Operating	Operating
Peripheral modules	Operating possible	Operating possible
I/O ports	Operating	Operating
RTCOUT	Operating possible	Operating possible
CLKOUT	Operating possible	Operating possible
Comparator B	Operating possible	Operating possible

Table 2.14 Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (Software Standby Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX230/RX231	RX130
	Software Standby Mode	Software Standby Mode
Entry trigger	Control register + instruction	Control register + instruction
Exit trigger	Interrupt	Interrupt
After exiting from each mode, CPU begins from	Interrupt handling	Interrupt handling
Main clock oscillator	Stopped	Stopped
Sub-clock oscillator	Operating possible	Operating possible
High-speed on-chip oscillator	Stopped	Operating possible
Low-speed on-chip oscillator	Stopped	Stopped
IWDT-dedicated on-chip oscillator	Operating possible	Operating possible
PLL	Stopped	Stopped
USB-dedicated PLL	Stopped	—
CPU	Stopped (Retained)	Stopped (Retained)
RAM (0000 0000h to 0000 FFFFh)	Stopped (Retained)	—
RAM0 (0000 0000h to 0000 BFFFh)	—	Stopped (Retained)
DMAC	Stopped (Retained)	—
DTC	Stopped (Retained)	Stopped (Retained)
Flash memory	Stopped (Retained)	Stopped (Retained)
Watchdog timer (WDT)	Stopped (Retained)	—
Independent watchdog timer (IWDT)	Operating possible	Operating possible
Remote control signal receiver (REMC)	—	Operating possible
Realtime clock (RTC)	Operating possible	Operating possible
Low power timer (LPT)	Operating possible	Operating possible
Voltage detection circuit (LVD)	Operating possible	Operating possible
Power-on reset circuit	Operating	Operating
Peripheral modules	Stopped (Retained)	Stopped (Retained)
I/O ports	Retained	Retained
RTCOUT	Operating possible	Operating possible
CLKOUT	Operating possible	Operating possible
Comparator B	Operating possible	Operating possible

Table 2.15 Comparative Listing of Low Power Consumption Function Registers

Register	Bit	RX230/RX231	RX130
SBYCR	OPE	Output port enable Value after a reset is different.	—
MSTPCRA	MSTPA9	Multi-function timer pulse unit 2 module stop bit	Multi-function timer pulse unit module stop bit
	MSTPA13	16-bit timer pulse unit 0 (unit 0) module stop bit	—
	MSTPA14	Compare match timer 1 (unit 1) module stop bit	—
	MSTPA19	12-bit D/A converter module stop bit	D/A converter module stop bit
	MSTPA28	DMA controller/data transfer controller module stop bit	Data transfer controller module stop bit
MSTPCRB	MSTPB0	RCAN0 module stop bit*1	—
	MSTPB4	Serial Communication Interface SCIh Module Stop	Serial Communication Interface SCIf Module Stop
	MSTPB10	Comparator B Module Stop	Comparator Module Stop
	MSTPB19	USB0 module stop bit*1	—
MSTPCRC	MSTPC20	IrDA module stop bit	—
	MSTPC28	—	Remote control receive 1 module stop setting bit
	MSTPC29	—	Remote control receive 0 module stop setting bit
MSTPCRD	MSTPD15	Serial sound interface module stop bit	—
	MSTPD19	SD host interface (SDHI) module stop bit*1	—
	MSTPD31	Trusted Secure IP Function Module Stop*1	—

Note 1. Implemented on the RX231 Group only. Not implemented on the RX230 Group.

2.9 Register Write Protection Function

Table 2.16 shows a comparative overview of the register write protection function specifications.

Table 2.16 Comparative Overview of Register Write Protection Function Specifications

Item	RX230/RX231	RX130
PRCR0 bit	Registers related to the clock generation circuit SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, CKOCR, UPLLCR*1, UPLLCR2*1, BCKCR, HOCOCR2, MEMWAIT, LOCOTRR, ILOCOTRR, HOCOTRR0, HOCOTRR3	Registers related to the clock generation circuit SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOFCR, OSTDCR, OSTDSR, CKOCR, LOCOTRR, ILOCOTRR, HOCOTRR0
PRCR1 bit	• Registers related to the operating modes SYSCR0, SYSCR1 • Registers related to the low power consumption functions SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, SOPCCR • Registers related to the clock generation circuit MOFCR, MOSCWTCR • Software reset register SWRR	• Registers related to the operating modes SYSCR1 • Registers related to the low power consumption functions SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, SOPCCR • Registers related to the clock generation circuit MOFCR, MOSCWTCR • Software reset register SWRR
PRCR2 bit	Registers related to the low power timer LPTCR1, LPTCR2, LPTCR3, LPTPRD, LPCMR0, LPWUCR	Registers related to the low power timer LPTCR1, LPTCR2, LPTCR3, LPTPRD, LPCMR0, LPWUCR
PRCR3 bit	• Registers related to the LVD LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR • Registers related to the battery backup function VBATTCR, VBATTSR, VBTLVDICR	• Registers related to the LVD LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

Note 1. Implemented on the RX231 Group only. Not implemented on the RX230 Group.

2.10 Exception Handling

Table 2.17 shows a Comparative Listing of Vector, and Table 2.18 shows a Comparative Listing of Return from Exception Handling Routine.

Table 2.17 Comparative Listing of Vector

Exception		RX230/RX231	RX130
Undefined instruction exception		Exception vector table (EXTB)	Fixed vector table
Privileged instruction exception		Exception vector table (EXTB)	Fixed vector table
Access exception		Exception vector table (EXTB)	—
Floating-point exception		Exception vector table (EXTB)	—
Reset		Exception vector table (EXTB)	Fixed vector table
Non-maskable interrupt		Exception vector table (EXTB)	Fixed vector table
Interrupt	Fast interrupt	FINTV	FINTV
	Other than above	Interrupt vector table (INTB)	Relocatable vector table (INTB)
Unconditional trap		Interrupt vector table (INTB)	Relocatable vector table (INTB)

Table 2.18 Comparative Listing of Return from Exception Handling Routine

Exception		RX230/RX231	RX130
Undefined instruction exception		RTE	RTE
Privileged instruction exception		RTE	RTE
Access exception		RTE	—
Floating-point exception		RTE	—
Reset		Return is impossible	Return is impossible
Non-maskable interrupt		Prohibited	Return is impossible
Interrupt	Fast interrupt	RTFI	RTFI
	Other than above	RTE	RTE
Unconditional trap		RTE	RTE

2.11 Interrupt Controller

Table 2.19 shows a comparative listing of the interrupt controller specifications, and Table 2.20 shows a comparative listing of the interrupt controller registers.

Table 2.19 Comparative Listing of Interrupt Controller Specifications

Item		RX230/RX231 (ICUb)	RX130 (ICUb)
Interrupt	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection The detection method is fixed for each source of connected peripheral modules.	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection The detection method is fixed for each source of connected peripheral modules.
	External pin interrupts	• Interrupts from pins IRQ0 to IRQ7 • Sources: 8 • Interrupt detection: One detection method among low level, falling edge, rising edge, and rising and falling edges can be set for each source. • Digital filter function: Supported	• Interrupts from pins IRQ0 to IRQ7 • Sources: 8 • Interrupt detection: One detection method among low level, falling edge, rising edge, and rising and falling edges can be set for each source. • Digital filter function: Supported
	Software interrupt	• Interrupt generated by writing to a register. • Source: 1	• Interrupt generated by writing to a register. • Source: 1
	Event link interrupt	The ELSR8I, ELSR18I, or ELSR19I interrupt is generated by an ELC event.	The ELSR8I or ELSR18I interrupt is generated by an ELC event.
	Interrupt priority level	Priority is specified by register settings.	Priority is specified by register settings.
	Fast interrupt function	Faster interrupt processing by the CPU can be specified only for a single interrupt source.	Faster interrupt processing by the CPU can be specified only for a single interrupt source.
	DTC and DMAC control	The DTC and DMAC can be activated by interrupt sources.	The DTC can be activated by interrupt sources.
Non-maskable interrupts	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: Supported	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: Supported
	Oscillation stop detection interrupt	Interrupt at oscillation stop detection	Interrupt at oscillation stop detection
	WDT underflow/refresh error	Interrupt at an underflow of the down counter or at the occurrence of a refresh error	—
	IWDT underflow/refresh error	Interrupt at an underflow of the down counter or at the occurrence of a refresh error	Interrupt at an underflow of the down counter or at the occurrence of a refresh error
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)

Item		RX230/RX231 (ICUb)	RX130 (ICUb)
Non-maskable interrupts	VBATT voltage monitoring interrupt	VBATT voltage monitoring interrupt	—
Return from low power consumption modes		• Sleep mode and deep sleep mode: Return is initiated by a non-maskable interrupt or any other interrupt source. • Software standby mode: Return is initiated by a non-maskable interrupt, interrupt IRQ0 to IRQ7, or RTC alarm/period interrupt.	• Sleep mode and deep sleep mode: Return is initiated by a non-maskable interrupt or any other interrupt source. • Software standby mode: Return is initiated by a non-maskable interrupt, interrupt IRQ0 to IRQ7, or RTC alarm/period interrupt.

Table 2.20 Comparative Listing of Interrupt Controller Registers

Register	Bit	RX230/RX231 (ICUb)	RX130 (ICUb)
DTCERn	DTCE	DTC Transfer Request Enable 0: The corresponding interrupt source is selected as the CPU or DMAC trigger. 1: The corresponding interrupt source is selected as the DTC trigger.	DTC Transfer Request Enable 0: The corresponding interrupt source is selected as the CPU trigger. 1: The corresponding interrupt source is selected as the DTC trigger.
DMRSRm	—	DMAC activation request select register m (m = DMAC channel number)	—
NMISR	WDTST	WDT underflow/refresh error status flag	—
	VBATST	VBATT voltage monitoring interrupt status flag	—
NMIER	WDTEN	WDT underflow/refresh error enable bit	—
	VBATEN	VBATT voltage monitoring interrupt enable bit	—
NMICLR	WDTCLR	WDT clear bit	—
	VBATCLR	VBAT clear bit	—

2.12 Bus

Table 2.21 shows a comparative listing of the bus specifications, and Table 2.22 shows a comparative listing of the bus registers.

Table 2.21 Comparative Listing of Bus Specifications

Item		RX230/RX231	RX130
CPU bus	Instruction bus	• Connected to the CPU (for instructions). • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).	• Connected to the CPU (for instructions). • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).
	Operand bus	• Connected to the CPU (for operand). • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).	• Connected to the CPU (for operand). • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).
Memory buses	Memory bus 1	Connected to the RAM.	Connected to the RAM.
	Memory bus 2	Connected to the ROM.	Connected to the ROM.
Internal main buses	Internal main bus 1	• Connected to the CPU. • Operates in synchronization with the system clock (ICLK).	• Connected to the CPU. • Operates in synchronization with the system clock (ICLK).
	Internal main bus 2	• Connected to the DTC and DMAC. • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).	• Connected to the DTC. • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section). • Operates in synchronization with the system clock (ICLK).	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section). • Operates in synchronization with the system clock (ICLK).
	Internal peripheral bus 2	• Connected to peripheral modules (modules other than those connected to internal peripheral bus 1, 3, 4). • Operates in synchronization with the peripheral module clock (PCLKB).	• Connected to peripheral modules. • Operates in synchronization with the peripheral module clock (PCLKB, PCLKD).
	Internal peripheral bus 3	• Connected to peripheral modules (USB0[*1], RSCAN[*1], CTSU). • Operates in synchronization with the peripheral module clock (PCLKB).	• Connected to peripheral modules (Touch). • Operates in synchronization with the peripheral module clock (PCLKB).
	Internal peripheral bus 4	• Connected to peripheral modules MTU2. • Operates in synchronization with the peripheral module clock (PCLKA).	—

Item		RX230/RX231	RX130
Internal peripheral buses	Internal peripheral bus 6	• Connected to the flash control module and E2 data flash • Operates in synchronization with the FlashIF clock (FCLK).	• Connected to the ROM (P/E) and E2 data flash memory. • Operates in synchronization with the FlashIF clock (FCLK).
External bus	CS area	• Connected to the external device. • Operates in synchronization with the external clock (BCLK).	—

Note 1. Implemented on the RX231 Group only. Not implemented on the RX230 Group.

Table 2.22 Comparative Listing of Bus Registers

Register	Bit	RX230/RX231	RX130
CSnCR	—	CSn control register (n = 0 to 3)	—
CSnREC	—	CSn recovery cycle register (n = 0 to 3)	—
CSRECEN	—	CS recovery cycle insertion enable register	—
CSnMOD	—	CSn mode register (n = 0 to 3)	—
CSnWCR1	—	CSn weight control register 1 (n = 0 to 3)	—
CSnWCR2	—	CSn weight control register 2 (n = 0 to 3)	—
BERSR1	MST[2:0]	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved
BUSPRI	BPHB[1:0]	Internal peripheral bus 4 priority control bits	—
	BPEB[1:0]	External bus priority control bits	—

2.13 Event Link Controller

Table 2.23 shows a comparative listing of the event link controller specifications, Table 2.24 shows a comparative listing of the event link controller registers, and Table 2.25 shows a comparative listing of ELSRn register setting values.

Table 2.23 Comparative Listing of Event Link Controller Specifications

Item	RX230/RX231 (ELC)	RX130 (ELC)
Event link function	• 63 event signals can be directly connected to modules. • It is possible to specify that timer modules operate when an event is input. • Event link operation is possible for port B and port E. Single-port: Event link operation can be enabled for a specified single bit in a port. Port group: Event link operation can be enabled for a group of specified bits within an 8-bit I/O port.	• 47 event signals can be directly connected to modules. • It is possible to specify that timer modules operate when an event is input. • Event link operation is possible for port B. Single-port: Event link operation can be enabled for a specified single bit in a port. Port group: Event link operation can be enabled for a group of specified bits within an 8-bit I/O port.
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.

Table 2.24 Comparative Listing of Event Link Controller Registers

Register	Bit	RX230/RX231 (ELC)	RX130 (ELC)
ELSR19	ELS[7:0]	Event link setting register 19 ICU (interrupt 2)	—
ELSR21	ELS[7:0]	Event link setting register 21 output port group 2	—
ELSR23	ELS[7:0]	Event link setting register 23 input port group 2	—
ELSR26	ELS[7:0]	Event link setting register 26 single port 2	—
ELSR27	ELS[7:0]	Event link setting register 27 single port 3	—
ELSR28	ELS[7:0]	Event link setting register 28 Clock source switching to LOCO	—
ELSR29	ELS[7:0]	Event link setting register 29 POE	—
PGR2	—	Port group setting register 2	—
PGC2	—	Port group control register 2	—
PDBF2	—	Port buffer register 2	—
PELn	—	Event link port setting register n (n = 0 to 3)	Event link port setting register n (n = 0, 1)
	PSP[1:0]	Port number specification bits b4 b3 0 0: Setting disabled 0 1: Port B (corresponding to PGR1 register) 1 0: Port E (corresponding to PGR2 register) 1 1: Do not set	Port number specification bits b4 b3 0 0: Setting disabled 0 1: Port B (corresponding to PGR1 register) 1 x: Do not set

Table 2.25 Comparative Listing of ELSRn Register Setting Values

Setting Value	RX230/RX231	RX130	Event
2Eh	○	—	RTC cycle (selects 1/256, 1/64, 1/4, 1, or 2 seconds)
31h	○	—	IWDT underflow or refresh error
52h	○	—	RSPI0 error (mode fault, overrun, or parity error)
53h	○	—	RSPI0 idle
54h	○	—	RSPI0 receive data full
55h	○	—	RSPI0 transmit data empty
56h	○	—	RSPI0 transmit end (except when in clock synchronous slave mode)
5Ch	○	—	LVD2 voltage detection
5Dh	○	—	DMAC0 transfer end
5Eh	○	—	DMAC1 transfer end
5Fh	○	—	DMAC2 transfer end
60h	○	—	DMAC3 transfer end
62h	○	—	Oscillation stop detection of clock generation circuit
64h	○	—	Input edge detection of input port group 2
67h	○	—	Input edge detection of single input port 2
68h	○	—	Input edge detection of single input port 3

2.14 I/O Ports

Table 2.26 lists the points of difference between general I/O ports (100-pin package), Table 2.27 lists the points of difference between general I/O ports (64-pin package), Table 2.28 lists the points of difference between general I/O ports (48-pin package), and Table 2.29 lists the points of difference between the I/O registers related to I/O ports.

Table 2.26 Points of Difference between General I/O Ports (100-Pin Package)

Item	Port Symbol	RX230 RX231	RX130
Input pull-up function	PORT0	P03, p05. P07	P03, P04, P05, P06, P07
	PORT1	P12, P13, P14, P15, P16, P17,	P12, P13, P14, P15, P16, P17,
	PORT2	P20, P21, P22, P23, P24, P25, P26, P27	P20, P21, P22, P23, P24, P25, P26, P27
	PORT3	P30, P31, P32, P33, P34, P35, P36, P37	P30, P31, P32, P33, P34, P35, P36, P37
	PORT4	P40, P41, P42, P43, P44, P45, P46, P47	P40, P41, P42, P43, P44, P45, P46, P47
	PORT5	P50, P51, P52, P53, P54, P55	P50, P51, P52, P53, P54, P55
	PORTA	PA0, PA1, PA2, PA3, PA4, PA5, PA6, PA7	PA0, PA1, PA2, PA3, PA4, PA5, PA6, PA7
	PORTB	PB0, PB1, PB3, PB5, PB6, PB7	PB0, PB1, PB2, PB3, PB4, PB5, PB6, PB7
	PORTC	PC2, PC3, PC4, PC5, PC6, PC7	PC0, PC1, PC2, PC3, PC4, PC5, PC6, PC7
	PORTE	PE0, PE1, PE2, PE3, PE4, PE5, PE6, PE7	PE0, PE1, PE2, PE3, PE4, PE5, PE6, PE7
	PORTH	PH0, PH1, PH2, — PH3	PH0, PH1, PH2, PH3
	PORTJ	PJ3	PJ1, PJ3, PJ6, PJ7
Open-drain output function	PORT1	P12, P13, P14, P15, P16, P17	P12, P13, P14, P15, P16, P17
	PORT2	P20, P21, P22, P23, P24, P25, P26, P27	P20, P21, P22, P23, P24, P25, P26, P27
	PORT3	P30, P31, P32, P33, P34, P36, P37	P30, P31, P32, P33, P34, P36, P37
	PORT5	P50, P51, P52, P54	—
	PORTA	PA0, PA1, PA2, PA3, PA4, PA5, PA6, PA7	PA0, PA1, PA2, PA3, PA4, PA5, PA6, PA7
	PORTB	PB0, PB1, PB2, PB3, PB4, PB5, PB6, PB7	PB0, PB1, PB2, PB3, PB4, PB5, PB6, PB7
	PORTC	PC0, PC1, PC2, PC3, PC4, PC5, PC6, PC7	PC0, PC1, PC2, PC3, PC4, PC5, PC6, PC7
	PORTD	—	PD0, PD1, PD2
	PORTE	PE0, PE1, PE2, PE3, PE4, PE5, PE6, PE7	PE0, PE1, PE2, PE3
	PORTJ	PJ3	PJ3
Drive capacity switching function	PORT1	P12, P13, P14, P15, P16, P17	P12, P13, P14, P15, P16, P17
	PORT2	P20, P21, P22, P23, P24, P25, P26, P27	P20, P21, P22, P23, P24, P25, P26, P27
	PORT3	P30, P31, P32, P33, P34	P30, P31, P32, P33, P34
	PORT5	P50, P51, P52, P53, P54, P55	P50, P51, P52, P53, P54, P55
	PORTA	PA0, PA1, PA2, PA3, PA4, PA5, PA6, PA7	PA0, PA1, PA2, PA3, PA4, PA5, PA6, PA7
	PORTB	PB0, PB1, PB3, PB5, PB6, PB7	PB0, PB1, PB2, PB3, PB4, PB5, PB6, PB7

Item	Port Symbol	RX230 RX231	RX130
Drive capacity switching function	PORTC	PC2, PC3, PC4, PC5, PC6, PC7	PC0, PC1, PC2, PC3, PC4, PC5, PC6, PC7
	PORTD	PD0, PD1, PD2, PD3, PD4, PD5, PD6, PD7	PD0, PD1, PD2, PD3, PD4, PD5, PD6, PD7
	PORTE	PE0, PE1, PE2, PE3, PE4, PE5, PE6, PE7	PE0, PE1, PE2, PE3, PE4, PE5, PE6, PE7
	PORTH	PH0, PH1, PH2, PH3	— PH0, PH1, PH2, PH3
	PORTJ	PJ3	PJ1, PJ3
5 V tolerant	PORT1	P12, P13, P16, P17	P12, P13, P16, P17
	PORT3	P30, P31, P32	—
	PORTB	PB5	—

Table 2.27 Points of Difference between General I/O Ports (64-Pin Package)

Item	Port Symbol	RX230 RX231	RX130
Input pull-up function	PORT0	P03, P05	P03, P05
	PORT1	P14, P15, P16, P17	P14, P15, P16, P17
	PORT2	P26, P27	P26, P27
	PORT3	P30, P31, P36, P37	P30, P31, P32, P36, P37
	PORT4	P40, P41, P42, P43, P44, P46	P40, P41, P42, P43, P44, P45, P46, P47
	PORT5	P54, P55	P54, P55
	PORTA	PA0, PA1, PA3, PA4, PA6	PA0, PA1, PA3, PA4, PA6
	PORTB	PB0, PB1, PB3, PB5, PB6*, PB7*	PB0, PB1, PB3, PB5, PB6*, PB7*
	PORTC	PC0*1, PC1*1, PC2, PC3, PC4, PC5, PC6, PC7	PC0*1, PC1*1, PC2, PC3, PC4, PC5, PC6, PC7
	PORTE	PE0, PE1, PE2, PE3, PE4, PE5	PE0, PE1, PE2, PE3, PE4, PE5
	PORTH	PH0, PH1, PH2, PH3 —	PH0, PH1, PH2, PH3
	PORTJ	—	PJ6, PJ7
Open-drain output function	PORT1	P14, P15, P16, P17	P14, P15, P16, P17
	PORT2	P26, P27	P26, P27
	PORT3	P30, P31, P36, P37	P30, P31, P32, P36, P37
	PORT5	P54	—
	PORTA	PA0, PA1, PA3, PA4, PA6	PA0, PA1, PA3, PA4, PA6
	PORTB	PB0, PB1, PB3, PB5, PB6*1, PB7*1	PB0, PB1, PB3
	PORTC	PC0*1, PC1*1, PC2, PC3, PC4, PC5, PC6, PC7	PC0*1, PC1*1, PC2, PC3, PC4, PC5, PC6, PC7
	PORTE	PE0, PE1, PE2, PE3, PE4, PE5	PE0, PE1, PE2, PE3
Drive capacity switching function	PORT1	P14, P15, P16, P17	P14, P15, P16, P17
	PORT2	P26, P27	P26, P27
	PORT3	P30, P31	P30, P31, P32
	PORT5	P54, P55	P54, P55
	PORTA	PA0, PA1, PA3, PA4, PA6	PA0, PA1, PA3, PA4, PA6
	PORTB	PB0, PB1, PB3, PB5, PB6*1, PB7*1	PB0, PB1, PB3, PB5, PB6*1, PB7*1
	PORTC	PC0*1, PC1*1, PC2, PC3, PC4, PC5, PC6, PC7	PC0*1, PC1*1, PC2, PC3, PC4, PC5, PC6, PC7
	PORTE	PE0, PE1, PE2, PE3, PE4, PE5	PE0, PE1, PE2, PE3, PE4, PE5
	PORTH	PH0, PH1, PH2, PH3 —	PH0, PH1, PH2, PH3
5 V tolerant	PORT1	P16, P17	P16, P17
	PORT3	P30, P31	—
	PORT5	PB5	—

Note 1. On 80-pin (RX130 only) and 64-pin package products, pins PB6 and PC0, and PB7 and PC1 have multiplexed functions. These can be switched by making settings to the PSRA register. The pin functions conform to the settings of the selected port.

Table 2.28 Points of Difference between General I/O Ports (48-Pin Package)

Item	Port Symbol	RX230 RX231	RX130
Input pull-up function	PORT1	P14, P15, P16, P17	P14, P15, P16, P17
	PORT2	P26, P27	P26, P27
	PORT3	P30, P31, P36, P37	P30, P31, P36, P37
	PORT4	P40, P41, P42, P43, P44, P46	P40, P41, P42 P45, P46, P47
	PORTA	PA1, PA3, PA4, PA6	PA1, PA3, PA4, PA6
	PORTB	PB0*1, PB1*1, PB3*1, PB5*1	PB0*1, PB1*1, PB3*1, PB5*1
	PORTC	PC0*1, PC1*1, PC2*1, PC3*1, PC4, PC5, PC6, PC7	PC0*1, PC1*1, PC2*1, PC3*1, PC4, PC5, PC6, PC7
	PORTE	PE1, PE2, PE3, PE4	PE1, PE2, PE3, PE4
	PORTH	PH0, PH1, PH2, — PH3	PH0, PH1, PH2, PH3
	PORTJ	—	PJ6, PJ7
Open-drain output function	PORT1	P14, P15, P16, P17	P14, P15, P16, P17
	PORT2	P26, P27	P26, P27
	PORT3	P30, P31, P36, P37	P30, P31, P36, P37
	PORTA	PA1, PA3, PA4, PA6	PA1, PA3, PA4, PA6
	PORTB	PB0*1, PB1*1, PB3*1, PB5*1	PB0*1, PB1*1, PB3*1
	PORTC	PC0*1, PC1*1, PC2*1, PC3*1, PC4, PC5, PC6, PC7	PC0*1, PC1*1, PC2*1, PC3*1, PC4, PC5, PC6, PC7
	PORTE	PE0, PE1, PE2, PE3, PE4	PE0, PE1, PE2, PE3
Drive capacity switching function	PORT1	P14, P15, P16, P17	P14, P15, P16, P17
	PORT2	P26, P27	P26, P27
	PORT3	P30, P31	P30, P31
	PORTA	PA1, PA3, PA4, PA6	PA1, PA3, PA4, PA6
	PORTB	PB0*1, PB1*1, PB3*1, PB5*1	PB0*1, PB1*1, PB3*1, PB5*1
	PORTC	PC0*1, PC1*1, PC2*1, PC3*1, PC4, PC5, PC6, PC7	PC0*1, PC1*1, PC2*1, PC3*1, PC4, PC5, PC6, PC7
	PORTE	PE0, PE1, PE2, PE3	PE0, PE1, PE2, PE3
	PORTH	PH0, PH1, PH2, — PH3	PH0, PH1, PH2, PH3
5 V tolerant	PORT1	P16, P17	P16, P17
	PORT3	P30, P31	—
	PORTB	PB5	—

Note 1. On 48-pin package products, pins PB0 and PC0, PB1 and PC1, PB3 and PC2, and PB5 and PC3 have multiplexed functions. These can be switched by making settings to the PSRB register. The pin functions conform to the settings of the selected port.

Table 2.29 Comparative Listing of I/O Port Registers

Register	Bit	RX230/RX231	RX130
ODR0	B2	Pm1 output type select bit • P21, P31, P51, PA1, PB1, PC1 b2 0: CMOS output 1: N-channel open-drain output b3 This bit is read as 0. The write value should be 0. • PE1 b3 b2 00: CMOS output 01: N-channel open-drain output 10: P-channel open-drain output 11: Hi-Z	Pm1 output type select bit • P21, P31, PA1, PB1, PC1, PD1 b2 0: CMOS output 1: N-channel open-drain output b3 This bit is read as 0. The write value should be 0. • PE1 b3 b2 00: CMOS output 01: N-channel open-drain output 10: P-channel open-drain output 11: Hi-Z

2.15 Multi-Function Pin Controller

Table 2.30 shows a comparative listing of functions assigned to each multiplexed pin, and Table 2.31 shows a comparative listing of the multi-function pin controller port registers.

Blue characters exist only in the RX230/RX231, and orange characters exist only in the RX130. "√" indicates pin implemented, "×" indicates pin not implemented, "-" indicates no assignment pin for function, Grey hatching indicates pin function not implemented.

Table 2.30 Comparative Listing of Functions Assigned to Each Multiplexed Pin

Module/Function	Pin Functions	Allocation Port	RX230 / RX231			RX130		
			100 pin	64 pin	48 pin	100 pin	64 pin	48 pin
Interrupt	NMI (input)	P35	○	○	○	○	○	○
	IRQ0 (input)	P30	○	○	○	○	○	○
		PD0	○	×	×	○	×	×
		PH1	○	○	○	○	○	○
	IRQ1 (input)	P31	○	○	○	○	○	○
		PD1	○	×	×	○	×	×
		PH2	○	○	○	○	○	○
	IRQ2 (input)	P32	○	×	×	○	○	×
		P12	○	×	×	○	×	×
		PD2	○	×	×	○	×	×
	IRQ3 (input)	P33	○	×	×	○	×	×
		P13	○	×	×	○	×	×
		PD3	○	×	×	○	×	×
	IRQ4 (input)	PB1	○	○	○	○	○	○
		P14	○	○	○	○	○	○
		P34	○	×	×	○	×	×
		PD4	○	×	×	○	×	×
	IRQ5 (input)	PA4	○	○	○	○	○	○
		P15	○	○	○	○	○	○
		PD5	○	×	×	○	×	×
		PE5	○	○	×	○	○	×
	IRQ6 (input)	PA3	○	○	○	○	○	○
		P16	○	○	○	○	○	○
		PD6	○	×	×	○	×	×
		PE6	○	×	×	○	×	×
	IRQ7 (input)	PE2	○	○	○	○	○	○
		P17	○	○	○	○	○	○
		PD7	○	×	×	○	×	×
		PE7	○	×	×	○	×	×
Clock generation circuit	CLKOUT (output)	PE3	○	○	○	○	○	○
		PE4	○	○	○	○	○	○
Multi-function timer unit 2	MTIOC0A (input/output)	P34	○	×	×	○	×	×
		PB3	○	○	○	○	○	○
	MTIOC0B (input/output)	P13	○	×	×	○	×	×
		P15	○	○	○	○	○	○
		PA1	○	○	○	○	○	○
	MTIOC0C (input/output)	P32	○	×	×	○	○	×
		PB1	○	○	○	○	○	○

Module/Function	Pin Functions	Allocation Port	RX230 / RX231			RX130		
			100 pin	64 pin	48 pin	100 pin	64 pin	48 pin
Multi-function timer unit 2	MTIOC0D (input/output)	P33	○	×	×	○	×	×
		PA3	○	○	○	○	○	○
	MTIOC1A (input/output)	P20	○	×	×	○	×	×
		PE4	○	○	○	○	○	○
	MTIOC1B (input/output)	P21	○	×	×	○	×	×
		PB5	○	○	○	○	○	○
	MTIOC2A (input/output)	P26	○	○	○	○	○	○
		PB5	○	○	○	○	○	○
	MTIOC2B (input/output)	P27	○	○	○	○	○	○
		PE5	○	○	×	○	○	×
	MTIOC3A (input/output)	P14	○	○	○	○	○	○
		P17	○	○	○	○	○	○
		PC1	○	×	×	○	×	×
		PC7	○	○	○	○	○	○
		PJ1	-	-	-	○	×	×
	MTIOC3B (input/output)	P17	○	○	○	○	○	○
		P22	○	×	×	○	×	×
		PB7	○	○	×	○	○	×
		PC5	○	○	○	○	○	○
	MTIOC3C (input/output)	P16	○	○	○	○	○	○
		PC0	○	×	×	○	×	×
		PC6	○	○	○	○	○	○
		PJ3	○	×	×	○	×	×
	MTIOC3D (input/output)	P16	○	○	○	○	○	○
		P23	○	×	×	○	×	×
		PB6	○	○	×	○	○	×
		PC4	○	○	○	○	○	○
	MTIOC4A (input/output)	P24	○	×	×	○	×	×
		PA0	○	○	×	○	○	×
		PB3	○	○	○	○	○	○
		PE2	○	○	○	○	○	○
	MTIOC4B (input/output)	P30	○	○	○	○	○	○
		P54	○	○	×	○	○	×
		PC2	○	○	×	○	○	×
		PD1	○	×	×	○	×	×
		PE3	○	○	○	○	○	○
	MTIOC4C (input/output)	P25	○	×	×	○	×	×
		PB1	○	○	○	○	○	○
		PE1	○	○	○	○	○	○
		PE5	○	○	×	○	○	×

Module/Function	Pin Functions	Allocation Port	RX230 / RX231			RX130		
			100 pin	64 pin	48 pin	100 pin	64 pin	48 pin
Multi-function timer unit 2	MTIOC4D (input/output)	P31	○	○	○	○	○	○
		P55	○	○	×	○	○	×
		PC3	○	○	×	○	○	×
		PD2	○	×	×	○	×	×
		PE4	○	○	○	○	○	○
	MTIC5U (input)	PA4	○	○	○	○	○	○
		PD7	○	×	×	○	×	×
	MTIC5V (input)	PA6	○	○	○	○	○	○
		PD6	○	×	×	○	×	×
	MTIC5W (input)	PB0	○	○	○	○	○	○
		PD5	○	×	×	○	×	×
	MTCLKA (input)	P14	○	○	○	○	○	○
		P24	○	×	×	○	×	×
		PA4	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	MTCLKB (input)	P15	○	○	○	○	○	○
		P25	○	×	×	○	×	×
		PA6	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	MTCLKC (input)	P22	○	×	×	○	×	×
		PA1	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	MTCLKD (input)	P23	○	×	×	○	×	×
		PA3	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
Port output enable 2	POE0# (input)	PC4	○	○	○	○	○	○
		PD7	○	×	×	○	×	×
	POE1# (input)	PB5	○	○	○	○	○	○
		PD6	○	×	×	○	×	×
	POE2# (input)	P34	○	×	×	○	×	×
		PA6	○	○	○	○	○	○
		PD5	○	×	×	○	×	×
	POE3# (input)	P33	○	×	×	○	×	×
		PB3	○	○	○	○	○	○
		PD4	○	×	×	○	×	×
	POE8# (input)	P17	○	○	○	○	○	○
		P30	○	○	○	○	○	○
		PD3	○	×	×	○	×	×
		PE3	○	○	○	○	○	○

Module/Function	Pin Functions	Allocation Port	RX230 / RX231			RX130		
			100 pin	64 pin	48 pin	100 pin	64 pin	48 pin
16-bit timer pulse unit	TIOCA0 (input/output)	PA0	○	○	×			
	TIOCB0 (input/output)	P17	○	○	○			
		PA1	○	○	○			
	TIOCC0 (input/output)	P32	○	×	×			
	TIOCD0 (input/output)	P33	○	×	×			
		PA3	○	○	○			
	TIOCA1 (input/output)	PA4	○	○	○			
	TIOCB1 (input/output)	P16	○	○	○			
		PA5	○	×	×			
	TIOCA2 (input/output)	PA6	○	○	○			
	TIOCB2 (input/output)	P15	○	○	○			
		PA7	○	×	×			
	TIOCA3 (input/output)	P21	○	×	×			
		PB0	○	○	○			
	TIOCB3 (input/output)	P20	○	×	×			
		PB1	○	○	○			
	TIOCC3 (input/output)	P22	○	×	×			
		PB2	○	×	×			
	TIOCD3 (input/output)	P23	○	×	×			
		PB3	○	○	○			
	TIOCA4 (input/output)	P25	○	×	×			
		PB4	○	×	×			
	TIOCB4 (input/output)	P24	○	×	×			
		PB5	○	○	○			
	TIOCA5 (input/output)	P13	○	×	×			
		PB6	○	○	×			
	TIOCB5 (input/output)	P14	○	○	○			
		PB7	○	○	×			
	TCLKA (input)	P14	○	○	○			
		PC2	○	○	×			
	TCLKB (input)	P15	○	○	○			
		PA3	○	○	○			
		PC3	○	○	×			
	TCLKC (input)	P16	○	○	○			
		PB2	○	×	×			
		PC0	○	×	×			
	TCLKD (input)	P17	○	○	○			
		PB3	○	○	○			
		PC1	○	×	×			

Module/Function	Pin Functions	Allocation Port	RX230 / RX231			RX130		
			100 pin	64 pin	48 pin	100 pin	64 pin	48 pin
8-bit timer	TMO0 (output)	P22	○	×	×	○	×	×
		PB3	○	○	○	○	○	○
		PH1	○	○	○	○	○	○
	TMCI0 (input)	P21	○	×	×	○	×	×
		PB1	○	○	○	○	○	○
		PH3	○	○	○	○	○	○
	TMRI0 (input)	P20	○	×	×	○	×	×
		PA4	○	○	○	○	○	○
		PH2	○	○	○	○	○	○
	TMO1 (output)	P17	○	○	○	○	○	○
		P26	○	○	○	○	○	○
	TMCI1 (input)	P12	○	×	×	○	×	×
		P54	○	○	×	○	○	×
		PC4	○	○	○	○	○	○
	TMRI1 (input)	P24	○	×	×	○	×	×
		PB5	○	○	○	○	○	○
	TMO2 (output)	P16	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	TMCI2 (input)	P15	○	○	○	○	○	○
		P31	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	TMRI2 (input)	P14	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
	TMO3 (output)	P13	○	×	×	○	×	×
		P32	○	×	×	○	○	×
		P55	○	○	×	○	○	×
	TMCI3 (input)	P27	○	○	○	○	○	○
		P34	○	×	×	○	×	×
		PA6	○	○	○	○	○	○
	TMRI3 (input)	P30	○	○	○	○	○	○
		P33	○	×	×	○	×	×
Serial communications interface	RXD0 (input)/ SMISO0 (input/output)/ SSCL0 (input/output)	P21	○	×	×	○	×	×
	TXD0 (output)/ SMOSI0 (input/output)/ SSDA0 (input/output)	P20	○	×	×	○	×	×
	SCK0 (input/output)	P22	○	×	×	○	×	×
	CTS0# (input)/ RTS0# (output)/ SS0# (input)	P23	○	×	×	○	×	×

Module/Function	Pin Functions	Allocation Port	RX230 / RX231			RX130		
			100 pin	64 pin	48 pin	100 pin	64 pin	48 pin
Serial communications interface	RXD1 (input)/ SMISO1 (input/output)/ SSCL1 (input/output)	P15	○	○	○	○	○	○
		P30	○	○	○	○	○	○
	TXD1 (output)/ SMOSI1 (input/output)/ SSDA1 (input/output)	P16	○	○	○	○	○	○
		P26	○	○	○	○	○	○
	SCK1 (input/output)	P17	○	○	○	○	○	○
		P27	○	○	○	○	○	○
	CTS1# (input)/ RTS1# (output)/ SS1# (input)	P14	○	○	○	○	○	○
		P31	○	○	○	○	○	○
	RXD5 (input)/ SMISO5 (input/output)/ SSCL5 (input/output)	PA2	○	×	×	○	×	×
		PA3	○	○	○	○	○	○
		PC2	○	○	×	○	○	×
	TXD5 (output)/ SMOSI5 (input/output)/ SSDA5 (input/output)	PA4	○	○	○	○	○	○
		PC3	○	○	×	○	○	×
	SCK5 (input/output)	PA1	○	○	○	○	○	○
		PC1	○	×	×	○	×	×
		PC4	○	○	○	○	○	○
	CTS5# (input)/ RTS5# (output)/ SS5# (input)	PA6	○	○	○			
		PC0	○	×	×			
	RXD6 (input)/ SMISO6 (input/output)/ SSCL6 (input/output)	P33	○	×	×	○	×	×
		PB0	○	○	○	○	○	○
		PD1	-	-	-	○	×	×
	TXD6 (output)/ SMOSI6 (input/output)/ SSDA6 (input/output)	P32	○	×	×	○	○	×
		PB1	○	○	○	○	○	○
		PD0	-	-	-	○	×	×
	SCK6 (input/output)	P34	○	×	×	○	×	×
		PB3	○	○	○	○	○	○
		PD2	-	-	-	○	×	×
	CTS6# (input)/ RTS6# (output)/ SS6# (input)	PB2	○	×	×	○	×	×
		PJ3	○	×	×	○	×	×

Module/Function	Pin Functions	Allocation Port	RX230 / RX231			RX130		
			100 pin	64 pin	48 pin	100 pin	64 pin	48 pin
Serial communications interface	RXD8 (input)/ SMISO8 (input/output)/ SSCL8 (input/output)	PC6	○	○	○	○	×	×
	TXD8 (output)/ SMOSI8 (input/output)/ SSDA8 (input/output)	PC7	○	○	○	○	×	×
	SCK8 (input/output)	PC5	○	○	○	○	×	×
	CTS8# (input)/ RTS8# (output)/ SS8# (input)	PC4	○	○	○	○	×	×
	RXD9 (input)/ SMISO9 (input/output)/ SSCL9 (input/output)	PB6	○	○	×	○	×	×
	TXD9 (output)/ SMOSI9 (input/output)/ SSDA9 (input/output)	PB7	○	○	×	○	×	×
	SCK9 (input/output)	PB5	○	○	×	○	×	×
	CTS9# (input)/ RTS9# (output)/ SS9# (input)	PB4	○	×	×	○	×	×
	RXD12 (input)/ SMISO12 (input/output)/ SSCL12 (input/output)/ RXDX12 (input)	PE2	○	○	○	○	○	○
	TXD12 (output)/ SMOSI12 (input/output)/ SSDA12 (input/output)/ TXDX12 (output)/ SIOX12 (input/output)	PE1	○	○	○	○	○	○
	SCK12 (input/output)	PE0	○	○	×	○	○	×
	CTS12# (input)/ RTS12# (output)/ SS12# (input)	PE3	○	○	○	○	○	○

Module/Function	Pin Functions	Allocation Port	RX230 / RX231			RX130		
			100 pin	64 pin	48 pin	100 pin	64 pin	48 pin
I²C bus interface	SCL (input/output)	P16	○	○	○	○	○	○
		P12	○	×	×	○	×	×
	SDA (input/output)	P17	○	○	○	○	○	○
		P13	○	×	×	○	×	×
Serial peripheral interface	RSPCKA (input/output)	PA5	○	×	×	○	×	×
		PB0	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
	MOSIA (input/output)	P16	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	MISOA (input/output)	P17	○	○	○	○	○	○
		PA7	○	×	×	○	×	×
		PC7	○	○	○	○	○	○
	SSLA0 (input/output)	PA4	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	SSLA1 (output)	PA0	○	○	×	○	○	×
		PC0	○	×	×	○	×	×
	SSLA2 (output)	PA1	○	○	○	○	○	○
		PC1	○	×	×	○	×	×
	SSLA3 (output)	PA2	○	×	×	○	×	×
		PC2	○	○	×	○	○	×
Realtime clock	RTCOUT (output)	P16	○	○	×	○	○	×
		P32	○	×	×	○	○	×
	RTCIC0 (input)	P30	○	○	×			
	RTCIC1 (input)	P31	○	○	×			
	RTCIC2 (input)	P32	○	×	×			
IrDA interface	IRTXD5 (output)	PA4	○	○	○			
		PC3	○	○	×			
	IRRXD5 (input)	PA2	○	×	×			
		PA3	○	○	○			
		PC2	○	○	×			
CAN module	CRXD0 (input)	P15	○	○	○			
		P55	○	○	×			
	CTXD0 (output)	P14	○	○	○			
		P54	○	○	×			
Serial sound interface	SSISCK0 (input/output)	P23	○	×	×			
		P31	○	○	○			
		PA1	○	○	○			
	SSIWS0 (input/output)	P21	○	×	×			
		P27	○	○	○			
		PA6	○	○	○			
	SSITXD0 (output)	P17	○	○	○			
		PA4	○	○	○			
	SSIRXD0 (input)	P20	○	×	×			
		P26	○	○	○			
		PA3	○	○	○			

Module/Function	Pin Functions	Allocation Port	RX230 / RX231			RX130		
			100 pin	64 pin	48 pin	100 pin	64 pin	48 pin
Serial sound interface	AUDIO_MCLK (input)	P22	○	×	×			
		P30	○	○	○			
		PE3	○	○	○			
SD host interface	SDHI_CLK (output)	PB1	○	○	×			
	SDHI_CMD (input/output)	PB0	○	○	×			
	SDHI_D0 (input/output)	PC3	○	○	×			
	SDHI_D1 (input/output)	PB6	○	○	×			
		PC4	○	○	×			
	SDHI_D2 (input/output)	PB7	○	○	×			
	SDHI_D3 (input/output)	PC2	○	○	×			
	SDHI_CD (input)	PB5	○	○	×			
	SDHI_WP (input)	PB3	○	○	×			
USB 2.0 host/function module	USB0_VBUS (input)	P16	○	○	○			
		PB5	○	○	○			
	USB0_EXICEN (output)	P21	○	×	×			
		PC6	×	○	○			
	USB0_VBUSEN (output)	P16	○	○	○			
		P24	○	×	×			
		P26	×	○	○			
		P32	○	×	×			
	USB0_OVRCURA (input)	P14	○	○	○			
	USB0_OVRCURB (input)	P16	○	○	○			
		P22	○	×	×			
	USB0_ID (input)	P20	○	×	×			
		PC5	×	○	○			
12-bit A/D converter	AN000 (input)	P40	○	○	○	○	○	○
	AN001 (input)	P41	○	○	○	○	○	○
	AN002 (input)	P42	○	○	○	○	○	○
	AN003 (input)	P43	○	○	×	○	○	×
	AN004 (input)	P44	○	○	×	○	○	×
	AN005 (input)	P45	○	×	×	○	○	○
	AN006 (input)	P46	○	○	○	○	○	○
	AN007 (input)	P47	○	×	×	○	○	○
	AN016 (input)	PE0	○	○	×	○	○	×
	AN017 (input)	PE1	○	○	○	○	○	○
	AN018 (input)	PE2	○	○	○	○	○	○
	AN019 (input)	PE3	○	○	○	○	○	○
	AN020 (input)	PE4	○	○	○	○	○	○
	AN021 (input)	PE5	○	○	×	○	○	×
	AN022 (input)	PE6	○	×	×	○	×	×
	AN023 (input)	PE7	○	×	×	○	×	×

Module/Function	Pin Functions	Allocation Port	RX230 / RX231			RX130		
			100 pin	64 pin	48 pin	100 pin	64 pin	48 pin
12-bit A/D converter	AN024 (input)	PD0	○	×	×	○	×	×
	AN025 (input)	PD1	○	×	×	○	×	×
	AN026 (input)	PD2	○	×	×	○	×	×
	AN027 (input)	PD3	○	×	×	○	×	×
	AN028 (input)	PD4	○	×	×	○	×	×
	AN029 (input)	PD5	○	×	×	○	×	×
	AN030 (input)	PD6	○	×	×	○	×	×
	AN031 (input)	PD7	○	×	×	○	×	×
	ADTRG0# (input)	P07	○	×	×	○	×	×
		P16	○	○	○	○	○	○
		P25	○	×	×	○	×	×
D/A converter	DA0 (output)	P03	○	○	×	○	○	×
	DA1 (output)	P05	○	○	×	○	○	×
Clock frequency accuracy measurement circuit	CACREF (input)	PA0	○	○	×	○	○	×
		PC7	○	○	○	○	○	○
		PH0	○	○	○	○	○	○
LVD voltage detection input	CMPA2 (input)	PE4	○	○	○	○	○	○
Comparator B	CMPB0 (input)	PE1	○	○	○	○	○	○
	CVREFB0 (input)	PE2	○	○	○	○	○	○
	CMPB1 (input)	PA3	○	○	○	○	○	○
	CVREFB1 (input)	PA4	○	○	○	○	○	○
	CMPB2 (input)	P15	○	○	○			
	CVREFB2 (input)	P14	○	○	○			
	CMPB3 (input)	P26	○	○	○			
	CVREFB3 (input)	P27	○	○	○			
	CMPOB0 (output)	PE5	○	○	×	○	○	×
	CMPOB1 (output)	PB1	○	○	○	○	○	○
	CMPOB2 (output)	P17	○	○	○			
	CMPOB3 (output)	P30	○	○	○			
Capacitive touch sensing unit (CTSU)	TSCAP (output)	PC4	○	○	○			
	TSCAP (—)	PC4				○	○	○
	TS0 (output)	P34	○	×	×			
	TS0 (input/output)	P32				○	○	×
	TS1 (output)	P33	○	×	×			
	TS1 (input/output)	P31				○	○	○
	TS2 (output)	P27	○	○	○	-	-	-
		P30	-	-	-	○	○	○
	TS3 (output)	P26	○	○	○	-	-	-
		P27	-	-	-	○	○	○
	TS4 (output)	P25	○	×	×	-	-	-
		P26	-	-	-	○	○	○
	TS5 (output)	P24	○	×	×	-	-	-
		P15	-	-	-	○	○	○

Module/Function	Pin Functions	Allocation Port	RX230 / RX231			RX130		
			100 pin	64 pin	48 pin	100 pin	64 pin	48 pin
Capacitive touch sensing unit (CTSU)	TS6 (output)	P23	○	×	×	-	-	-
		P14	-	-	-	○	○	○
	TS7 (output)	P22	○	×	×	-	-	-
		PH3	-	-	-	○	○	○
	TS8 (output)	P21	○	×	×	-	-	-
		PH2	-	-	-	○	○	○
	TS9 (output)	P20	○	×	×	-	-	-
		PH1	-	-	-	○	○	○
	TS10 (output)	PH0				○	○	○
	TS11 (output)	P55				○	○	×
	TS12 (output)	P15	○	○	○	-	-	-
		P54	-	-	-	○	○	×
	TS13 (output)	P14	○	○	○	-	-	-
		PC7	-	-	-	○	○	○
	TS14 (output)	PC6				○	○	○
	TS15 (output)	P55	○	○	×	-	-	-
		PC5	-	-	-	○	○	○
	TS16 (output)	P54	○	○	×	-	-	-
		PC3	-	-	-	○	○	×
	TS17 (output)	P53	○	×	×	-	-	-
		PC2	-	-	-	○	○	×
	TS18 (output)	P52	○	×	×	-	-	-
		PB7	-	-	-	○	○	×
	TS19 (output)	P51	○	×	×	-	-	-
		PB6	-	-	-	○	○	×
	TS20 (output)	P50	○	×	×	-	-	-
		PB5	-	-	-	○	○	○
	TS21 (output)	PB4				○	×	×
	TS22 (output)	PC6	○	○	○	-	-	-
		PB3	-	-	-	○	○	○
	TS23 (output)	PC5	○	○	○	-	-	-
		PB2	-	-	-	○	×	×
	TS24 (output)	PB1				○	○	○
	TS25 (output)	PB0				○	○	○
	TS26 (output)	PA6				○	○	○
	TS27 (output)	PC3	○	○	×	-	-	-
		PA5	-	-	-	○	×	×
	TS28 (output)	PA4				○	○	○
	TS29 (output)	PA3				○	○	○
	TS30 (output)	PC2	○	○	×	-	-	-
		PA2	-	-	-	○	×	×
	TS31 (output)	PA1				○	○	○
	TS32 (output)	PA0				○	○	×

Module/Function	Pin Functions	Allocation Port	RX230 / RX231			RX130		
			100 pin	64 pin	48 pin	100 pin	64 pin	48 pin
Capacitive touch sensing unit (CTSU)	TS33 (output)	PC1	○	×	×	-	-	-
		PE4	-	-	-	○	○	○
	TS34 (output)	PE3				○	○	○
	TS35 (output)	PC0	○	×	×	-	-	-
		PE2	-	-	-	○	○	○
Remote control signal receiver (REMC)	PMC0	P51				○	×	×
	PMC1	P52				○	×	×

Table 2.31 Comparative Listing of Multi-Function Pin Controller Registers

Register	Bit	RX230/RX231 (MPC)	RX130 (MPC)
P0nPFS	ASEL	Analog Function Select 0: Used other than as analog pin 1: Used as analog pin P03: DA0 (100/64 pins) P05: DA1 (100/64 pins)	Analog Function Select 0: Used other than as analog pin 1: Used as analog pin P03: DA0 (100/80/64 pins) P05: DA1 (100/80/64 pins)
P1nPFS	ISEL	Interrupt Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P12: IRQ2 input switch (100 pins) P13: IRQ3 input switch (100 pins) P14: IRQ4 input switch (100/64/48 pins) P15: IRQ5 input switch (100/64/48 pins) P16: IRQ6 input switch (100/64/48 pins) P17: IRQ7 input switch (100/64/48 pins)	Interrupt Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P12: IRQ2 input switch (100/80 pins) P13: IRQ3 input switch (100/80 pins) P14: IRQ4 input switch (100/80/64/48 pins) P15: IRQ5 input switch (100/80/64/48 pins) P16: IRQ6 input switch (100/80/64/48 pins) P17: IRQ7 input switch (100/80/64/48 pins)
	ASEL	Analog Function Select 0: Used other than as analog pin 1: Used as analog pin P14: CVREFB2 (100/64/48 pins) P15: CMPB2 (100/64/48 pins)	—
P2nPFS	ASEL	Analog Function Select 0: Used other than as analog pin 1: Used as analog pin P26: CMPB3 (100/64/48 pins) P27: CVREFB3 (100/64/48 pins)	—

Register	Bit	RX230/RX231 (MPC)	RX130 (MPC)
P3nPFS	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0 input switch (100/64/48 pins) P31: IRQ1 input switch (100/64/48 pins) P32: IRQ2 input switch (100 pins) P33: IRQ3 input switch (100 pins) P34: IRQ4 input switch (100 pins)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0 input switch (100/80/64/48 pins) P31: IRQ1 input switch (100/80/64/48 pins) P32: IRQ2 input switch (100/80/64 pins) P33: IRQ3 input switch (100 pins) P34: IRQ4 input switch (100/80 pins)
P4nPFS	ASEL	Analog Function Select 0: Not used as an analog pin 1: Used as an analog pin P40: AN000 (100/64/48 pins) P41: AN001 (100/64/48 pins) P42: AN002 (100/64/48 pins) P43: AN003 (100/64 pins) P44: AN004 (100/64 pins) P45: AN005 (100 pins) P46: AN006 (100/64/48 pins) P47: AN007 (100 pins)	Analog Function Select 0: Not used as an analog pin 1: Used as an analog pin P40: AN000 (100/80/64/48 pins) P41: AN001 (100/80/64/48 pins) P42: AN002 (100/80/64/48 pins) P43: AN003 (100/80/64 pins) P44: AN004 (100/80/64 pins) P45: AN005 (100/80/64/48 pins) P46: AN006 (100/80/64/48 pins) P47: AN007 (100/80/64/48 pins)
PAnPFS	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PA3: IRQ6 input switch (100/64/48 pins) PA4: IRQ5 input switch (100/64/48 pins)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PA3: IRQ6 input switch (100/80/64/48 pins) PA4: IRQ5 input switch (100/80/64/48 pins)
	ASEL	Analog Function Select 0: Not used as an analog pin 1: Used as an analog pin PA3: CMPB1 (100/64/48 pins) PA4: CVREFB1 (100/64/48 pins)	Analog Function Select 0: Not used as an analog pin 1: Used as an analog pin PA3: CMPB1 (100/80/64/48 pins) PA4: CVREFB1 (100/80/64/48 pins)
PBnPFS	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PB1: IRQ4 (100/64/48 pins)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PB1: IRQ4 (100/80/64/48 pins)

Register	Bit	RX230/RX231 (MPC)	RX130 (MPC)
PDnPFS	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PD0: IRQ0 input switch (100 pins) PD1: IRQ1 input switch (100 pins) PD2: IRQ2 input switch (100 pins) PD3: IRQ3 input switch (100 pins) PD4: IRQ4 input switch (100 pins) PD5: IRQ5 input switch (100 pins) PD6: IRQ6 input switch (100 pins) PD7: IRQ7 input switch (100 pins)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PD0: IRQ0 input switch (100/80 pins) PD1: IRQ1 input switch (100/80 pins) PD2: IRQ2 input switch (100/80 pins) PD3: IRQ3 input switch (100 pins) PD4: IRQ4 input switch (100 pins) PD5: IRQ5 input switch (100 pins) PD6: IRQ6 input switch (100 pins) PD7: IRQ7 input switch (100 pins)
	ASEL	Analog Function Select 0: Used other than as analog pin 1: Used as analog pin PD0: AN024 (100 pins) PD1: AN025 (100 pins) PD2: AN026 (100 pins) PD3: AN027 (100 pins) PD4: AN028 (100 pins) PD5: AN029 (100 pins) PD6: AN030 (100 pins) PD7: AN031 (100 pins)	Analog Function Select 0: Used other than as analog pin 1: Used as analog pin PD0: AN024 (100/80 pins) PD1: AN025 (100/80 pins) PD2: AN026 (100/80 pins) PD3: AN027 (100 pins) PD4: AN028 (100 pins) PD5: AN029 (100 pins) PD6: AN030 (100 pins) PD7: AN031 (100 pins)
PEnPFS	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ7 input switch (100/64/48 pins) PE5: IRQ5 input switch (100/64 pins) PE6: IRQ6 input switch (100 pins) PE7: IRQ7 input switch (100 pins)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ7 input switch (100/80/64/48 pins) PE5: IRQ5 input switch (100/80/64 pins) PE6: IRQ6 input switch (100 pins) PE7: IRQ7 input switch (100 pins)
PEnPFS	ASEL	Analog Function Select 0: Not used as an analog pin 1: Used as an analog pin PE0:AN016 (100/64 pins) PE1:AN017 or CMPB0 (100/64/48 pins) PE2:AN018 or CVREFB0 (100/64/48 pins) PE3:AN019 (100/64/48 pins) PE4:AN020 (100/64/48 pins) PE5:AN021 (100/64 pins) PE6:AN022 (100 pins) PE7:AN023 (100 pins)	Analog Function Select 0: Not used as an analog pin 1: Used as an analog pin PE0:AN016 (100/80/64 pins) PE1:AN017 or CMPB0 (100/80/64/48 pins) PE2:AN018 or CVREFB0 (100/80/64/48 pins) PE3:AN019 (100/80/64/48 pins) PE4:AN020 or CMPA2 (100/80/64/48 pins) PE5:AN021 (100/80/64 pins) PE6:AN022 (100 pins) PE7:AN023 (100 pins)

Register	Bit	RX230/RX231 (MPC)	RX130 (MPC)
PHnPFS	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PH1: IRQ0 (100/64/48 pins) PH2: IRQ1 (100/64/48 pins)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PH1: IRQ0 input switch (100/80/64/48 pins) PH2: IRQ1 input switch (100/80/64/48 pins)
PJnPFS	ASEL	—	Analog Function Select 0: Used as a pin other than an analog pin 1: Used as an analog pin PJ6: VREFH0 PJ7:VREFL0
PFCSE		CS Output Enable Register	—
PFAOE0		Address Output Enable Register 0	—
PFAOE1		Address Output Enable Register 1	—
PFBCR0		External Bus Control Register 0	—
PFBCR1		External Bus Control Register 1	—

2.16 Port Output Enable 2

Table 2.32 shows a comparative overview of the port output enable 2 specifications.

Table 2.32 Comparative Overview of Port Output Enable 2 Specifications

Item	RX230/RX231 (POE2a)	RX130 (POE2a)
High-impedance is controlled by the input level detection	• Falling-edge detection or sampling of the low level 16 times at PCLK/8, PCLK/16, or PCLK/128 clock cycles can be set for each of the POE0# to POE3# and POE8# input pins. • Pins for complementary PWM output from the MTU can be placed in the high-impedance on detection of falling edges or sampling of the low level on the POE0# to POE3# pins. • Pins for output from MTU0 can be placed in the high-impedance on detection of falling edges or sampling of the low level on the POE8# pin.	• Falling-edge detection or sampling of the low level 16 times at PCLK/8, PCLK/16, or PCLK/128 clock cycles can be set for each of the POE0# to POE3# and POE8# input pins. • Pins for complementary PWM output from the MTU can be placed in the high-impedance on detection of falling edges or sampling of the low level on the POE0# to POE3# pins. • Pins for output from MTU0 can be placed in the high-impedance on detection of falling edges or sampling of the low level on the POE8# pin.
High-impedance is controlled by the output level comparison	Levels output on pins for complementary PWM output from the MTU are compared, and when simultaneous output of the active level continues for one or more clock cycles, the pins can be placed in the high-impedance.	Levels output on pins for complementary PWM output from the MTU are compared, and when simultaneous output of the active level continues for one or more clock cycles, the pins can be placed in the high-impedance.
High-impedance is controlled by the oscillation stop detection	Pins for complementary PWM output from the MTU and output pins for MTU0 can be placed in the high-impedance when oscillation by the clock generation circuit stops.	Pins for complementary PWM output from the MTU and output pins for MTU0 can be placed in the high-impedance when oscillation by the clock generation circuit stops.
High-impedance is controlled by software (registers)	Pins for complementary PWM output from the MTU and output pins for MTU0 can be placed in the high-impedance by modifying settings of POE registers.	Pins for complementary PWM output from the MTU and output pins for MTU0 can be placed in the high-impedance by modifying settings of POE registers.
High-impedance is controlled by the event signal	Pins for complementary PWM output from the MTU and output pins for MTU0 can be placed in the high-impedance in response to an event signal from the event link controller (ELC).	—
Interrupts	Interrupts can be generated in response to the results of POE0# to POE3# and POE8# inputlevel detection and MTU complementary PWM output-level comparison.	Interrupts can be generated in response to the results of POE0# to POE3# and POE8# inputlevel detection and MTU complementary PWM output-level comparison.

2.17 8-Bit Timer

Table 2.33 shows a comparative overview of the 8-Bit Timer specifications.

Table 2.33 Comparative Overview of 8-Bit Timer Specifications

Item	RX230/RX231 (TMR)	RX130 (TMR)
Count clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192 • External clock: external count clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192 • External clock: external count clock
Number of channels	(8 bits × 2 channels) × 2 units	(8 bits × 2 channels) × 2 units
Compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selected by compare match A or B, or an external counter reset signal.	Selected by compare match A or B, or an external counter reset signal.
Timer output	Output pulses with a desired duty cycle or PWM output	Output pulses with a desired duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (Output)	Compare match A, compare match B, and overflow (TMR0, TMR2)	Compare match A, compare match B, and overflow (TMR0, TMR2)
Event link function (Input)	One of the following three operations proceeds in response to an event reception: (1) Counting start operation (TMR0, TMR2) (2) Event counting operation (TMR0, TMR2) (3) Counting restart operation (TMR0, TMR2)	One of the following three operations proceeds in response to an event reception: (1) Counting start operation (TMR0, TMR2) (2) Event counting operation (TMR0, TMR2) (3) Counting restart operation (TMR0, TMR2)
DTC activation	DTC can be activated by compare match A interrupts or compare match B interrupts.	DTC can be activated by compare match A interrupts or compare match B interrupts.
Capable of generating baud rate clock for SCI	Generates baud rate clock for SCI.	Generates baud rate clock for SCI.
Capable of generating receive clock for REMC	—	Generates operating clock for remote control signal receiver (REMC)
Low power consumption function	Each unit can be placed in a module stop state	Each unit can be placed in a module stop state

2.18 Compare Match Timer

Table 2.34 shows a comparative overview of the compare match timer specification, and Table 2.35 shows a comparative listing of the compare match timer registers.

Table 2.34 Comparative Overview of Compare Match Timer Specifications

Item	RX230/RX231 (CMT)	RX130 (CMT)
Number of units	2 units	1 unit
Number of channels	4 channels	2 channels
Count clocks	Four frequency-divided clocks One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected independently for each channel.	Four frequency-divided clocks One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.
Interrupt	A compare match interrupt can be requested independently for each channel.	A compare match interrupt can be requested for each channel.
Event link function (output)	Event signal output at CMT1 compare match	Event signal output at CMT1 compare match
Event link function (input)	• Support for linked operation of specified module • Support for CMT1 counter start, event counter, and count restart	• Support for linked operation of specified module • Support for CMT1 counter start, event counter, and count restart
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.

Table 2.35 Comparative Listing of Compare Match Timer Registers

Register	Bit	RX230/RX231 (CMT)	RX130 (CMT)
CMSTR1	—	Compare match timer start register 1	—

2.19 Realtime Clock

Table 2.36 shows a comparative overview of the realtime clock specifications, and Table 2.37 shows a comparative listing of the realtime clock registers.

Table 2.36 Comparative Overview of Realtime Clock Specifications

Item	RX230/RX231 (RTCe)	RX130 (RTCc)
Count modes	Calendar count mode, binary count mode	Calendar count mode, binary count mode
Count source	Sub-clock (XCIN)	Sub-clock (XCIN)
Clock and calendar functions	• Calendar count mode — Year, month, date, day of the week, hours, minutes, and seconds are counted and represented in BCD format — Selection of 12- or 24-hour mode — 30-second adjustment (30 seconds or less are rounded down to 00 seconds, and 30 seconds or more are rounded up to one minute.) — Automatic leap year adjustment • Binary count mode 32-bit counting and binary display of seconds • Common to both modes — Start/stop function — Binary display of digits below seconds (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, 64 Hz) — Time error adjustment function — Clock (1 Hz/64 Hz) output	• Calendar count mode — Year, month, date, day of the week, hours, minutes, and seconds are counted and represented in BCD format — Selection of 12- or 24-hour mode — 30-second adjustment (30 seconds or less are rounded down to 00 seconds, and 30 seconds or more are rounded up to one minute.) — Automatic leap year adjustment • Binary count mode 32-bit counting and binary display of seconds • Common to both modes — Start/stop function — Binary display of digits below seconds (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, 64 Hz) — Time error adjustment function — Clock (1 Hz/64 Hz) output
Interrupt	• Alarm interrupt (ALM) Any of the following can be selected as conditions for the alarm interrupt: — Calendar count mode: Year, month, date, day of the week, hours, minutes, and seconds — Binary count mode: Each bit of 32-bit binary counter • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as the interrupt period. • Carry interrupt (CUP) Generates interrupt requests at either of the following times: — At occurrence of a carry to the seconds counter from the 64 Hz counter — At coincidence of a change in the 64 Hz counter and read access to the R64CNT register	• Alarm interrupt (ALM) Any of the following can be selected as conditions for the alarm interrupt: — Calendar count mode: Year, month, date, day of the week, hours, minutes, and seconds — Binary count mode: Each bit of 32-bit binary counter • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as the interrupt period. • Carry interrupt (CUP) Generates interrupt requests at either of the following times: — At occurrence of a carry to the seconds counter from the 64 Hz counter — At coincidence of a change in the 64 Hz counter and read access to the R64CNT register

Item	RX230/RX231 (RTCe)	RX130 (RTCc)
Interrupt	• Recovery from software standby mode can be performed by an alarm interrupt or periodic interrupt	• Recovery from software standby mode can be performed by an alarm interrupt or periodic interrupt
Time-capture function	Time capture using edge detection on the time capture event input pin is available. At each input event the month, date, hour, minute, and second is captured, or the 32 -bit counter value is captured.	—
Event link function	Periodic event output	—

Table 2.37 Comparative Listing of Realtime Clock Registers

Register	Bit	RX230/RX231 (RTCe)	RX130 (RTCc)
RTCCRy	—	Time capture control register y (y = 0 to 2)	—
RSECCPy	—	Second capture register y (y = 0 to 2)	—
BCNT0CPy	—	BCNT0 capture register y (y = 0 to 2)	—
RMINCPy	—	Minute capture register y (y = 0 to 2)	—
BCNT1CPy	—	BCNT1 capture register y (y = 0 to 2)	—
RHRCPy	—	Hour capture register y (y = 0 to 2)	—
BCNT2CPy	—	BCNT2 capture register y (y = 0 to 2)	—
RDAYCPy	—	Date capture register y (y = 0 to 2)	—
BCNT3CPy	—	BCNT3 capture register y (y = 0 to 2)	—
RMONCPy	—	Month capture register y (y = 0 to 2)	—

2.20 Independent Watchdog Timer

Table 2.38 shows a comparative overview of the independent watchdog timer specifications.

Table 2.38 Comparative Overview of Independent Watchdog Timer Specifications

Item	RX230/RX231 (IWDTa)	RX130 (IWDTa)
Count source	IWDT-dedicated clock (IWDTCLK)	IWDT-dedicated clock (IWDTCLK)
Clock divide ratio	Divide by 1, 16, 32, 64, 128, or 256	Divide by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Counting automatically starts after a reset (auto-start mode) • Counting is started (register start mode) by refreshing the counter (writing 00h and then FFh to the IWDTRR register).	• Counting automatically starts after a reset (auto-start mode) • Counting is started (register start mode) by refreshing the counter (writing 00h and then FFh to the IWDTRR register).
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error occurs • Counting restarts (In auto-start mode, counting automatically restarts after a reset or after a nonmaskable interrupt request is output. In register start mode, counting restarts after refreshing.)	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error occurs • Counting restarts (In auto-start mode, counting automatically restarts after a reset or after a nonmaskable interrupt request is output. In register start mode, counting restarts after refreshing.)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Reset output sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by the IWDTSR register.	Reading the counter value
Event link function (output)	• Down-counter underflow event output • Refresh error event output	—
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep mode count stop control output	• Reset output • Interrupt request output • Sleep mode count stop control output

Item	RX230/RX231 (IWDTa)	RX130 (IWDTa)
Auto-start mode (controlled by option function select register 0 (OFS0))	• Selecting the clock frequency divide ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (OFS0.IWDTSLCSTP bit)	• Selecting the clock frequency divide ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (OFS0.IWDTSLCSTP bit)
Register start mode (controlled by the IWDT registers)	• Selecting the clock frequency divide ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (IWDTCSTPR.SLCSTP bit)	• Selecting the clock frequency divide ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (IWDTCSTPR.SLCSTP bit)

2.21 Serial Peripheral Interface

Table 2.39 shows a comparative overview of the serial peripheral interface specifications.

Table 2.39 Comparative Overview of Serial Peripheral Interface Specifications

Item	RX230/RX231 (RSPIa)	RX130 (RSPIa)
Number of channels	1 channel	1 channel
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communication through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK is supported. • Switching of the phase of RSPCK is supported.	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communication through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK is supported. • Switching of the phase of RSPCK is supported.
Data format	• Selectable between MSB-first and LSB-first. • Transfer bit length is selectable among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (with each frame consisting of up to 32 bits).	• Selectable between MSB-first and LSB-first. • Transfer bit length is selectable among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (with each frame consisting of up to 32 bits).
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from 2 to 4096). • In slave mode, the minimum PCLK clock divided by 8 can be input as RSPCK (the maximum frequency of RSPCK is PCLK divided by 8). Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from 2 to 4096). • In slave mode, the minimum PCLK clock divided by 8 can be input as RSPCK (the maximum frequency of RSPCK is PCLK divided by 8). Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK
Buffer configuration	• The transmit and receive buffers have a double buffer configuration. • The transmit and receive buffers are each 128 bits in size.	• The transmit and receive buffers have a double buffer configuration. • The transmit and receive buffers are each 128 bits in size.
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection • Parity error detection

Item	RX230/RX231 (RSPIa)	RX130 (RSPIa)
SSL control function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin is input, and SSLA1 to SSLA3 pins are either output or unused. • In slave mode: SSLA0 pin is input, and SSLA1 to SSLA3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • SSL polarity-change function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin is input, and SSLA1 to SSLA3 pins are either output or unused. • In slave mode: SSLA0 pin is input, and SSLA1 to SSLA3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • SSL polarity-change function
Control in master transfer	• Transfers of up to eight commands can be performed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, LSB/MSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value when SSL is negated can be specified. • RSPCK auto-stop function	• Transfers of up to eight commands can be performed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, LSB/MSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value when SSL is negated can be specified. • RSPCK auto-stop function
Interrupt sources	Interrupt sources: • Receive buffer full interrupt • transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, parity error) • RSPI idle interrupt (RSPI idle)	Interrupt sources: • Receive buffer full interrupt • transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, parity error) • RSPI idle interrupt (RSPI idle)
Event link function (output)	The following events can be output to the event link controller (RSPI0): • Receive buffer full event signal • Transmit buffer empty event signal • Mode fault, overrun, or parity error event signal • RSPI idle event signal • Transmit end event signal	—

Item	RX230/RX231 (RSPIa)	RX130 (RSPIa)
Other functions	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode function	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode function
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.

2.22 Capacitive Touch Sensing Unit

Table 2.40 shows a comparative overview of the capacitive touch sensing unit specifications, and Table 2.41 shows a comparative listing of the capacitive touch sensing unit registers.

Table 2.40 Comparative Overview of Capacitive Touch Sensing Unit Specifications

Item		RX230/RX231 (CTSU)	RX130 (CTSUa)
Operating clock		PCLK, PCLK/2, or PCLK/4	PCLK, PCLK/2, or PCLK/4
Pins		TS0 to TS9, TS12, TS13, TS15 to TS20, TS22, TS23, TS27, TS30, TS33, TS35: Electrostatic capacitance measurement pins (24 channels)	TS0 to TS35: Electrostatic capacitance measurement pins (36 channels)
		TSCAP: Low-pass filter (LPF) connection pin	TSCAP: Low-pass filter (LPF) connection pin
Measurement modes	Self-capacitance single scan mode	Electrostatic capacitance on a channel is measured by the self-capacitance method.	Electrostatic capacitance on a channel is measured by the self-capacitance method.
	Self-capacitance multi-scan mode	Electrostatic capacitance on multiple channels is measured successively by the self-capacitance method.	Electrostatic capacitance on multiple channels is measured successively by the self-capacitance method.
	Mutual capacitance full scan mode	Electrostatic capacitance on multiple channels is measured successively by the mutual capacitance method.	Electrostatic capacitance on multiple channels is measured successively by the mutual capacitance method.
Noise prevention		Synchronous noise prevention, high-range noise prevention	Synchronous noise prevention, high-range noise prevention
Measurement start conditions		• Software trigger • External trigger (event input by the event link controller (ELC))	• Software trigger • External trigger (event input by the event link controller (ELC))

Table 2.41 Comparative Listing of Capacitive Touch Sensing Unit Registers

Register	Bit	RX230/RX231 (CTSU)	RX130 (CTSUa)
CTSUCR0	CTSUTXVSEL	—	CTSU transmission power supply select bit
CTSUMCH0	CTSUMCH0[5:0]	CTSU measurement channel 0 bits • Self-capacitance single scan mode b5 b0 0 0 0 0 0 0: TS0 : 0 0 1 0 0 1: TS9 0 0 1 1 0 0: TS12 0 0 1 1 0 1: TS13 0 0 1 1 1 1: TS15 : 0 1 0 1 0 0: TS20 0 1 0 1 1 0: TS22 0 1 0 1 1 1: TS23 0 1 1 0 1 1: TS27 0 1 1 1 1 0: TS30 1 0 0 0 0 1: TS33 1 0 0 0 1 1: TS35 Other than above: Starting measurement operation (CTSUCR0.CTSUSTRT bit = 1) is prohibited after these bits are set. • Modes other than self-capacitance single scan b5 b0 0 0 0 0 0 0: TS0 : 0 0 1 0 0 1: TS9 0 0 1 1 0 0: TS12 0 0 1 1 0 1: TS13 0 0 1 1 1 1: TS15 : 0 1 0 1 0 0: TS20 0 1 0 1 1 0: TS22 0 1 0 1 1 1: TS23 0 1 1 0 1 1: TS27 0 1 1 1 1 0: TS30 1 0 0 0 0 1: TS33 1 0 0 0 1 1: TS35 1 1 1 1 1 1: Measurement is stopped.	CTSU measurement channel 0 bits • Self-capacitance single scan mode b5 b0 0 0 0 0 0 0: TS0 : 1 0 0 0 1 1: TS35 Other than above: Starting measurement operation (CTSUCR0.CTSUSTRT bit = 1) is prohibited after these bits are set. • Modes other than self-capacitance single scan b5 b0 0 0 0 0 0 0: TS0 : 1 0 0 0 1 1: TS35 1 1 1 1 1 1: Measurement is stopped.

Register	Bit	RX230/RX231 (CTSU)	RX130 (CTSUa)
CTSUMCH1	CTSUMCH1[5:0]	CTSU measurement channel 1 bits b5 b0 0 0 0 0 0 0: TS0 : 0 0 1 0 0 1: TS9 0 0 1 1 0 0: TS12 0 0 1 1 0 1: TS13 0 0 1 1 1 1: TS15 : 0 1 0 1 0 0: TS20 0 1 0 1 1 0: TS22 0 1 0 1 1 1: TS23 0 1 1 0 1 1: TS27 0 1 1 1 1 0: TS30 1 0 0 0 0 1: TS33 1 0 0 0 1 1: TS35 1 1 1 1 1 1: Measurement is stopped.	CTSU measurement channel 1 bits b5 b0 0 0 0 0 0 0: TS0 : 1 0 0 0 1 1: TS35 1 1 1 1 1 1: Measurement is stopped.
CTSUTRMR	—	—	CTSU reference voltage adjustment register

2.23 12-Bit A/D Converter

Table 2.42 shows a comparative overview of the 12-bit A/D converter specifications.

Table 2.42 Comparative Overview of 12-Bit A/D Converter

Item	RX230/RX231 (S12ADE)	RX130 (S12ADE)
Number of units	1 unit	1 unit
Input channels	24 channels	24 channels
Extended analog function	Temperature sensor output, internal reference voltage	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	0.83 µs per channel (when operating with A/D conversion clock ADCLK = 54 MHz)	1.4 µs per channel (when operating with A/D conversion clock ADCLK = 32 MHz)
A/D conversion clock	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio is one of the following: PCLK: ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.	Peripheral module clock PCLK*1 and A/D conversion clock ADCLK*1 can be set so that the frequency ratio is one of the following: PCLK: ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.
Data register	• For analog input: 24 data registers • One data register for each unit for A/D conversion data multiplexing in double trigger mode • For temperature sensor: One data register • For internal reference voltage: One data register • 1 register per unit for self-diagnostics • The results of A/D conversion are stored in 12-bit A/D data registers. • Output of A/D conversion results at 12-bit precision • The value obtained by adding up A/D-converted results is stored as a value (number of conversion accuracy bits + 2 bits/4 bits) in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes) • The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.	• For analog input: 24 data registers • One data register for each unit for A/D conversion data multiplexing in double trigger mode • For temperature sensor: One data register • For internal reference voltage: One data register • 1 register per unit for self-diagnostics • The results of A/D conversion are stored in 12-bit A/D data registers. • Output of A/D conversion results at 12-bit precision • The value obtained by adding up A/D-converted results is stored as a value (number of conversion accuracy bits + 2 bits/4 bits) in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes) • The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.

Item	RX230/RX231 (S12ADE)	RX130 (S12ADE)
Operating mode	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up To 24 user-selected channels. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of up to 24 user-selected channels. • Group scan mode: — Up to 24 channels of analog input are divided between group A and group B, and A/D conversion is performed only once on all the channels in the selected group. — The scanning start conditions (synchronous triggers) can be selected independently for group A and group B allowing conversion to start at a different time for each group. • Group scan mode (with group A priority control selected): — If a group A trigger is input when A/D conversion on group B is in progress, scanning of group B is stopped and scanning of group A starts. — Restart of A/D conversion on group B (rescan) after completion of A/D conversion on group A can be enabled.	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 24 user-selected channels. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of up to 24 user-selected channels. • Group scan mode: — Up to 24 channels of analog input are divided between group A and group B, and A/D conversion is performed only once on all the channels in the selected group. — The scanning start conditions (synchronous triggers) can be selected independently for group A and group B allowing conversion to start at a different time for each group. • Group scan mode (with group A priority control selected): — If a group A trigger is input when A/D conversion on group B is in progress, scanning of group B is stopped and scanning of group A starts. — Restart of A/D conversion on group B (rescan) after completion of A/D conversion on group A can be enabled.
A/D conversion start conditions	• Software trigger • Synchronous trigger Conversion start is triggered by the multi-function timer pulse unit (MTU), event link controller (ELC), and 16-bit timer pulse unit (TPU). • Asynchronous trigger A/D conversion can be triggered by the ADTRG0# pin.	• Software trigger • Synchronous trigger Conversion start is triggered by the multi-function timer pulse unit (MTU) and event link controller (ELC). • Asynchronous trigger A/D conversion can be started by the external trigger ADTRG0# pin.

Item	RX230/RX231 (S12ADE)	RX130 (S12ADE)
Functions	• Variable sampling state count • Self-diagnostic function for 12-bit A/D converter • Selectable A/D-converted value adding mode or averaging mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • A/D data register auto-clear function • Compare function (window A, window B) • Ring buffers (16) for compare function	• Variable sampling state count • Self-diagnostic function for 12-bit A/D converter • Selectable A/D-converted value adding mode or averaging mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • A/D data register auto-clear function • Compare function (window A, window B) • Ring buffers (16) for compare function
Interrupt sources	• In modes other than double trigger mode and group scan mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of a single scan. • In double trigger mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of a double scan. • In group scan mode, a scan end interrupt request (S12ADI0) can be generated on completion of a group A scan. On completion of a group B scan a dedicated group B scan end interrupt request (GBADI) can be generated. • When double trigger mode is selected in group scan mode, a scan end interrupt request (S12ADI0) can be generated on completion of two scans of group A. On completion of a group B scan a dedicated scan end interrupt request (GBADI) can be generated. • The DMA controller (DMAC) or data transfer controller (DTC) can be activated by the S12ADI0 or GBADI interrupt.	• In modes other than double trigger mode and group scan mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of a single scan. • In double trigger mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of a double scan. • In group scan mode, a scan end interrupt request (S12ADI0) can be generated on completion of a group A scan. On completion of a group B scan a dedicated group B scan end interrupt request (GBADI) can be generated. • When double trigger mode is selected in group scan mode, a scan end interrupt request (S12ADI0) can be generated on completion of two scans of group A. On completion of a group B scan a dedicated scan end interrupt request (GBADI) can be generated. • The data transfer controller (DTC) can be activated by the S12ADI0 or GBADI interrupt.
Event link function	• In group scan mode an ELC event can be generated on completion of scans other than group B scan. • An ELC event can be generated on completion of group B scan in group scan mode. • An ELC event can be generated at end of all scans. • Scanning can be started by a trigger from the ELC. • An ELC event can be generated according to the window compare function event conditions in single scan mode.	• In group scan mode an ELC event can be generated on completion of scans other than group B scan. • An ELC event can be generated on completion of group B scan in group scan mode. • An ELC event can be generated at end of all scans. • Scanning can be started by a trigger from the ELC. • An ELC event can be generated according to the window compare function event conditions in single scan mode.

Item	RX230/RX231 (S12ADE)	RX130 (S12ADE)
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.

2.24 D/A Converter

Table 2.43 shows a comparative overview of the D/A converter specifications, and Table 2.44 shows a comparative listing of the D/A converter registers.

Table 2.43 Comparative Overview of D/A Converter Specifications

Item	RX230/RX231 (R12DAA)	RX130 (DAa)
Resolution	12 bits	8 bits
Output channel	2 channels	2 channels
Measure against mutual interference between analog modules	Measure against interference between D/A and A/D conversion: D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable input signal output by the the 12-bit A/D converter. Degradation of 12-bit A/D conversion accuracy caused by interference is reduced by controlling the D/A converter inrush current generation timing with the enable signal.	Measure against interference between D/A and A/D conversion: D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable input signal output by the the 12-bit A/D converter. Degradation of 8-bit A/D conversion accuracy caused by interference is reduced by controlling the D/A converter inrush current generation timing with the enable signal.
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.
Event link function (input)	Ability to activate DA0 by event signal input	Ability to activate DA0 by event signal input

Table 2.44 Comparative Listing of D/A Converter Registers

Register	Bit	RX230/RX231 (R12DAA)	RX130 (DAa)
DADRm	—	D/A data register m (m = 0, 1) The DADRm register is a 16-bit readable/writable register that stores data on which D/A conversion is to be performed. When analog output is enabled, the values in the DADRm register are converted and output on the analog output pins. 12-bit data can be relocated by setting the DPSEL bit in DADPR. Bits designated as "—" are read as 0, and the write value should be 0.	D/A data register m (m = 0, 1) The DADRm register is a 16-bit readable/writable register that stores data on which D/A conversion is to be performed. When analog output is enabled, the values in the DADRm register are converted and output on the analog output pins. 8-bit data can be relocated by setting the DPSEL bit in DADPR. Bits designated as "—" are read as 0, and the write value should be 0.
DAADSCR	DAADST	D/A A/D synchronous conversion bit 0: 12-bit D/A converter operation is not synchronized with 12-bit A/D converter operation. (Measures against interference between D/A and A/D conversion are disabled.) 1: 12-bit D/A converter operation is synchronized with 12-bit A/D converter operation. (Measures against interference between D/A and A/D conversion are enabled.)	D/A A/D synchronous conversion bit 0: 8-bit D/A converter operation is not synchronized with 12-bit A/D converter operation. (Measures against interference between D/A and A/D conversion are disabled.) 1: 8-bit D/A converter operation is synchronized with 12-bit A/D converter operation. (Measures against interference between D/A and A/D conversion are enabled.)
DAVREFCR	—	D/A VREF control register	—

2.25 Comparator B

Table 2.45 shows a comparative overview of the comparator B specifications, and Table 2.46 shows a comparative listing of the comparator B registers.

Table 2.45 Comparative Overview of Comparator B Specifications

Item	RX230/RX231 (CMPBa)	RX130 (CMPBa)
Channels	Comparator B0 Comparator B1 Comparator B2 Comparator B3	Comparator B0 Comparator B1
Analog input voltage	Voltage input on the CMPBn pin (n = 0 to 3)	Analog input voltage: Voltage input on the CMPBn pin (n = 0, 1)
Reference input voltage	Voltage input on the CVREFBn pin (n = 0 to 3) or internal reference voltage	Reference input voltage: Voltage input on the CVREFBn pin (n = 0, 1) or internal reference voltage
Comparison result	Read from CPBFLG.CPBnOUT flag (n = 0 to 3). The comparison result can be output on the CMPOBn pin (n = 0 to 3).	Read from CPBFLG.CPBnOUT flag (n = 0, 1). The comparison result can be output on the CMPOBn pin (n = 0, 1).
Interrupt request generation timing	When comparator B0 comparison result changes When comparator B1 comparison result changes When comparator B2 comparison result changes When comparator B3 comparison result changes	When comparator B0 comparison result changes When comparator B1 comparison result changes
Event generation timing to ELC	When comparator B0 comparison result changes When comparator B0 or comparator B1 comparison result changes	When comparator B0 comparison result changes When comparator B0 or comparator B1 comparison result changes
Selectable functions	• Digital filter function Whether the digital filter is applied or not, and the sampling frequency, can be selected. • Window function Whether the window function is enabled or disabled (low-side reference (VRFL)) < CMPBn (n = 0 to 3) < high-side reference (VRFH)) can be selected. • Reference input voltage CVREFBn pin input or internal reference voltage (generated internally) can be selected (n = 0 to 3). • Comparator B response speed High-speed mode or low-speed mode can be selected.	• Digital filter function Whether the digital filter is applied or not, and the sampling frequency, can be selected. • Window function Whether the window function is enabled or disabled (low-side reference (VRFL)) < CMPBn (n = 0, 1) < high-side reference (VRFH)) can be selected. • Reference input voltage CVREFBn pin input or internal reference voltage (generated internally) can be selected (n = 0, 1). • Comparator B response speed High-speed mode or low-speed mode can be selected.
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.

Table 2.46 Comparative Listing of Comparator B Registers

Register	Bit	RX230/RX231 (CMPBa)	RX130 (CMPBa)
CPB1CNT1	—	Comparator B1 control register 1	—
CPB1CNT2	—	Comparator B1 control register 2	—
CPB1FLG	—	Comparator B1 flag register	—
CPB1INT	—	Comparator B1 interrupt control register	—
CPB1F	—	Comparator B1 filter select register	—
CPB1MD	—	Comparator B1 mode select register	—
CPB1REF	—	Comparator B1 reference input voltage select register	—
CPB1OCR	—	Comparator B1 output control register	—

2.26 RAM

Table 2.47 shows a comparative overview of the RAM.

Table 2.47 Comparative Overview of RAM

Item	RX230/RX231	RX130
RAM capacity	64 KB or 32 KB	48KB, 32KB, 16 KB or 10 KB
RAM address	0000 0000h to 0000 FFFFh (64 KB) 0000 0000h to 0000 7FFFh (32 KB)	0000 0000h to 0000 BFFFh (48 KB) 0000 0000h to 0000 7FFFh (32 KB) 0000 0000h to 0000 3FFFh (16 KB) 0000 0000h to 0000 27FFh (10 KB)
Access	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.
Low power consumption function	It is possible to specify for RAM0 the module stop state.	It is possible to specify the module stop state.

2.27 Flash Memory (ROM)

Table 2.48 shows a comparative listing of the flash memory specifications, and Table 2.49 shows a comparative listing of the flash memory registers.

Table 2.48 Comparative Listing of Flash Memory Specifications

Item	RX230/RX231	RX130
Memory space	• User area: Max. 256 KB (RX230) Max. 512 KB (RX231) • Data area: 8 KB • Extra area: Stores the start-up area information, access window information, and unique ID.	• User area: Max. 512 KB • Data area: 8 KB • Extra area: Stores the start-up area information, access window information, and unique ID.
Software commands	• The following commands are implemented: Program, blank check, block erase, all-block erase • The following commands are implemented for programming the extra area: Program start-up area information, program access window information	• The following commands are implemented: Program, blank check, block erase, unique ID read • The following commands are implemented for programming the extra area: Program start-up area information, program access window information
Value after erase	• ROM: FFh • E2 data flash: FFh	• ROM: FFh • E2 data flash: FFh
Interrupt	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.

Item	RX230/RX231	RX130
On-board programming	Boot mode (SCI interface) • Channel 1 of the serial communications interface (SCI1) is used for asynchronous serial communication. • The user area and data area are rewritable. • Boot mode (FINE interface) • The FINE is used. • The user area and data area are rewritable. Boot mode (USB interface)*1 • Channel 0 of the USB 2.0 Function (USB0) module is used. • The user area and data area are rewritable. • The flash memory can be rewritten in self-powered or bus-powered mode. • A personal computer can be connected using only a USB cable. Self-programming (single-chip mode) • The user area and data area are rewritable using a flash rewrite routine in a user program.	Boot mode (SCI interface) • Channel 1 of the serial communications interface (SCI1) is used for asynchronous serial communication. • The user area and data area are rewritable. • Boot mode (FINE interface) • The FINE is used. • The user area and data area are rewritable. Self-programming (single-chip mode) • The user area and data area are rewritable using a flash rewrite routine in a user program.
Off-board programming	The user area and data area are rewritable using a flash programmer (serial programmer or parallel programmer) compatible with the MCU.	The user area and data area are rewritable using a flash programmer compatible with the MCU.
ID code protect	• Connection with the serial programmer can be enabled or disabled using ID codes in boot mode. • Connection with an on-chip debugging emulator can be enabled or disabled using ID codes. • Connection with a parallel programmer can be enabled or disabled using ROM codes.	• Connection with the serial programmer can be enabled or disabled using ID codes in boot mode. • Connection with an on-chip debugging emulator can be enabled or disabled using ID codes.
Start-up program protection function	This function is used to safely rewrite blocks 0 to 7.	This function is used to safely rewrite blocks 0 to 15.
Area protection	This function enables rewriting of only the specified range in the user area and disables rewriting of the other blocks during self-programming.	This function enables rewriting of only the specified range in the user area and disables rewriting of the other blocks during self-programming.
Background operation (BGO) function	Programs in the ROM can be executed while rewriting the E2 data flash.	Programs in the ROM can be executed while rewriting the E2 data flash.

Note 1. Implemented on the RX231 Group only. Not implemented on the RX230 Group.

Table 2.49 Comparative Listing of Flash Memory Registers

Register	Bit	RX230/RX231	RX130
FCR	DRC	—	Data read completion bit
	CMD[3:0]	Software command setting bits b3 b0 0 0 0 1: Program 0 0 1 1: Blank check 0 1 0 0: Block erase 0 1 1 0: All-block erase Settings other than the above are prohibited.	Software command setting bits b3 b0 0 0 0 1: Program 0 0 1 1: Blank check 0 1 0 0: Block erase 0 1 0 1: Unique ID read Settings other than the above are prohibited.
FSARH	—	Flash processing start address register H This register is used to set the target processing address or the start address of the target processing range in the flash memory when a software command is executed. Set bits 31 to 25 or bits 20 to 16 of the flash memory address for programming or erasure in this register. Data can be written to this register in ROM P/E mode or E2 data flash P/E mode. This register is initialized by a reset or setting the FRESET bit in FRESETR to 1. Data cannot be written to this register while the value of the FRESET bit in FRESETR is 1. If this register is read while executing a software command set by the FEXCR register, an undefined value is read.	Flash processing start address register H This register is used to set the target processing address or the start address of the target processing range in the flash memory when a software command is executed. Set bits 19 to 16 of the flash memory address for programming or erasure in this register. Data can be written to this register in ROM P/E mode or E2 data flash P/E mode. This register is initialized by a reset or setting the FRESET bit in FRESETR to 1. Data cannot be written to this register while the value of the FRESET bit in FRESETR is 1. If this register is read while executing a software command set by the FEXCR register, an undefined value is read.

Register	Bit	RX230/RX231	RX130
FSARL	—	Flash processing start address register L This register is used to set the target processing address or the start address of the target processing range in the flash memory when a software command is executed. Set bits 15 to 0 of the flash memory address for programming or erasure in this register. To set the ROM area, set bits 2 to 0 to 000b. Data can be written to this register in ROM P/E mode or E2 data flash P/E mode. This register is initialized by a reset or setting the FRESET bit in FRESETR to 1. Data cannot be written to this register while the value of the FRESET bit in FRESETR is 1. After a program command is executed, the value set in this register is incremented by 8h if the code flash area is specified and 1h if the data flash area is specified. Therefore, it is not necessary to specify the target write address in this register when executing program commands sequentially. If this register is read while executing a software command set by the FEXCR register, an undefined value is read.	Flash processing start address register L This register is used to set the target processing address or the start address of the target processing range in the flash memory when a software command is executed. Set bits 15 to 0 of the flash memory address for programming or erasure in this register. To set the ROM area, set bits 1 and 0 to 00b. Data can be written to this register in ROM P/E mode or E2 data flash P/E mode. This register is initialized by a reset or setting the FRESET bit in FRESETR to 1. Data cannot be written to this register while the value of the FRESET bit in FRESETR is 1. If this register is read while executing a software command set by the FEXCR register, an undefined value is read.

Register	Bit	RX230/RX231	RX130
FEARH	—	Flash processing end address register H This register is used to set the end address of the target processing range in the flash memory when a software command is executed. Set bits 31 to 25 or bits 20 to 16 of the flash memory address for programming or erasure in this register. Data can be written to this register in ROM P/E mode or E2 data flash P/E mode. This register is initialized by a reset or setting the FRESET bit in FRESETR to 1. Data cannot be written to this register while the value of the FRESET bit in FRESETR is 1. If this register is read while executing a software command set by the FEXCR register, an undefined value is read.	Flash processing end address register H This register is used to set the end address of the target processing range in the flash memory when a software command is executed. Set bits 19 to 16 of the flash memory address for programming or erasure in this register. Data can be written to this register in ROM P/E mode or E2 data flash P/E mode. This register is initialized by a reset or setting the FRESET bit in FRESETR to 1. Data cannot be written to this register while the value of the FRESET bit in FRESETR is 1. If this register is read while executing a software command set by the FEXCR register, an undefined value is read.
FEARL	—	Flash processing end address register L This register is used to set the target processing address or the start address of the target processing range in the flash memory when a software command is executed. Set bits 15 to 0 of the flash memory address for programming or erasure in this register. To set the ROM area, set bits 2 to 0 to 000b. Data can be written to this register in ROM P/E mode or E2 data flash P/E mode. This register is initialized by a reset or setting the FRESET bit in FRESETR to 1. Data cannot be written to this register while the value of the FRESET bit in FRESETR is 1. If this register is read while executing a software command set by the FEXCR register, an undefined value is read.	Flash processing end address register L This register is used to set the target processing address or the start address of the target processing range in the flash memory when a software command is executed. Set bits 15 to 0 of the flash memory address for programming or erasure in this register. To set the ROM area, set bits 1 and 0 to 00b. Data can be written to this register in ROM P/E mode or E2 data flash P/E mode. This register is initialized by a reset or setting the FRESET bit in FRESETR to 1. Data cannot be written to this register while the value of the FRESET bit in FRESETR is 1. If this register is read while executing a software command set by the FEXCR register, an undefined value is read.
FRBH	—	—	Flash read buffer register H
FRBL	—	—	Flash read buffer register L
FWBH	—	—	Flash write buffer register H
FWBL	—	—	Flash write buffer register L
FWBn	—	Flash write buffer n register (n = 0 to 3)	—

Register	Bit	RX230/RX231	RX130
FSTATR1	DRRDY	—	Data read ready flag
FEAMH	—	Flash error address monitor register H When an error occurs during processing of a software command, this register is used to confirm the address where the error occurred. This register stores bits 31 to 25 or bits 20 to 16 of the address where the error occurred (program command or blank check command), or it stores bits 31 to 25 or bits 20 to 16 of the beginning address of the area where the error has occurred (block erase command or all-block erase command). Since this register value becomes undefined when the FRESET bit in FRESETR is set to 1, read the value before error processing. If the software command terminates normally, this register stores bits 31 to 25 or bits 20 to 16 of the end address at execution of the command.	Flash error address monitor register H When an error occurs during processing of a software command, this register is used to confirm the address where the error occurred. This register stores bits 19 to 16 of the address where the error occurred (program command or blank check command), or it stores bits 19 to 16 of the beginning address of the area where the error has occurred (block erase command). Since this register value becomes undefined when the FRESET bit in FRESETR is set to 1, read the value before error processing. If the software command terminates normally, this register stores bits 19 to 16 of the end address at execution of the command.
FEAML	—	Flash error address monitor register L When an error occurs during processing of a software command, this register is used to confirm the address where the error occurred. This register stores bits 15 to 0 of the address where the error occurred (program command or blank check command), or it stores bits 15 to 0 of the beginning address of the area where the error has occurred (block erase command or all-block erase command). Since this register value becomes undefined when the FRESET bit in FRESETR is set to 1, read the value before error processing. If the software command terminates normally, this register stores bits 15 to 0 of the end address at execution of the command. When executing a software command for the ROM, the value of the two lowest bits becomes 00b.	Flash error address monitor register L When an error occurs during processing of a software command, this register is used to confirm the address where the error occurred. This register stores bits 15 to 0 of the address where the error occurred (program command or blank check command), or it stores bits 15 to 0 of the beginning address of the area where the error has occurred (block erase command). Since this register value becomes undefined when the FRESET bit in FRESETR is set to 1, read the value before error processing. If the software command terminates normally, this register stores bits 15 to 0 of the end address at execution of the command. When executing a software command for the ROM or the unique ID read command, the value of the two lowest bits becomes 00b.

Register	Bit	RX230/RX231	RX130
FSCMR	—	b11 Reserved bit This bit is read as 0. Writing to this bit has no effect.	b11 Reserved bit This bit is read as 1. Writing to this bit has no effect.
FAWSMR	—	Flash access window start address monitor register b11-b0 On a blank product the value is is 1. These bits are set to the same value set in bits 11 to 0 in the FWB0 register after the access window information program command is executed.	Flash access window start address monitor register b9-b0 On a blank product the value is is 1. These bits are set to the same value set in bits 9 to 0 in the FWBL register after the access window information program command is executed.
FAWEMR	—	Flash access window end address monitor register b11-b0 On a blank product the value is is 1. These bits are set to the same value set in bits 11 to 0 in the FWB1 register after the access window information program command is executed.	Flash access window end address monitor register b9-b0 On a blank product the value is is 1. These bits are set to the same value set in bits 9 to 0 in the FWBH register after the access window information program command is executed.
UIDRn	—	unique ID register n (n = 0 to 3)	unique ID register n (n = 0 to 31)

3. Comparison of Pin Functions

Comparison of pin functions and between pins for power supplies, clocks, and system control are listed below of the RX130, RX230, and RX231 groups. Items that apply only to one group or the other are indicated in **blue**. Items that are different between groups are indicated in **red**. Items that apply to both groups are indicated in **black**.

3.1 100-Pin Package

Table 3.1 lists comparison the pin functions for the 100-pin package.

Table 3.1 Comparison of Pin Functions for 100-Pin Package

100-Pin LFQPF	RX230 Group	RX231 Group	RX130 Group
1	VREFH		P06
2	P03/DA0		P03/DA0
3	VREFL		P04
4	PJ3/MTIOC3C/CTS6#/RTS6#/SS6#		PJ3/MTIOC3C/CTS6#/RTS6#/SS6#
5	VCL		VCL
6	VBATT		PJ1/MTIOC3A
7	MD/FINED		MD/FINED
8	XCIN		XCIN
9	XCOUT		XCOUT
10	RES#		RES#
11	XTAL/P37		XTAL/P37
12	VSS		VSS
13	EXTAL/P36		EXTAL/P36
14	VCC		VCC
15	P35/NMI		P35/NMI
16	P34/MTIOC0A/TMCI3/POE2#/SCK6/TS0/IRQ4		P34/MTIOC0A/TMCI3/POE2#/SCK6/IRQ4
17	P33/MTIOC0D/TMRI3/POE3#/TIOCD0/RXD6/SMISO6/SSCL6/TS1/IRQ3		P33/MTIOC0D/TMRI3/POE3#/RXD6/SMISO6/SSCL6/IRQ3
18	P32/MTIOC0C/TMO3/TIOCC0/RTCOUT/RTCIC2/TXD6/SMOSI6/SSDA6/USB0_VBUSEN/IRQ2		P32/MTIOC0C/TMO3/TXD6/SMOSI6/SSDA6/TS0/IRQ2/RTCOUT
19	P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/RTS1#/SS1#/SSISCK0/IRQ1		P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/TS1/IRQ1
20	P30/MTIOC4B/TMRI3/POE8#/RTCIC0/RXD1/SMISO1/SSCL1/AUDIO_MCLK/IRQ0/CMPOB3		P30/MTIOC4B/POE8#/TMRI3/RXD1/SMISO1/SSCL1/TS2/IRQ0
21	P27/CS3#/MTIOC2B/TMCI3/SCK1/SSIWS0/TS2/CVREFB3		P27/MTIOC2B/TMCI3/SCK1/TS3
22	P26/CS2#/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/SSIRXD0/TS3/CMPB3		P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/TS4
23	P25/CS1#/MTIOC4C/MTCLKB/TIOCA4/TS4/ADTRG0#		P25/MTIOC4C/MTCLKB/ADTRG0#
24	P24/CS0#/MTIOC4A/MTCLKA/TMRI1/TIOCB4/USB0_VBUSEN/TS5		P24/MTIOC4A/MTCLKA/TMRI1
25	P23/MTIOC3D/MTCLKD/TIOCD3/CTS0#/RTS0#/SS0#/SSISCK0/TS6		P23/MTIOC3D/MTCLKD/CTS0#/RTS0#/SS0#
26	P22/MTIOC3B/MTCLKC/TMO0/TIOCC3/SCK0/USB0_OVRCURB/AUDIO_MCLK/TS7		P22/MTIOC3B/MTCLKC/TMO0/SCK0

100-Pin LFQPF	RX230 Group	RX231 Group	RX130 Group
27	P21/MTIOC1B/TMCI0/TIOCA3/RXD0/SMISO0/SSCL0/USB0_EXICEN/SSIWS0/TS8		P21/MTIOC1B/TMCI0/RXD0/SMISO0/SSCL0
28	P20/MTIOC1A/TMRI0/TIOCB3/TXD0/SMOSI0/SSDA0/USB0_ID/SSIRXD0/TS9		P20/MTIOC1A/TMRI0/TXD0/SMOSI0/SSDA0
29	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/TIOCB0/TCLKD/SCK1/MISOA/SDA/SSITXD0/IRQ7/CMPOB2		P17/MTIOC3A/MTIOC3B/TMO1/POE8#/SCK1/MISOA/SDA/IRQ7
30	P16/MTIOC3C/MTIOC3D/TMO2/TIOCB1/TCLKC/RTCOUT/TXD1/SMOSI1/SSDA1/MOSIA/SCL/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0#		P16/MTIOC3C/MTIOC3D/TMO2/TXD1/SMOSI1/SSDA1/MOSIA/SCL/IRQ6/RTCOUT/ADTRG0#
31	P15/MTIOC0B/MTCLKB/TMCI2/TIOCB2/TCLKB/RXD1/SMISO1/SSCL1/CRXD0/TS12/IRQ5/CMPB2		P15/MTIOC0B/MTCLKB/TMCI2/RXD1/SMISO1/SSCL1/TS5/IRQ5
32	P14/MTIOC3A/MTCLKA/TMRI2/TIOCB5/TCLKA/CTS1#/RTS1#/SS1#/CTXD0/USB0_OVRCURA/TS13/IRQ4/CVREFB2		P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/RTS1#/SS1#/TS6/IRQ4
33	P13/MTIOC0B/TMO3/TIOCA5/SDA/IRQ3		P13/MTIOC0B/TMO3/SDA/IRQ3
34	P12/TMCI1/SCL/IRQ2		P12/TMCI1/SCL/IRQ2
35	PH3/TMCI0	VCC_USB	PH3/TMCI0/TS7
36	PH2/TMRI0/IRQ1	USB0_DM	PH2/TMRI0/TS8/IRQ1
37	PH1/TMO0/ IRQ0	USB0_DP	PH1/TMO0/TS9/IRQ0
38	PH0/CACREF	VSS_USB	PH0/TS10/CACREF
39	P55/WAIT#/MTIOC4D/TMO3/CRXD0/TS15		P55/MTIOC4D/TMO3/TS11
40	P54/ALE/MTIOC4B/TMCI1/CTXD0/TS16		P54/MTIOC4B/TMCI1/TS12
41	BCLK/P53/TS17		P53
42	P52/RD#/TS18		P52/PMC1
43	P51/WR1#/BC1#/WAIT#/TS19		P51/PMC0
44	P50/WR0#/WR#/TS20		P50
45	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/TXD8/SMOSI8/SSDA8/MISOA/CACREF		PC7/MTIOC3A/MTCLKB/TMO2/TXD8/SMOSI8/SSDA8/MISOA/TS13/CACREF
46	PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/RXD8/SMISO8/SSCL8/MOSIA/TS22		PC6/MTIOC3C/MTCLKA/TMCI2/RXD8/SMISO8/SSCL8/MOSIA/TS14
47	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/SCK8/RSPCKA/TS23		PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/RSPCKA/TS15
48	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0/SDHI_D1/TSCAP		PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0/TSCAP
49	PC3/A19/MTIOC4D/TCLKB/TXD5/SMOSI5/SSDA5/IRTXD5/SDHI_D0/TS27		PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/TS16
50	PC2/A18/MTIOC4B/TCLKA/RXD5/SMISO5/SSCL5/SSLA3/IRRXD5/SDHI_D3/TS30		PC2/MTIOC4B/RXD5/SMISO5/SSCL5/SSLA3/TS17
51	PC1/A17/MTIOC3A/TCLKD/SCK5/SSLA2/TS33		PC1/MTIOC3A/SCK5/SSLA2
52	PC0/A16/MTIOC3C/TCLKC/CTS5#/RTS5#/SS5#/SSLA1/TS35		PC0/MTIOC3C/CTS5#/RTS5#/SS5#/SSLA1
53	PB7/A15/MTIOC3B/TIOCB5/TXD9/SMOSI9/SSDA9/SDHI_D2		PB7/MTIOC3B/TXD9/SMOSI9/SSDA9/TS18
54	PB6/A14/MTIOC3D/TIOCA5/RXD9/SMISO9/SSCL9/SDHI_D1		PB6/MTIOC3D/RXD9/SMISO9/SSCL9/TS19
55	PB5/A13/MTIOC2A/MTIOC1B/TMRI1/POE1#/TIOCB4/SCK9/USB0_VBUS/SDHI_CD		PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#/SCK9/TS20

100-Pin LFQPF	RX230 Group RX231 Group	RX130 Group
56	PB4/A12/TIOCA4/CTS9#/RTS9#/SS9#	PB4/CTS9#/RTS9#/SS9#/TS21
57	PB3/A11/MTIOC0A/MTIOC4A/TMO0/POE3#/TIOCD3/TCLKD/SCK6/SDHI_WP	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/SCK6/TS22
58	PB2/A10/TIOCC3/TCLKC/CTS6#/RTS6#/SS6#	PB2/CTS6#/RTS6#/SS6#/TS23
59	PB1/A9/MTIOC0C/MTIOC4C/TMCI0/TIOCB3/TXD6/SMOSI6/SSDA6/SDHI_CLK/IRQ4/CMPOB1	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD6/SMOSI6/SSDA6/TS24/IRQ4/CMPOB1
60	VCC	VCC
61	PB0/A8/MTIC5W/TIOCA3/RXD6/SMISO6/SSCL6/RSPCKA/SDHI_CMD	PB0/MTIC5W/RXD6/SMISO6/SSCL6/RSPCKA/TS25
62	VSS	VSS
63	PA7/A7/TIOCB2/MISOA	PA7/MISOA
64	PA6/A6/MTIC5V/MTCLKB/TMCI3/POE2#/TIOCA2/CTS5#/RTS5#/SS5#/MOSIA/SSIWS0	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/CTS5#/RTS5#/SS5#/MOSIA/TS26
65	PA5/A5/TIOCB1/RSPCKA	PA5/RSPCKA/TS27
66	PA4/A4/MTIC5U/MTCLKA/TMRI0/TIOCA1/TXD5/SMOSI5/SSDA5/SSLA0/SSITXD0/IRTXD5/IRQ5/CVREFB1	PA4/MTIC5U/MTCLKA/TMRI0/TXD5/SMOSI5/SSDA5/SSLA0/TS28/IRQ5/CVREFB1
67	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/RXD5/SMISO5/SSCL5/SSIRXD0/IRRXD5/IRQ6/CMPB1	PA3/MTIOC0D/MTCLKD/RXD5/SMISO5/SSCL5/TS29/IRQ6/CMPB1
68	PA2/A2/RXD5/SMISO5/SSCL5/SSLA3/IRRXD5	PA2/RXD5/SMISO5/SSCL5/SSLA3/TS30
69	PA1/A1/MTIOC0B/MTCLKC/TIOCB0/SCK5/SSLA2/SSISCK0	PA1/MTIOC0B/MTCLKC/SCK5/SSLA2/TS31
70	PA0/A0/BC0#/MTIOC4A/TIOCA0/SSLA1/CACREF	PA0/MTIOC4A/SSLA1/TS32/CACREF
71	PE7/D15[A15/D15]/IRQ7/AN023	PE7/IRQ7/AN023
72	PE6/D14[A14/D14]/IRQ6/AN022	PE6/IRQ6/AN022
73	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/IRQ5/AN021/CMPOB0	PE5/MTIOC4C/MTIOC2B/IRQ5/AN021/CMPOB0
74	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/AN020/CMPA2/CLKOUT	PE4/MTIOC4D/MTIOC1A/TS33/AN020/CMPA2/CLKOUT
75	PE3/D11[A11/D11]/MTIOC4B/POE8#/CTS12#/RTS12#/SS12#/AUDIO_MCLK/AN019/CLKOUT	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/SS12#/TS34/AN019/CLKOUT
76	PE2/D10[A10/D10]/MTIOC4A/RXD12/RXDX12/SMISO12/SSCL12/IRQ7/AN018/CVREFB0	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/SSCL12/TS35/IRQ7/AN018/CVREFB0
77	PE1/D9[A9/D9]/MTIOC4C/TXD12/TXDX12/SIOX12/SMOSI12/SSDA12/AN017/CMPB0	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/SMOSI12/SSDA12/AN017/CMPB0
78	PE0/D8[A8/D8]/SCK12/AN016	PE0/SCK12/AN016
79	PD7/D7[A7/D7]/MTIC5U/POE0#/IRQ7/AN031	PD7/MTIC5U/POE0#/IRQ7/AN031
80	PD6/D6[A6/D6]/MTIC5V/POE1#/IRQ6/AN030	PD6/MTIC5V/POE1#/IRQ6/AN030
81	PD5/D5[A5/D5]/MTIC5W/POE2#/IRQ5/AN029	PD5/MTIC5W/POE2#/IRQ5/AN029
82	PD4/D4[A4/D4]/POE3#/IRQ4/AN028	PD4/POE3#/IRQ4/AN028
83	PD3/D3[A3/D3]/POE8#/IRQ3/AN027	PD3/POE8#/IRQ3/AN027
84	PD2/D2[A2/D2]/MTIOC4D/IRQ2/AN026	PD2/MTIOC4D/SCK6/IRQ2/AN026

100-Pin LFQPF	RX230 Group	RX231 Group	RX130 Group
85	PD1/D1[A1/D1]/MTIOC4B/IRQ1/AN025		PD1/MTIOC4B/RXD6/SMISO6/SSCL6/IRQ1/AN025
86	PD0/D0[A0/D0]/IRQ0/AN024		PD0/TXD6/SMOSI6/SSDA6/IRQ0/AN024
87	P47/AN007		P47/AN007
88	P46/AN006		P46/AN006
89	P45/AN005		P45/AN005
90	P44/AN004		P44/AN004
91	P43/AN003		P43/AN003
92	P42/AN002		P42/AN002
93	P41/AN001		P41/AN001
94	VREFL0		VREFL0/PJ7
95	P40/AN000		P40/AN000
96	VREFH0		VREFH0/PJ6
97	AVCC0		AVCC0
98	P07/ADTRG0#		P07/ADTRG0#
99	AVSS0		AVSS0
100	P05/DA1		P05/DA1

3.2 64-Pin Package

Table 3.2 lists comparison the pin functions for the 64-pin package.

Table 3.2 Comparison of Pin Functions for 64-Pin Package

64-Pin LFQPF	RX230 Group	RX231 Group	RX130 Group
1	P03/DA0		P03/DA0
2	VCL		VCL
3	MD/FINED		MD/FINED
4	XCIN		XCIN
5	XCOUT		XCOUT
6	RES#		RES#
7	XTAL/P37		XTAL/P37
8	VSS		VSS
9	EXTAL/P36		EXTAL/P36
10	VCC		VCC
11	P35/NMI		P35/NMI
12	VBATT		P32/MTIOC0C/TMO3/TXD6/SMOSI6/SSDA6/TS0/IRQ2/RTCOUT
13	P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/RTS1#/SS1#/SSISCK0/IRQ1		P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/TS1/IRQ1
14	P30/MTIOC4B/TMRI3/POE8#/RTCIC0/RXD1/SMISO1/SSCL1/AUDIO_MCLK/IRQ0/CMPOB3		P30/MTIOC4B/TMRI3/POE8#/RXD1/SMISO1/SSCL1/TS2/IRQ0
15	P27/MTIOC2B/TMCI3/SCK1/SSIWS0/TS2/CVREFB3		P27/MTIOC2B/TMCI3/SCK1/TS3
16	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/USB0_VBUSEN/SSIRXD0/TS3/CMPB3		P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/TS4
17	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/TIOCB0/TCLKD/SCK1/MISOA/SDA/SSITXD0/IRQ7/CMPOB2		P17/MTIOC3A/MTIOC3B/TMO1/POE8#/SCK1/MISOA/SDA/IRQ7
18	P16/MTIOC3C/MTIOC3D/TMO2/TIOCB1/TCLKC/RTCOUT/TXD1/SMOSI1/SSDA1/MOSIA/SCL/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0#		P16/MTIOC3C/MTIOC3D/TMO2/TXD1/SMOSI1/SSDA1/MOSIA/SCL/IRQ6/RTCOUT/ADTRG0#
19	P15/MTIOC0B/MTCLKB/TMCI2/TIOCB2/TCLKB/RXD1/SMISO1/SSCL1/CRXD0/TS12/IRQ5/CMPB2		P15/MTIOC0B/MTCLKB/TMCI2/RXD1/SMISO1/SSCL1/TS5/IRQ5
20	P14/MTIOC3A/MTCLKA/TMRI2/TIOCB5/TCLKA/CTS1#/RTS1#/SS1#/CTXD0/USB0_OVRCURA/TS13/IRQ4/CVREFB2		P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/RTS1#/SS1#/TS6/IRQ4
21	PH3/TMCI0	VCC_USB	PH3/TMCI0/TS7
22	PH2/TMRI0/IRQ1	USB0_DM	PH2/TMRI0/TS8/IRQ1
23	PH1/TMO0/IRQ0	USB0_DP	PH1/TMO0/TS9/IRQ0
24	PH0/CACREF	VSS_USB	PH0/TS10/CACREF
25	P55/MTIOC4D/TMO3/CRXD0/TS15		P55/MTIOC4D/TMO3/TS11
26	P54/MTIOC4B/TMCI1/CTXD0/TS16		P54/MTIOC4B/TMCI1/TS12
27	UB/PC7/MTIOC3A/MTCLKB/TMO2/TXD8/SMOSI8/SSDA8/MISOA/CACREF		PC7/MTIOC3A/TMO2/MTCLKB/MISOA/TS13/CACREF
28	PC6/MTIOC3C/MTCLKA/TMCI2/RXD8/SMISO8/SSCL8/MOSIA/USB0_EXICEN/TS22		PC6/MTIOC3C/MTCLKA/TMCI2/MOSIA/TS14

64-Pin LFQPF	RX230 Group RX231 Group	RX130 Group
29	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/RSPCKA/USB0_ID/TS23	PC5/MTIOC3B/MTCLKD/TMRI2/RSPCKA/TS15
30	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0/SDHI_D1/TSCAP	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#SCK5/SSLA0/TSCAP
31	PC3/MTIOC4D/TCLKB/TXD5/SMOSI5/SSDA5/IRTXD5/SDHI_D0/TS27	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/TS16
32	PC2/MTIOC4B/TCLKA/RXD5/SMISO5/SSCL5/SSLA3/IRRXD5/SDHI_D3/TS30	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/SSLA3/TS17
33	PB7/PC1/MTIOC3B/TIOCB5/TXD9/SMOSI9/SSDA9/SDHI_D2	PB7/PC1/MTIOC3B/TS18
34	PB6/PC0/MTIOC3D/TIOCA5/RXD9/SMISO9/SSCL9/SDHI_D1	PB6/PC0/MTIOC3D/TS19
35	PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#/TIOCB4/SCK9/USB0_VBUS/SDHI_CD	PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#/TS20
36	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/TIOCD3/TCLKD/SCK6/SDHI_WP	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/SCK6/TS22
37	PB1/MTIOC0C/MTIOC4C/TMCI0/TIOCB3/TXD6/SMOSI6/SSDA6/SDHI_CLK/IRQ4/CMPOB1	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD6/SMOSI6/SSDA6/TS24/IRQ4/CMPOB1
38	VCC	VCC
39	PB0/MTIC5W/TIOCA3/RXD6/SMISO6/SSCL6/RSPCKA/SDHI_CMD	PB0/MTIC5W/RXD6/SMISO6/SSCL6/RSPCKA/TS25
40	VSS	VSS
41	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/TIOCA2/CTS5#/RTS5#/SS5#/MOSIA/SSIWS0	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/CTS5#/RTS5#/SS5#/MOSIA/TS26
42	PA4/MTIC5U/MTCLKA/TMRI0/TIOCA1/TXD5/SMOSI5/SSDA5/SSLA0/SSITXD0/IRTXD5/IRQ5/CVREFB1	PA4/MTIC5U/MTCLKA/TMRI0/TXD5/SMOSI5/SSDA5/SSLA0/TS28/IRQ5/CVREFB1
43	PA3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/RXD5/SMISO5/SSCL5/SSIRXD0/IRRXD5/IRQ6/CMPB1	PA3/MTIOC0D/MTCLKD/RXD5/SMISO5/SSCL5/TS29/IRQ6/CMPB1
44	PA1/MTIOC0B/MTCLKC/TIOCB0/SCK5/SSLA2/SSISCK0	PA1/MTIOC0B/MTCLKC/SCK5/SSLA2/TS31
45	PA0/MTIOC4A/TIOCA0/SSLA1/CACREF	PA0/MTIOC4A/SSLA1/TS32/CACREF
46	PE5/MTIOC4C/MTIOC2B/IRQ5/AN021/CMPOB0	PE5/MTIOC4C/MTIOC2B/IRQ5/AN021/CMPOB0
47	PE4/MTIOC4D/MTIOC1A/AN020/CMPA2/CLKOUT	PE4/MTIOC4D/MTIOC1A/TS33/AN020/CMPA2/CLKOUT
48	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/SS12#/AUDIO_MCLK/AN019/CLKOUT	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/SS12#/TS34/AN019/CLKOUT
49	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/SSCL12/IRQ7/AN018/CVREFB0	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/SSCL12/ TS35/IRQ7/AN018/CVREFB
50	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/SMOSI12/SSDA12/AN017/CMPB0	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/SMOSI12/SSDA12/AN017/CMPB0
51	PE0/SCK12/AN016	PE0/SCK12/AN016
52	VREFL	P47/AN007
53	P46/AN006	P46/AN006
54	VREFH	P45/AN005
55	P44/AN004	P44/AN004
56	P43/AN003	P43/AN003
57	P42/AN002	P42/AN002

64-Pin LFQPF	RX230 Group	RX231 Group	RX130 Group
58	P41/AN001		P41/AN001
59	VREFL0		VREFL0/PJ7
60	P40/AN000		P40/AN000
61	VREFH0		VREFH0/PJ6
62	AVCC0		AVCC0
63	P05/DA1		P05/DA1
64	AVSS0		AVSS0

3.3 48-Pin Package

Table 3.3 lists comparison the pin functions for the 48-pin package.

Table 3.3 Comparison of Pin Functions for 48-Pin Package

48-Pin LFQPF	RX230 Group	RX231 Group	RX130 Group
1	VCL		VCL
2	MD/FINED		MD/FINED
3	RES#		RES#
4	XTAL/P37		XTAL/P37
5	VSS		VSS
6	EXTAL/P36		EXTAL/P36
7	VCC		VCC
8	P35/NMI		P35/NMI
9	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/SSISCK0/IRQ1		P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/TS1/IRQ1
10	P30/MTIOC4B/TMRI3/POE8#/RXD1/SMISO1/SSCL1/AUDIO_MCLK/IRQ0/CMPOB3		P30/MTIOC4B/TMRI3/POE8#/RXD1/SMISO1/SSCL1/TS2/IRQ0
11	P27/MTIOC2B/TMCI3/SCK1/SSIWS0/TS2/CVREFB3		P27/MTIOC2B/TMCI3/SCK1/TS3
12	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/USB0_VBUSEN/SSIRXD0/TS3/CMPB3		P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/TS4
13	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/TIOCB0/TCLKD/SCK1/MISOA/SDA//SSITXD0/IRQ7/CMPOB2		P17/MTIOC3A/MTIOC3B/TMO1/POE8#/SCK1/MISOA/SDA/IRQ7
14	P16/MTIOC3C/MTIOC3D/TMO2/TIOCB1/TCLKC/TXD1/SMOSI1/SSDA1/MOSIA/SCL/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0#		P16/MTIOC3C/MTIOC3D/TMO2/TXD1/SMOSI1/SSDA1/MOSIA/SCL/IRQ6/ADTRG0#
15	P15/MTIOC0B/MTCLKB/TMCI2/TIOCB2/TCLKB/RXD1/SMISO1/SSCL1/CRXD0/TS12/IRQ5/CMPB2		P15/MTIOC0B/MTCLKB/TMCI2/RXD1/SMISO1/SSCL1/TS5/IRQ5
16	P14/MTIOC3A/MTCLKA/TMRI2/TIOCB5/TCLKA/CTS1#/RTS1#/SS1#/CTXD0/USB0_OVRCURA/TS13/IRQ4/CVREFB2		P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/RTS1#/SS1#/TS6/IRQ4
17	PH3/TMCI0	VCC_USB	PH3/TMCI0/TS7
18	PH2/TMRI0/IRQ1	USB0_DM	PH2/TMRI0/TS8/IRQ1
19	PH1/TMO0/IRQ0	USB0_DP	PH1/TMO0/TS9/IRQ0
20	PH0/CACREF	VSS_USB	PH0/TS10/CACREF
21	UB/PC7/MTIOC3A/MTCLKB/TMO2/TXD8/SMOSI8/SSDA8/MISOA/CACREF		PC7/MTIOC3A/TMO2/MTCLKB/MISOA/TS13/CACREF
22	PC6/MTIOC3C/MTCLKA/TMCI2/RXD8/SMISO8/SSCL8/MOSIA/USB0_EXICEN/TS22		PC6/MTIOC3C/MTCLKA/TMCI2/MOSIA/TS14
23	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/RSPCKA/USB0_ID/TS23		PC5/MTIOC3B/MTCLKD/TMRI2/RSPCKA/TS15
24	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0/SDHI_D1/TSCAP		PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/SCK5/SSLA0/TSCAP
25	PB5/PC3/MTIOC2A/MTIOC1B/TMRI1/POE1#/TIOCB4/USB0_VBUS/SDHI_CD		PB5/PC3/MTIOC2A/MTIOC1B/TMRI1/POE1#/TS20
26	PB3/PC2/MTIOC0A/MTIOC4A/TMO0/POE3#/TIOCD3/TCLKD/SCK6/SDHI_WP		PB3/PC2/MTIOC0A/MTIOC4A/TMO0/POE3#/SCK6/TS22

48-Pin LFQPF	RX230 Group RX231 Group	RX130 Group
27	PB1/PC1/MTIOC0C/MTIOC4C/TMCI0/TIOCB3/TXD6/SMOSI6/SSDA6/SDHI_CLK/IRQ4/CMPOB1	PB1/PC1/MTIOC0C/MTIOC4C/TMCI0/TXD6/SMOSI6/SSDA6/TS24/IRQ4/CMPOB1
28	VCC	VCC
29	PB0/PC0/MTIC5W/TIOCA3/RXD6/SMISO6/SSCL6/RSPCKA/SDHI_CMD	PB0/PC0/MTIC5W/RXD6/SMISO6/SSCL6/RSPCKA/TS25
30	VSS	VSS
31	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/TIOCA2/CTS5#/RTS5#/SS5#/MOSIA/SSIWS0	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/CTS5#/RTS5#/SS5#/MOSIA/TS26
32	PA4/MTIC5U/MTCLKA/TMRI0/TIOCA1/TXD5/SMOSI5/SSDA5/SSLA0/SSITXD0/IRTXD5/IRQ5/CVREFB1	PA4/MTIC5U/MTCLKA/TMRI0/TXD5/SMOSI5/SSDA5/SSLA0/TS28/IRQ5/CVREFB1
33	PA3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/RXD5/SMISO5/SSCL5/SSIRXD0/IRRXD5/IRQ6/CMPB1	PA3/MTIOC0D/MTCLKD/RXD5/SMISO5/SSCL5/TS29/IRQ6/CMPB1
34	PA1/MTIOC0B/MTCLKC/TIOCB0/SCK5/SSLA2/SSISCK0	PA1/MTIOC0B/MTCLKC/SCK5/SSLA2/TS31
35	PE4/MTIOC4D/MTIOC1A/AN020/CMPA2/CLKOUT	PE4/MTIOC4D/MTIOC1A/TS33/AN020/CMPA2/CLKOUT
36	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/AUDIO_MCLK/AN019/CLKOUT	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/TS34/AN019/CLKOUT
37	PE2/MTIOC4A/RXD12/RXDX12/SSCL12/IRQ7/AN018/CVREFB0	PE2/MTIOC4A/RXD12/RXDX12/SSCL12/TS35/IRQ7/AN018/CVREFB0
38	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/SSDA12/AN017/CMPB0	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/SSDA12/AN017/CMPB0
39	VREFL	P47/AN007
40	P46/AN006	P46/AN006
41	VREFH	P45/AN005
42	P42/AN002	P42/AN002
43	P41/AN001	P41/AN001
44	VREFL0	VREFL0/PJ7
45	P40/AN000	P40/AN000
46	VREFH0	VREFH0/PJ6
47	AVCC0	AVCC0
48	AVSS0	AVSS0

4. Notes on Migration

Several points require attention when migrating between the RX230 or RX231 Group and the RX130 Group. Those related to hardware are described in 4.1, Notes on Pin Design, and those related to software are covered in 4.2, Notes on Function Settings.

4.1 Notes on Pin Design

The RX230, RX231, and RX130 groups are pin compatible, easing the pin design burden when migrating between groups. There are some differences in the handling of pins among the various series, however.

4.1.1 Power Supply Pin

On the RX230, RX231, and RX130 groups, the upper limit of the ICLK operating frequency differs depending on the voltage (Vcc) input on the power supply pin. Use a power supply voltage that is appropriate for the desired operating frequency.

Table 4.1 Power Supply Voltage and Operating Frequency

	Power Supply Voltage and Upper Limit Frequency		
MCU	**1.8 V to 2.4 V**	**2.4 V to 2.7 V**	**2.7 V to 5.5 V**
RX230/RX231	8 MHz	16 MHz	54 MHz
RX130			32 MHz

4.1.2 VBATT Pin

The VBATT pin and battery backup function are implemented on RX230 and RX231 Group MCUs but not on RX130 Group MCUs.

4.1.3 USB Pins

The VCC_USB, VSS_USB, USB0_VBUS, USB0_VBUSEN, USB0_OVRCURA, USB0_OVRCURB, USB0_EXICEN, USB0_ID, USB0_DM, and USB0_DP pins and the USBd function are implemented on RX231 Group MCUs but not on RX230 or RX130 Group MCUs.

4.1.4 D/A Converter Analog Input Pins

The VREFH and VREFL pins are implemented on RX230 and RX231 Group MCUs but not on RX130 Group MCUs.

4.1.5 Comparator B Analog Pins

The P14/CVREFB2 and P15/CMPB2 pins and comparator B2 function, and the P27/CVREFB3 and P26/CMPB3 pins and comparator B3 function, are implemented on RX230 and RX231 Group MCUs but not on RX130 Group MCUs.

4.2 Notes on Function Settings

Software that runs on RX230 and RX231 Group MCUs is highly compatible with software for RX130 Group MCUs. Nevertheless, careful evaluation is necessary due to differences in factors such as operation timing and electrical characteristics.

Points that require attention when porting software between RX230 or RX231 Group MCUs and RX130 Group MCUs due to different function settings are described below. For details of the differences between modules and functions, see 2, Comparative Overview of Functions. Make sure to perform careful evaluation of the software when making use of the information in this application note.

4.2.1 Option-Setting Memory

Option function select register 0 (OFS0) in the flash memory differs between RX230 and RX231 Group MCUs and RX130 Group MCUs. When migrating, make sure to change the setting values accordingly.

Refer to 2.5, Option-Setting Memory, for the points of difference. For more details, see User's Manual: Hardware, listed in 5, Reference Documents.

4.2.2 Exception Vector Table

On RX230 and RX231 Group MCUs the exception vector table is allocated according to the start address specified in the exception table register (EXTB), but on RX130 Group MCUs the table's address is fixed.

For details, see User's Manual: Hardware, listed in 5, Reference Documents.

4.2.3 Operating Modes

On-chip ROM enabled extended mode, on-chip ROM disabled extended mode, and boot mode (USB interface) are implemented on RX231 Group MCUs but not on RX230 and RX130 Group MCUs.

4.2.4 Clock Generation Circuit

The HOCO operating frequencies and PLL circuit multiplication factors differ between RX230 and RX231 Group MCUs and RX130 Group MCUs. When migrating, make sure to change the setting values accordingly.

Refer to 2.5, Clock Generation Circuit, for the points of difference. For more details, see User's Manual: Hardware, listed in 5, Reference Documents.

4.2.5 Memory Wait Cycles

The memory wait cycle setting register (MEMWAIT) is implemented on RX230 and RX231 Group MCUs but not on RX130 Group MCUs. On RX230 and RX231 Group MCUs, set the MEMWAIT bit to 1 (wait cycles) when selecting a frequency higher than 32 MHz for ICLK.

Refer to 2.5, Clock Generation Circuit, for the points of difference. For more details, see User's Manual: Hardware, listed in 5, Reference Documents.

4.2.6 Flash Memory

The flash memory programming and erasing times and units differ between RX130 Group MCUs and RX230 or RX231 Group MCUs. This means that software that uses self-programming in single-chip mode needs to be modified.

Refer to 2.22, Flash Memory, for the points of difference related to the flash memory. For more details, see User's Manual: Hardware, listed in 5, Reference Documents.

5. Reference Documents

User's Manual: Hardware

RX230/RX231 Group, User's Manual: Hardware Rev.1.20 (R01UH0496EJ)
(The latest version can be downloaded from the Renesas Electronics website.)

RX130 Group User's Manual: Hardware Rev.3.00 (R01UH0560EJ)
(The latest version can be downloaded from the Renesas Electronics website.)

On-Chip Debugging Emulator

E1/E20 Emulator, E2 Emulator Lite Additional Document for User's Manual (RX User System Design) (R20UT0399EJ)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The technical updates issued after each referenced user manual are not reflected in this application note, so obtain latest version from the Renesas Electronics website.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jan. 12, 2016	-	First edition issued
1.10	Sep. 14, 2018	Whole	Correspondence for 512KB of RX130
1.20	May. 22, 2019	Whole	Confirmed the contents of the description again (Addition of description mistake etc.)
		5	Add Comparative Overview of CPU
		7	Add memory map comparison of address space
		9	Add area comparison of option setting memory
		17	Add Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode
		22	Add Comparative Overview of Exception Handling
		34	Add Comparative Listing of Functions Assigned to Each Multiplexed Pin
		50	Add Comparative Overview of 8-Bit Timer
		54	Add Comparative Overview of Independent Watchdog Timer

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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