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RENESAS

32176 Group

Outline of the CAN Module

1. Overview

The 32176 Group microcomputer includes a 2-channel Full CAN module which conforms to the CAN Specification V2.0B active.

This document presents an outline of the CAN (Controller Area Network) module incorporated in the 32176 Group microcomputer.

2. Introduction

The sample task described in this document uses the following microcomputers, under the respective conditions.

- Microcomputer: 32176 Group (M32176FnVFP, M32176FnTFP)
- Operating Frequency: 20 to 40 MHz
- Operating Board: Starter kit for 32176 Group

3. Interpretation of the CAN (Controller Area Network)

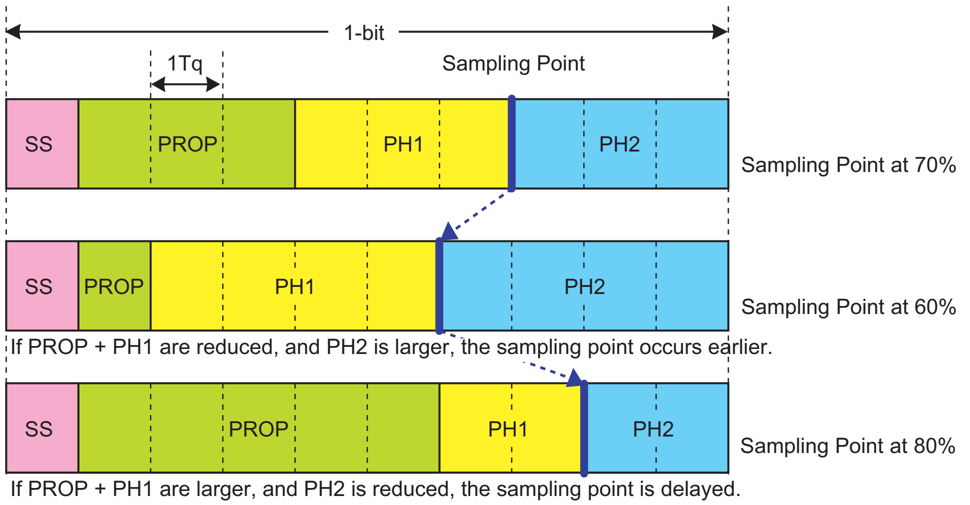
3.1 CAN Bit Timing

In the CAN protocol each communication frame bit comprises of 4 segments.

Figure 3.1.1 shows the segment structure of each bit and the sampling points.

These segments, the propagation time segment (PROP), phase buffer segment 1 (PH1), phase buffer segment 2 (PH2) define the sampling points, and by changing these values the sampling timing can be varied.

The minimum timing setting is called the time quantum (Tq). The Tq cycle is determined by the clock frequency input to the CAN module and the baud rate prescaler frequency division value.



SS: Synchronization Segment
PROP: Propagation Time Segment
PH1: Phase Buffer Segment1
PH2: Phase Buffer Segment2
Tq: Time Quantam

Figure 3.1.1 Bit Segment Structure and Sampling Points

(1) SS: Synchronization Segment
This segment controls synchronization by monitoring the recessive to dominant edge within the interframe space (Note 1).

(2) PROP: Propagation Time Segment
In a CAN network this is the segment which absorbs the physical delay. In the network the physical delay is double the total of, bus delay, input comparator delay, and output driver delay.

(3) PH1, PH2: Phase Buffer Segment 1, Phase Buffer Segment 2
The purpose of these segments is to compensate the phase error when re-synchronizing (Note 2).

(4) SJW: reSynchronization Jump Width
This is the maximum width by which the synchronization shift due to phase error can be compensated.

Note 1: Interframe Space is formed by the Intermission, Suspend Transmission, and Bus Idle.
Note 2: Phase Error is due to the shift in the oscillator frequency and the synchronization shift.

3.2 Bit Timing Conditions

Under the CAN protocol the range and limitations of each segment are as specified below.

(1) Setting each segment.

- SS = 1Tq fixed
- PROP = range between 1 to 8 Tq
- PH1 = range between 1 to 8 Tq
- PH2 = range between 1 to 8 Tq
- SJW = range between 1 to 4 Tq
- SS + PROP + PH1 + PH2 = 8 to 25 Tq

(2) Set PH1, PH2, and SJW to meet the conditions specified below.

- SJW ≤ min (PH1, PH2)
- PH2 = max (PH1, IPT)

  min() is the function for setting minimum values.
  max() is the function for setting maximum values.
  IPT: Information Processing Time defines the time immediately following the sampling point.
  (The 32176 internal CAN module has an IPT = 1.)

3.3 Synchronization Method

CAN protocol uses a NRZ (Non-Return to Zero) communication method. A synchronization signal cannot be added to the start or end of each bit.

(1) Hardware synchronization (synchronization when no messages are being transmitted or received)

When detecting the recessive to dominant edge within the interframe space, that point is recognized as the start of the bit (SS), and synchronization is attained. This is called hardware synchronization.
Figure 3.3.1 shows the structure of hardware synchronization.

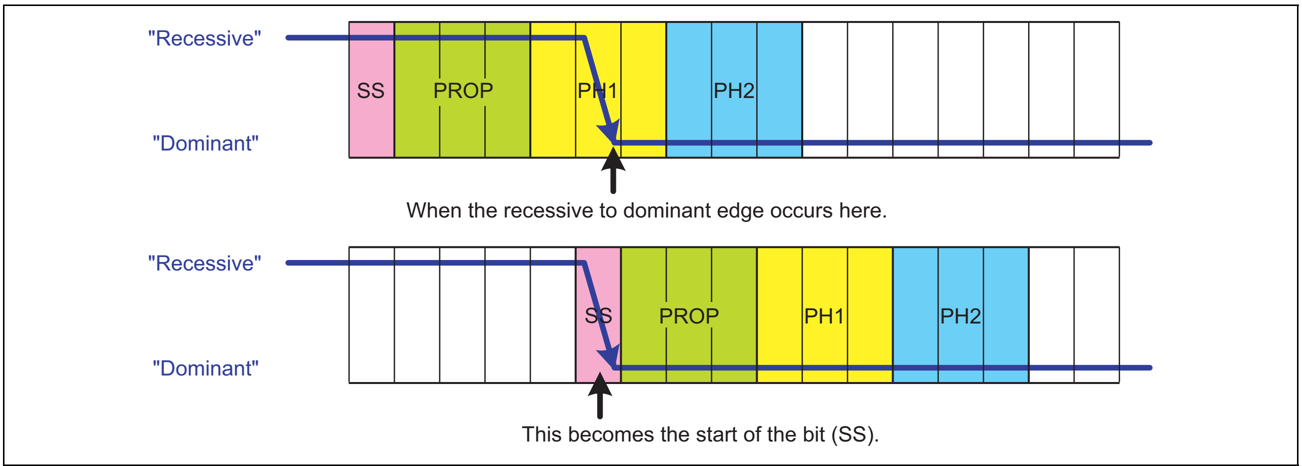


Figure 3.3.1 Hardware Synchronization Structure

(2) reSynchronization (synchronization during transmitting/receiving messages)

Synchronization between each node may be displaced due to the shift in the oscillator frequency, or the delay in the transmission circuit during transmitting or receiving messages. This is called phase error. When synchronization shift occurs, the length of 1 bit is corrected dynamically by increasing PH1 and reducing PH2 using values less than or equal to SJW according to the synchronization shift (if the shift exceeds SJW values then the SJW value is used). This is called reSynchronization.

reSynchronization, similar to hardware synchronization, only attains synchronization by detecting the recessive to dominant edge.

Figure 3.3.2 shows the structure when the recessive to dominant edge occurs in either the PROP or PH1 segment, Figure 3.3.3 shows the structure of reSynchronization when the recessive to dominant edge occurs in the PH2 segment.

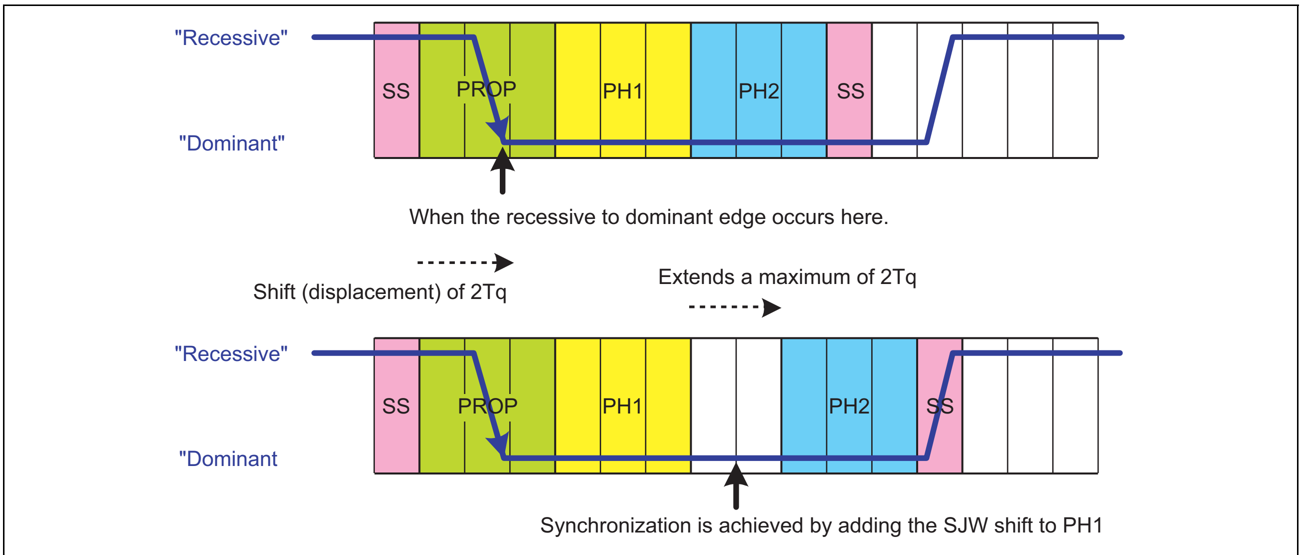


Figure 3.3.2 reSynchronization Structure 1 (SJW = 2 examples)

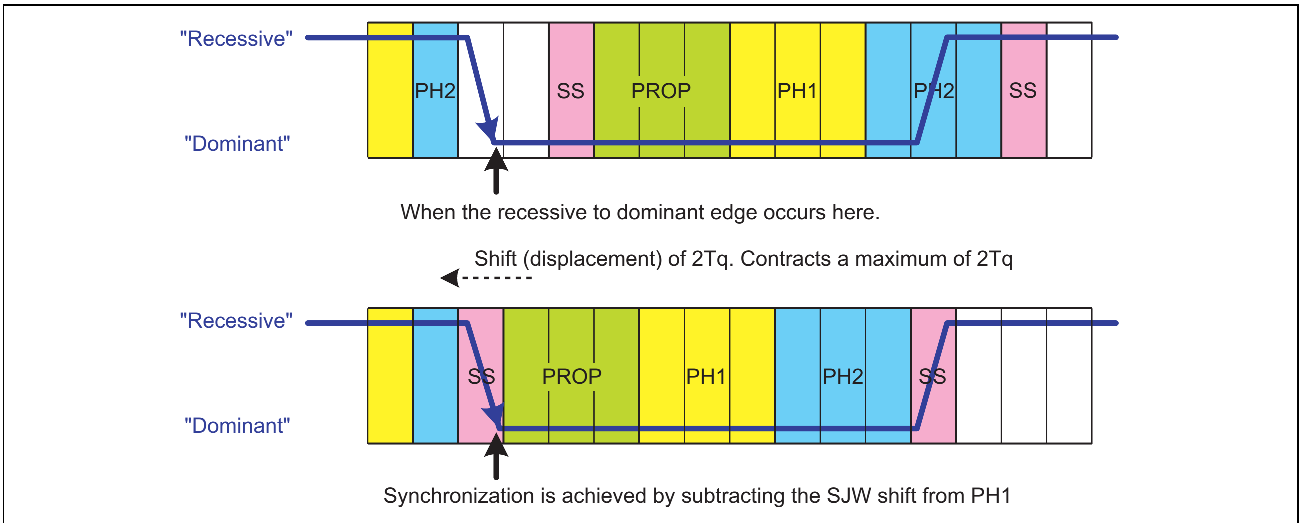


Figure 3.3.3 reSynchronization Structure 2 (SJW = 2 examples)

3.4 Transfer Speed

The CPU clock determines the transfer speed, the value set in baud rate prescaler (BRP), and the number of Tq's in 1 bit.

The transfer speed can be calculated using the equation below.

Tq cycle = (BRP + 1) / CPU clock
Tq number in 1-bit = SS + PROP + PH1 + PH2

$$\text{CAN transfer speed (bps)} = \frac{1}{\text{Tq cycle} \times \text{number of Tq in 1 bit}}$$

Table 3.4.1 shows example bit timing settings with the CPU clock at 40 MHz, and table 3.4.2 shows example bit timing settings with the CPU clock at 32 MHz.

Table 3.4.1 Example Bit Timing Settings with the CPU Clock at 40 MHz

Transfer Speed	BRP Setting Value	Tq cycle (ns)	Tq Count in 1 Bit	PROP + PH1	PH2	Sampling Point
1 Mbps	1	50	20	13	6	70%
	3	100	10	7	2	80%
				6	3	70%
				5	4	60%
	4	125	8	5	2	75%
				4	3	63%
500 Kbps	4	125	16	13	2	88%
				12	3	81%
				11	4	75%
	7	200	10	7	2	80%
				6	3	70%
				5	4	60%
	9	250	8	5	2	75%
				4	3	63%

Note: The above communication transfer speeds are not guaranteed. Use only after careful evaluation and verification.

Table 3.4.2 Example Bit Timing Settings with the CPU Clock at 32 MHz

Transfer Speed	BRP Setting Value	Tq cycle (ns)	Tq Count in 1 Bit	PROP + PH1	PH2	Sampling Point
1 Mbps	1	62.5	16	10	5	69%
	3	125	8	5	2	75%
				4	3	63%
500 Kbps	3	125	16	13	2	88%
				11	4	75%
	7	250	8	5	2	75%
				4	3	63%

Note: The above communication transfer speeds are not guaranteed. Use only after careful evaluation and verification.

4. Transmitting and Receiving CAN Messages

The 32176 Group microcomputer has 16 slots for each CAN module channel, and each slot can be set to transmit mode or receive mode. The transmit or receive mode is set by the CAN message slot control register.

Table 4.1.1 shows the relationship between the values written to the CAN message slot control register and the operations.

Table 4.1.1 Relationship between the Values Written to the CAN Message Slot Control Register and Operations

Value Written	Operation
H'00	Clears all the flags of the message slot control register and stops transmitting/receiving at the corresponding message slot. Before transmitting/receiving the data frame and the remote frame, H'00 must be written and it is necessary to confirm that the transmit/receive status bit is cleared.
H'0F	Cancels the requested data frame and the remote frame transmit requests at the corresponding message slot.
H'80	Issues the data frame transmit request for the corresponding message slot.
H'40	Issues the data frame receive request for the corresponding message slot.
H'A0	Issues the remote frame transmit request for the corresponding message slot.
H'60	Issues the remote frame receive request for the corresponding message slot. After receiving the remote frame, the data frame is automatically transmitted
H'70	Issues the remote frame receive request for the corresponding message slot. After receiving the remote frame, transmission stops.
H'4E	Clears the transmission/reception finished bit, when setting the data frame reception. The message lost bit will not be cleared.
H'AE	Clears the transmission/reception finished bit when setting the remote frame transmission. The message lost bit will not be cleared.

Note: If the transmit request bit and receive request bit are both set to 1, operation becomes unstable.

4.1 Message Transmission

The transmitting message is always transmitted from the slot of the next available lowest number. Transmission has the following two modes.

(1) Data frame transmit mode

By setting the slot to the data frame transmit mode, the data frame of ID allocated to that slot can be transmitted.

(2) Mode to receive data frame after transmitting remote frame

By setting the slot in this mode, the slot can automatically receive the data frame with the same ID after transmitting the ID set in the slot, and the DLC remote frame.

4.2 Message Reception

When not using the acceptance filter, the received message is stored in a slot of the next available lowest number. By using the acceptance filter, received messages can be selected.

Receive operation has the following two modes.

(1) Data frame receive mode.

By setting the slot to the data frame receive mode, the slot can receive the data frame of the allocated ID.

(2) Mode to transmit data frame after receiving remote frame.

By setting the slot, to this mode, the data frame which is set to the same slot can be transmitted automatically, after receiving the remote frame of the set ID. At this time, the number of bytes to be transmitted is determined by the DLC value of the received remote frame.

4.3 CAN Communication Error and Message Lost

(1) CAN communication error

In 32176 groups, error information when the communication error occurs by the CAN cause of error register can be obtained. Error information that can be obtained is as follows.

1) Transmission error
   When a communication error is detected at a transmission node.
2) Receive error
   When a communication error is detected at a reception node.
3) Bit error during transmission of "0"
   When the output level during transmission of "0" from CTX differs from the bus level.
4) Bit error during transmission of "1"
   When the output level during transmission of "1" from CTX differs from the bus level.
5) Stuff error
   When the same level is detected in the bit-stuffing field for six continuous/consecutive bits.
6) Form error
   When an illegal format is detected in a fixed format.
7) CRC error
   When the transmitted CRC value from a transmitting node differs from the CRC calculated at the receiving node.
8) ACK error
   When a transmission unit received is recessive at the ACK slot.

Note: Depending on the error state, multiple bits may be set simultaneously.

(2) Message Lost

When messages are received consecutively, the slot content is overwritten by the next message received. At the receiving slot, if the next message is received before transmission/reception finished bit of the CAN message slot control register is cleared to "0" by the program, then the message lost bit of the CAN message slot control register becomes "1".

Then, the newly received message is stored in that slot.

If there is message lost when reading received data, undefined values may be included in the read out data. In such cases re-receive the data, or discard the received data.

(3) CAN Controller Error State

The CAN controller, depending on the values of the transmit error counter and receive error counter, will form the following three error states.

1) Error active state
   - Errors rarely occur.
   - At error detection active error flags are transmitted.
   - CAN controller state immediately after initial settings.
2) Error passive state
   - Multiple errors occur.
   - At error detection passive error flags are transmitted.
3) Bus off state
   - Errors occur extremely frequently.
   - Until the error active state is entered CAN communication is not possible with other nodes.

Depending on the state of transmission/reception, when an error is detected at a slot, the transmit error counter value, or the receive error counter value is incremented. When the transmit error counter value, or the receive error counter value exceed 128, the CAN status becomes the error passive state. When the transmit error counter value exceeds 256, the status becomes the bus off state.

The error state transition diagram is shown in figure 4.3.1 and the variable conditions of the error counter value are shown in table 4.3.1.

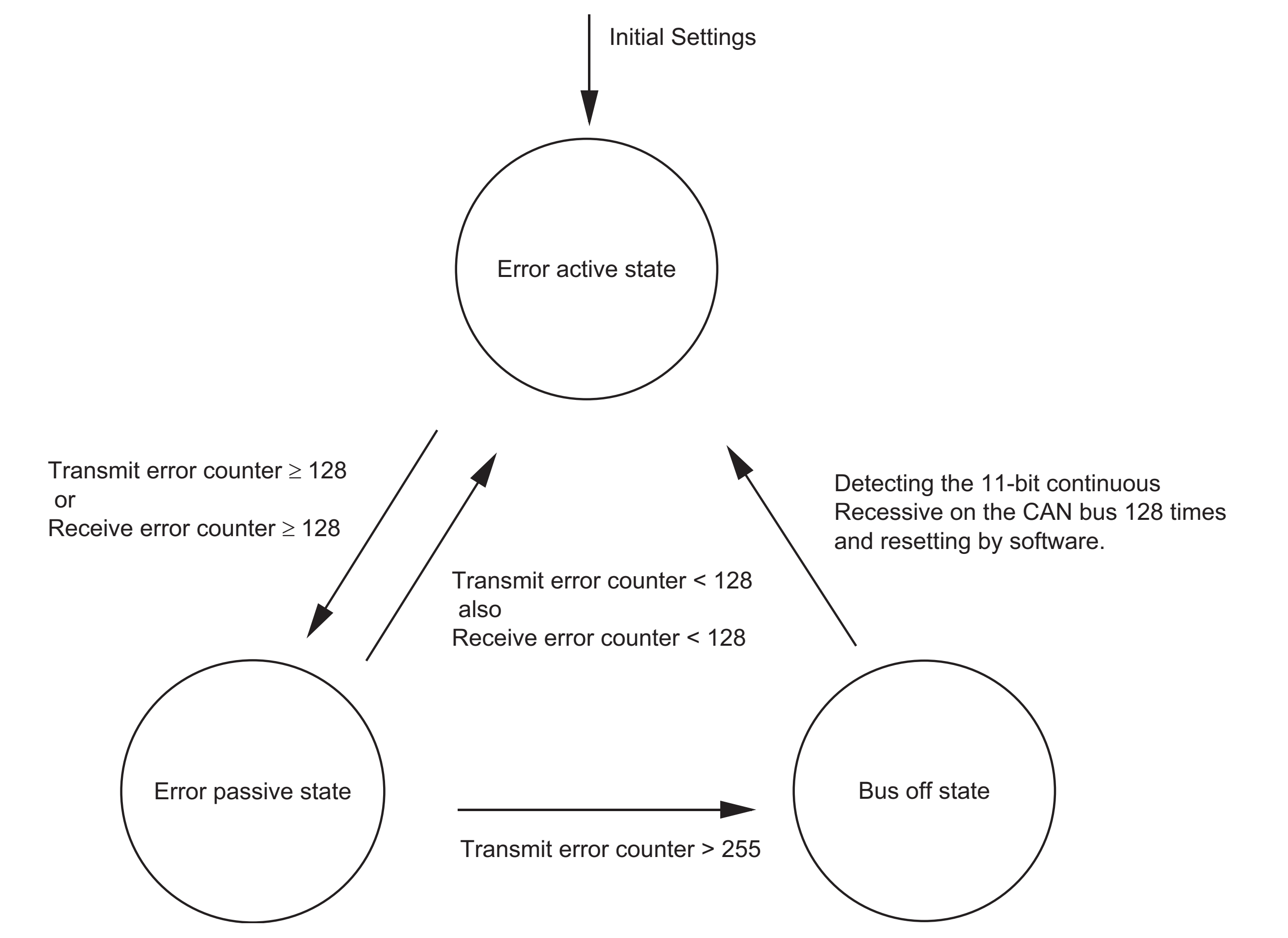


Figure 4.3.1 Error State Transition Diagram

Table 4.3.1 Variable Conditions of Error Counter Value

No.	Variable Condition of Transmit/Receive Error Counter	Transmit Error Counter (TEC)	Receive Error Counter (REC)
1	When the receive unit detects errors. However, the receive error counter is not incremented when the receive unit detects a bit error during transmission of an error flag or overload flag.	—	+1
2	When the receive unit detects a dominant bit after transmitting the error flag.	—	+8
3	When the transmission unit outputs an error flag.	+8	—
4	When the transmission unit detects a bit error during the transmission of active error flag or overload flag.	+8	—
5	When the receive unit detects a bit error during the transmission of an active error flag or overload flag.	—	+8
6	When each unit detects continuous 14-bit dominant from the start of the active error flag, and the overload flag. From there after, on detection of a continuous 8-bit dominant.	When transmitting +8	When receiving +8
7	When each unit detects an addition of a continuous 8-bit dominant after a passive error flag.	When transmitting +8	When receiving +8
8	A transmission unit transmits data in normal transmission (when ACK is returned and error is not detected until EOF)	–1 When TEC = 0, ±0	—
9	A receive unit received data normally (detecting no error until the CRC filed and ACK is returned normally)	—	When 1 ≤ REC ≤ 127, –1 When REC = 0, ±0 When REC > 127, set REC = 127
10	When the bus-off unit detects 11-bit recessive bits continuously for 128 times.	Clear TEC to 0	Clear REC to 0
Exception 1	When the transmission unit is in the error passive state, an ACK error is detected, then the dominant bit is not detected during transmission of a passive error flag.	—	—
Exception 2	The transmission unit outputs an error flag based on a stuff error occurred during arbitration. Here, this stuff bit is recessive, and the transmission unit transmitted a recessive but a dominant was detected.	—	—

4.4 CAN Interrupt

An interrupt request can be issued as a result of CAN transmission.

An interrupt request is possible when communicating normally or when abnormal termination occurs.

(1) When completed normally.

An interrupt request can be confirmed by the CAN slot interrupt request status register.

When using an interrupt, the bit of the CAN slot interrupt request mask register corresponding to the slot is set to "1" (interrupt request enabled). The CAN slot interrupt request status register is used together with the CAN transmission-finished interrupt and the CAN reception-finished interrupt. This slot setting by generating a transmission finish interrupt request when transmitting data, a receive finish interrupt request when receiving data, sets the corresponding bit to "1".

Each bit of the CAN slot interrupt request status register can be cleared to "0" by the program. For clearing write "0" to the bit to be cleared and "1" to other bits. When "1" is written the previous data is retained.

Note:

- When the auto response function is enabled at the remote frame receive slot, the request status is set after reception of the remote frame is complete, or after data frame transmission is complete.
- In the remote frame transmission slot, the request status is set, after remote frame transmission is complete, or after the data frame reception is complete.
- If setting the request status by an interrupt request and clearing the request status by the program occur simultaneously, priority is given to the request status setup by the interrupt request.

(2) When completed abnormally.

The occurrence of a communication error (bus error, transition to error passive state, transition to bus off state) can be confirmed by the CAN error interrupt request status register.

Furthermore, detection of arbitration-lost, or transmission failure due to a transmission error can be confirmed in the single-shot mode.

When using the CAN error interrupt, the corresponding bit of the CAN error interrupt request mask register is set to 1 (interrupt request enabled).

- When the CAN bus error interrupt request enable bit is "1", a CAN bus error interrupt request occurs for each bus error detected.
- When the CAN error passive interrupt request enable bit has a value "1" and the error passive state is entered, the CAN error passive interrupt request is generated.
- When the CAN bus off interrupt request enable bit is "1", and the bus off state is entered, the CAN bus off interrupt request is generated.

Each bit of the CAN error interrupt request status register can be cleared to "0" by the program.

For clearing write "0" to the bit to be cleared and "1" to other bits. When "1" is written the previous data is retained.

When using the single-shot interrupts, the corresponding bit of the CAN single-shot interrupt request mask register is set to "1" (interrupt request enabled).

- Detection of arbitration-lost, or when transmission failure due to transmission error occurs, the slot and corresponding bit of the CAN single-shot interrupt request status register is set to "1".

Each bit of the CAN single-shot interrupt request status register can be cleared to "0" by the program. For clearing write "0" to the bit to be cleared and "1" to other bits. When "1" is written the previous data is retained.

5. CAN Module Functions

5.1 Transmission Abort Function

When transmission on the CAN bus to two or more nodes starts simultaneously, the node with low message priority is lost to arbitration and transmission is aborted. (After transmission of the message predominant to arbitration ends, transmission recommences). If the message was not lost to arbitration, transmission would not end normally and re-transmission would be repeated infinitely. This would create the state when new messages could not be transmitted. For this reason, the transmission abort function is present to discard a message during re-transmission.

The transmission abort function is enabled to establish a time limit on the transmission of a message or when transmitting an urgent message with a high priority order. Figure 5.1.1 shows an application of the transmission abort function.

The transmission abort is executed by writing H'0F to the CAN message slot control register.

(1) The conditions when transmit abort request becomes enabled.

- When a data frame or remote frame is transmitted.
  When the transmit request bit of the CAN message slot control register is “1”.
- When a data frame is transmitted after receiving a remote frame.
  When the receive request bit of the CAN message slot control register is “1”.

(2) The conditions for executing transmit abort.

- When a message is waiting for transmission.
- When a message is lost to arbitration. (figures 5.1.2 and 5.1.3)
- When an error occurs during message transmission. (figures 5.1.2 and 5.1.3)

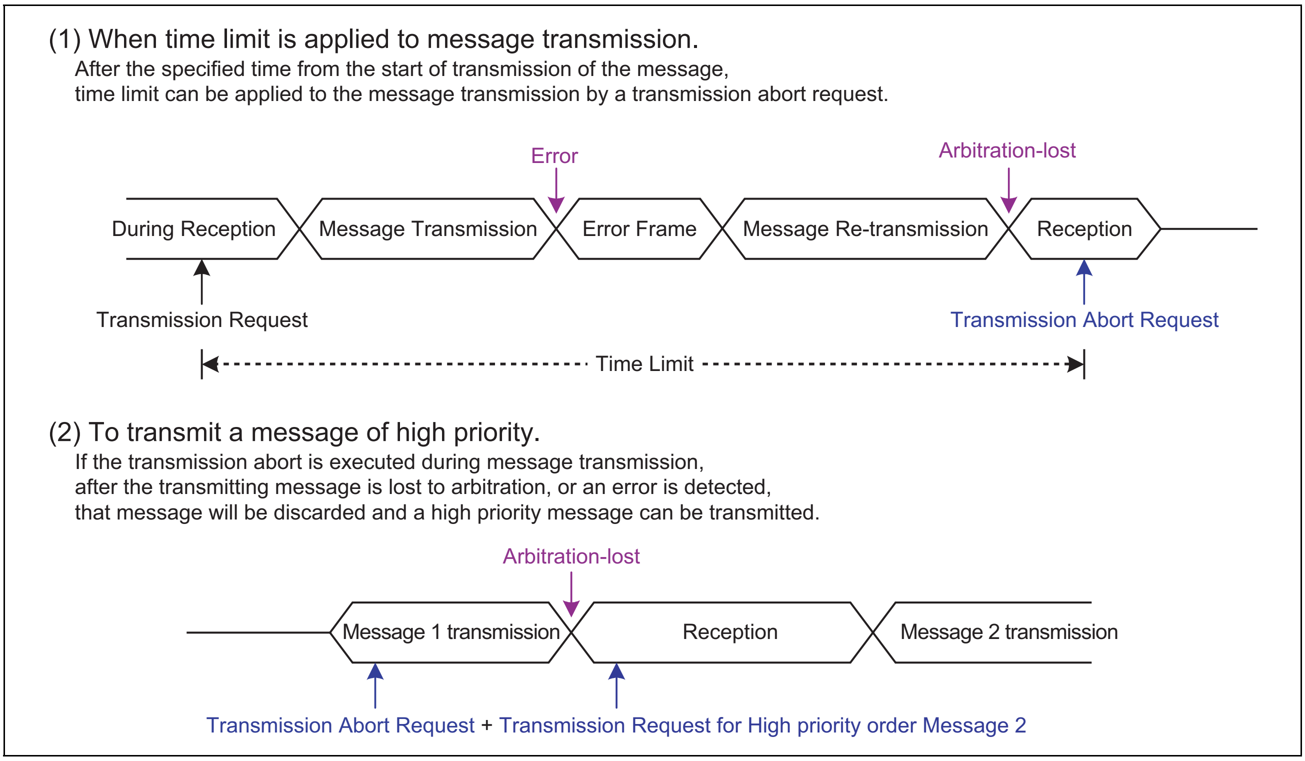


Figure 5.1.1 Example Application of the Transmission Abort Function

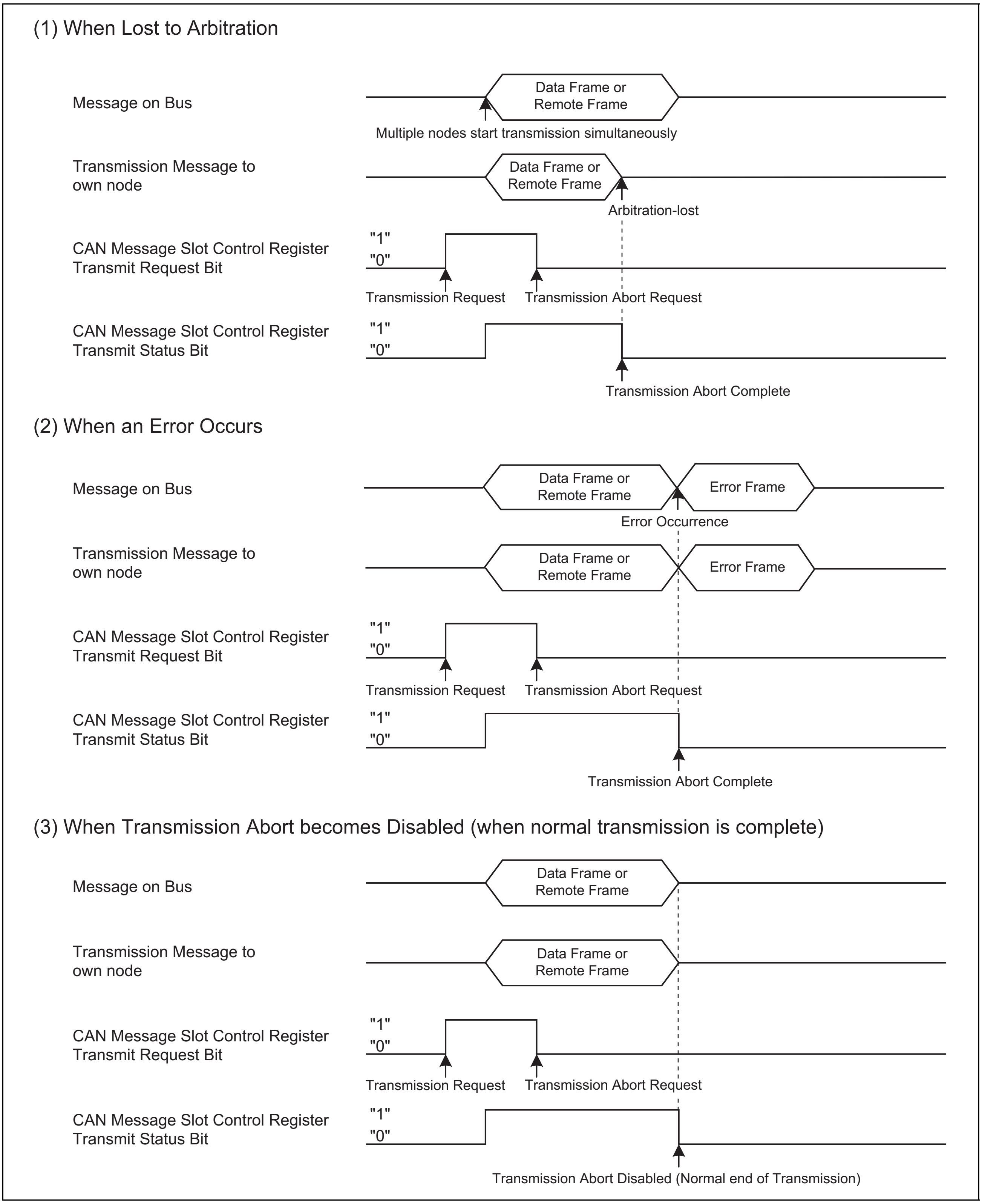


Figure 5.1.2 Transmission Abort During Data Frame or Remote Frame Transmission

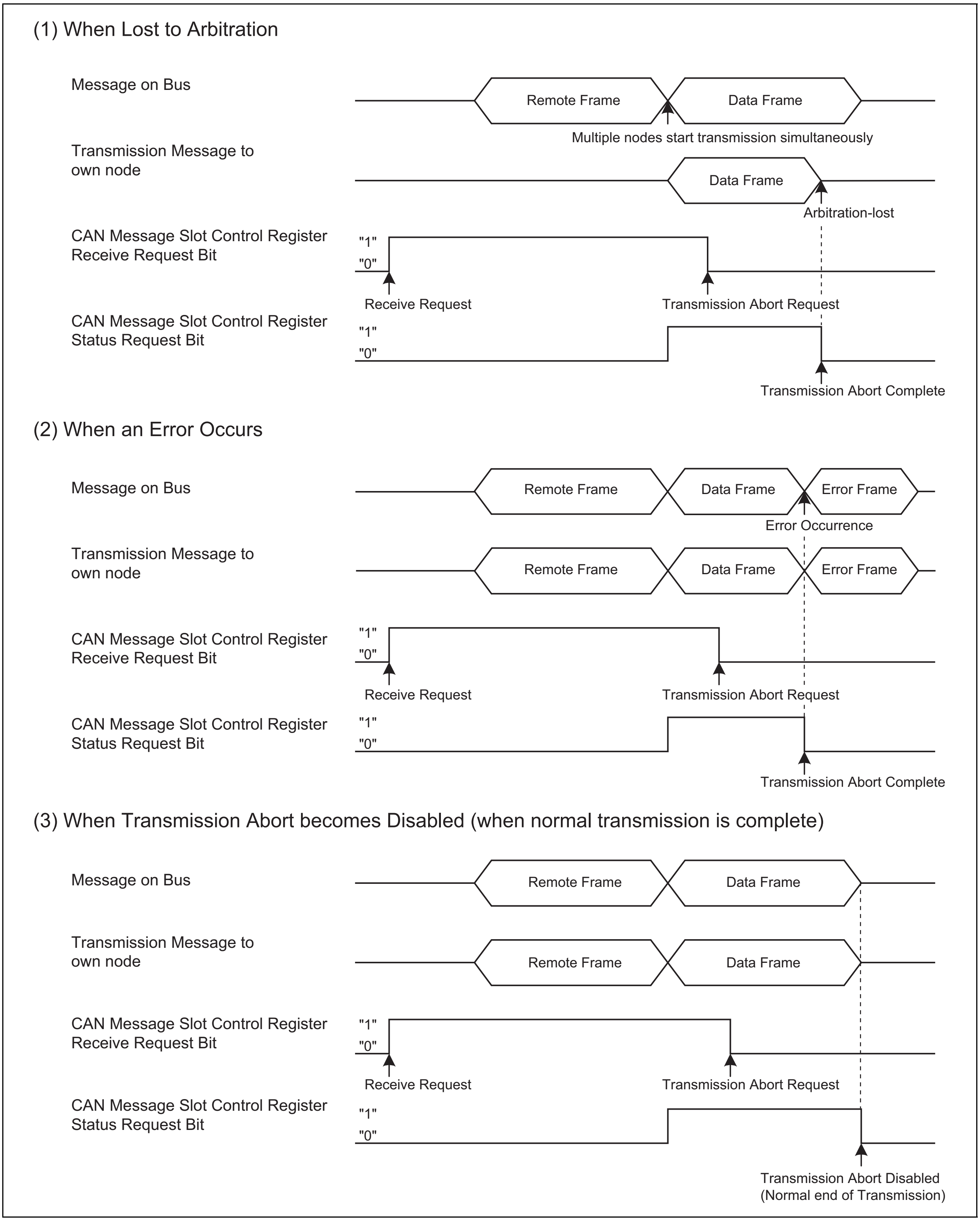


Figure 5.1.3 Transmission Aborted during Data Frame Transmission After Remote Frame Reception

5.2 Basic CAN Mode

CAN module comprises 16 slots per channel, each slot can be set as a transmit or receive slot. This is called the standard operating mode.
The basic CAN mode is for operation of slots 14 and 15 as receive slots, and slots 0 to 13 for normal operating mode.
In the basic mode, received messages are stored reciprocally in slots 14 and 15.
By setting the same ID for two slots and making the same settings for the respective mask registers, the possibility of message lost can be greatly reduced when receiving a frame with many ID's.
In the normal operating mode, by setting the CAN message slot control register, each slot can manage only one frame type, either the data frame or remote frame. However, in basic CAN mode, slots 14 and 15 can receive both frame types at the same time. The received type can be distinguished by the remote active bit of the CAN message slot control register; when a data frame is received the bit is cleared to "0" and when a remote frame is received the bit is set to "1".
When using the basic CAN mode, set the basic CAN mode bit of the CAN control register to "1".

When using the basic CAN mode, follow the procedure below.

- Set the ID for slot 14 and 15 and the local mask registers A, B. (Same settings recommended)
- Set the frame type (Standard/Extended) in CAN extended ID register for slot 14 and 15. (Same type recommended)
- Set the message slot control register for slots 14 and 15 to receive data frames.
- Basic CAN mode bit set to "1".

When using the basic CAN mode, note the following.

- Do not change the setting of the basic CAN mode bit when operating CAN (the CAN reset status bit of the CAN status register is "0").
- The auto response function cannot be used even when slots 14 and 15 receive a remote frame.
- When receiving a message, if another message is received at the same slot, the new message will overwrite the previous one.
- Even in the basic CAN mode slots 0 to 13 can be used in same way as during normal operation.

5.3 Loopback Function

Normally, in CAN a self transmitted frame cannot be received. If the loopback function is enabled, if a self-transmitted frame and receive slot with a matching ID exist, then that frame can be received.
When using the loopback mode, set the loopback mode bit of the CAN control register to "1".

When using the loopback function, note the following.

- The ACK corresponding to the transmit frame is not returned.
- During CAN operation (the CAN reset status bit of the CAN status register is "0"), do not change the setting of the loopback mode bit.

5.4 Single-Shot Mode

Normally, in CAN when there is a transmission failure due to arbitration-lost or transmission error, the operation continues until transmission succeeds. That re-transmission can be controlled at each slot by the CAN single-shot mode control register.
If a slot is set to the single-shot mode and transmission fails, re-transmission will not occur.

When using the single-shot mode, note the following.

- When changing the bit setting of the CAN single-shot mode control register, the value of the CAN message slot control register for the corresponding slot must be H'00.

5.5 Timestamp Function

CAN module has an internal 16 bit up-count register. The count cycle can be selected from 1-, 2-, 3-, or 4-division of the CAN bus bit clock by the timestamp prescaler bit of the CAN control register.

When transmission or reception is complete, the count register value is captured and that value is stored in the message slot.

The counter will start operating when the CAN reset bit of the CAN control register is cleared to “0”.

When using the timestamp function, note the following.

- During CAN operation (the CAN reset status bit of the CAN status register is “0”), do not change the setting of the time stamp prescaler bit.
- By setting the CAN reset bit of the CAN control register to “1”, the protocol control is reset and can be initialized to H'0000. Furthermore, by setting the timestamp counter reset bit to “1”, CAN module can be initialized to H'0000 while in operation.
- In the loopback mode, when multiple slots have the same ID, and receive is complete, the timestamp value is stored in the corresponding slot (when transmission is complete, the timestamp value is not stored).
- The count cycle of the CAN timestamp count register changes with the CAN re-synchronization function.

5.6 Return Bus Off Function

If the CAN module is in the bus off state, transmission or reception is not possible.

For transmission or reception, it is necessary to detect the recessive bit 128 times consecutively for 11 bits on the CAN bus and enter the error active state. However, when a message needs to be urgently transmitted, it is necessary to immediately establish the error active state. The return bus off function is for setting the error active state without waiting for a long period described above.

With the return bus off function, If the return bus off bit of the CAN control register is set to “1” (the request to clear the CAN Error Counter), the CAN received error count register and the CAN transmission error count register are cleared to H'0000, and the state of the CAN module can be forcibly returned to the error active state. The return bus off bit is automatically cleared after transition to the error active state.

When using the return bus off function, note the following.

- After clearing the error counter and after detecting the recessive bit consecutively for 11 bits on the CAN bus, communication becomes possible.

5.7 Self-Diagnostic Function

The CAN module internally connects the CTX and CRX. The CAN communication using the CAN module alone is possible in combination with the loopback function. In the self-diagnostic mode, the CTX pin output is fixed to a high level during transmission.

The self-diagnostic mode is set using the CAN operation mode select bit of the CAN mode register.

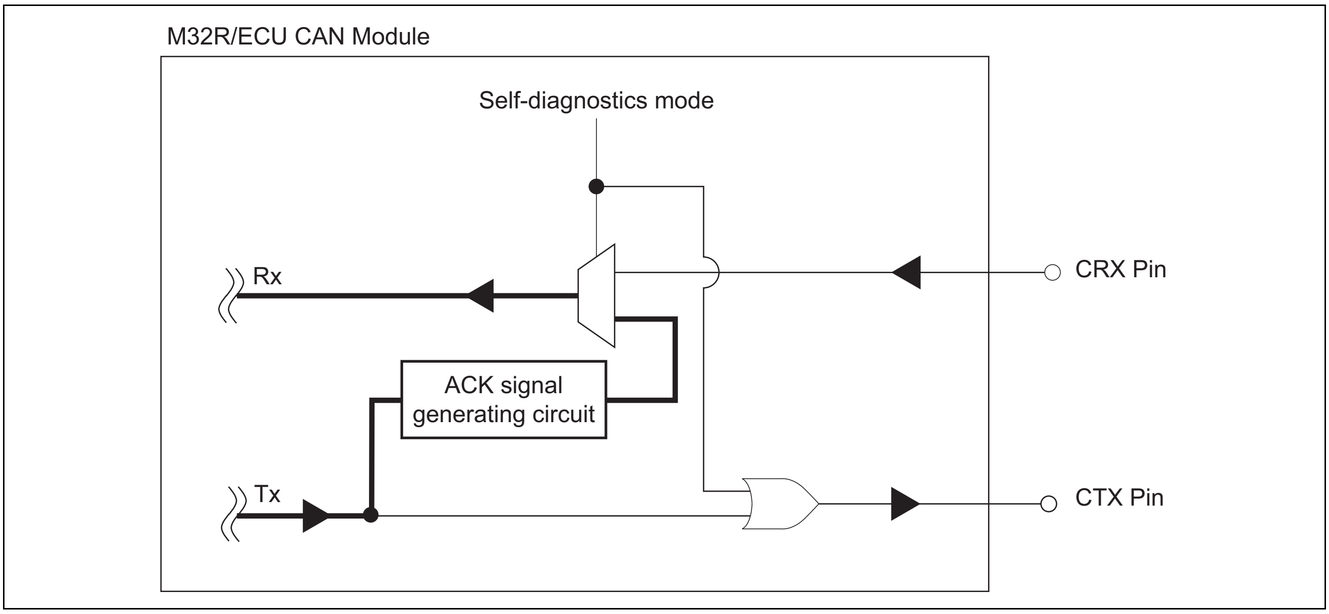


Figure 5.7.1 Self-Diagnostic Mode (Image Diagram)

5.8 Bus Monitor Mode

The bus monitor mode is for receive operation only. In the bus monitor mode the CTX pin output is fixed to a high level and the ACK and error frame cannot be returned.

The bus monitor mode is set using the CAN operation mode select bit of the CAN mode register.

When using the bus monitor mode, note the following.

- In the bus monitor mode, output of the transmit request is disabled.
- In the bus monitor mode, the ACK bit is treated as “Don't care.”

5.9 DMA Transfer Function

In the CAN0, DMA (DMA6 and DMA7) transfer requests can be generated, and in the CAN1, DMA (DMA8 and DMA9) transfer requests can be generated.

The transfer request sources for the DMA6 and the DMA8 can be selected from the following.

(1) Slot 0 transmission failure (error due to arbitration lost or a transmission failure).
(2) Slot 15 completion of transmission or reception.

Note:

- When slot 15 is set for the transmission of a remote frame, for each event of remote frame transmission completion and data frame reception completion, a DMA transfer request occurs.
- When slot 15 is set for the reception of a remote frame (auto-response), for each event of the remote frame reception completion and data frame reception completion, a DMA transfer request occurs.

The transfer request sources for the DMA7 and the DMA9 can be selected from the following.

(1) Slot 1 transmission failure (failure due to arbitration-lost or transmission error).
(2) Slot 14 completion of transmission or reception.

Note:

- When slot 14 is set for the transmission of a remote frame, for each event of remote frame transmission completion and data frame reception completion, a DMA transfer request occurs.
- When slot 14 is set for receiving a remote frame (auto response), for each event of remote frame reception completion and data frame transmission completion, a DMA transfer request occurs.

5.10 Acceptance Filter

This function receives messages with an ID within a specified range by filtering the ID of the received message using hardware.

5.10.1 Operation of the Acceptance Filter

The acceptance filter uses the global mask register (slots 0 to 13), local mask register A (slot 14), and local mask register B (Slot 15) for filtering.

Note: Make changes to the mask register when the receive request is not set in the slot .

Figure 5.10.1 shows the description of operation for the acceptance filter.

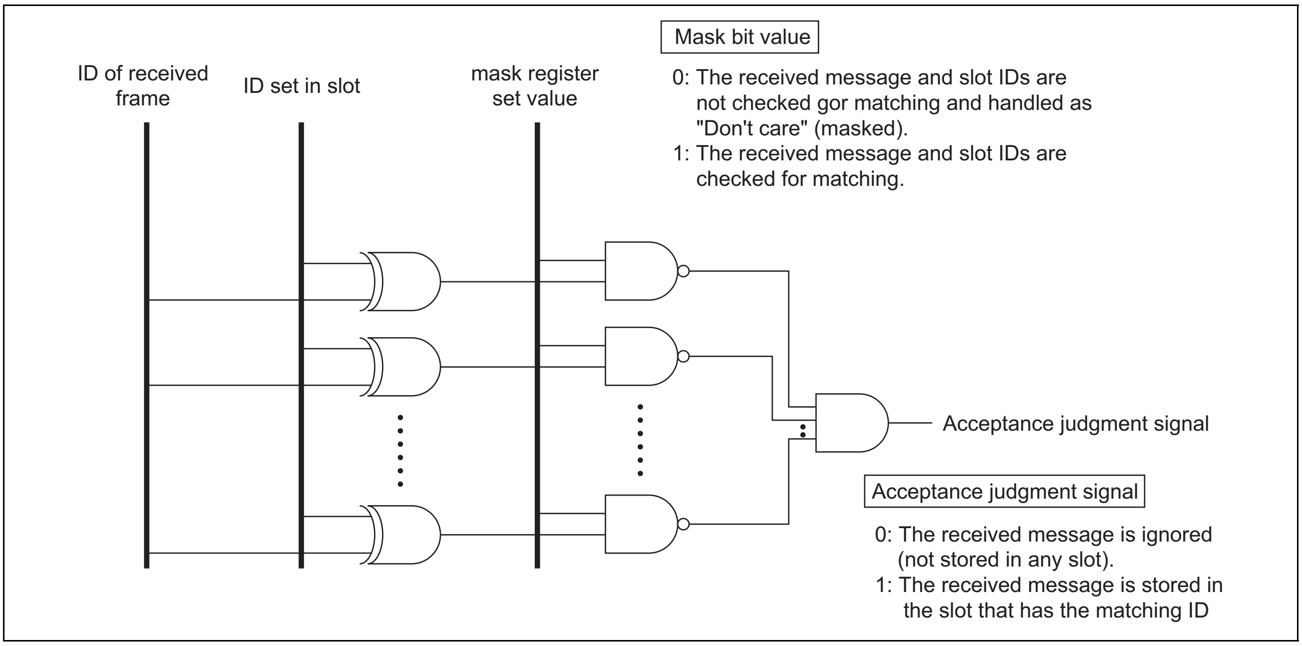


Figure 5.10.1 Operation Description for the Acceptance Filter

5.10.2 Examples Using the Acceptance Filter

(1) Example 1

The settings for each mask register when the CAN0 slot 0 receives a standard data frame of ID H'123, or receives a standard remote frame, are shown in table 5.10.1.

Table 5.10.1 Acceptance Filter Usage Example 1

Mask Register		C0GMSKS0 SID0-4	C0GMSKS1 SID5-10	C0GMSKE0 EID0-3	C0GMSKE1 EID4-11	C0GMSKE2 EID12-17
Mask register setting value		11111	111111	XXXX	XXXXXXXX	XXXXXX
Slot 0 ID setting value		00100	100011	XXXX	XXXXXXXX	XXXXXX
Received message	ID H'123	00100	100011	—	—	—

Note: X is treated as "Don't care"

(2) Example 2

The settings of each mask register when the CAN0 slot 0 receives two standard data frames ID H'122 and ID H'123, or when it receives a standard remote frame, are shown in table 5.10.2.

Table 5.10.2 Acceptance Filter Usage Example 2

Mask Register		C0GMSKS0 SID0-4	C0GMSKS1 SID5-10	C0GMSKE0 EID0-3	C0GMSKE1 EID4-11	C0GMSKE2 EID12-17
Mask register setting value		11111	111110	XXXX	XXXXXXXX	XXXXXX
Slot 0 ID setting value		00100	10001X	XXXX	XXXXXXXX	XXXXXX
Received message	ID H'122	00100	100010	—	—	—
	ID H'123	00100	100011	—	—	—

(3) Example 3

The settings for each mask register when the CAN0 slot 0 receives an extended data frame with an ID H'12345678, or when it receives an extended remote frame, are shown in table 5.10.3.

Table 5.10.3 Acceptance Filter Usage Example 3

Mask Register		C0GMSKS0 SID0-4	C0GMSKS1 SID5-10	C0GMSKE0 EID0-3	C0GMSKE1 EID4-11	C0GMSKE2 EID12-17
Mask register setting value		11111	111111	1111	11111111	111111
Slot 0 ID setting value		10010	001101	0001	01011001	111000
Received message	ID H'12345678	10010	001101	0001	01011001	111000

6. Reference Documents

- 32176 Group User's Manual (Rev.1.01)
- M32R Family Software Manual (Rev.1.20)
- M3T-CC32R V.4.30 User’s Manual (Compiler)
- M3T-CC32R V.4.30 User’s Manual (Assembler)

(Please get the latest one from Renesas Technology Corp. website.)

- Robert Bosch GmbH/Bosch's CAN: http://www.can.bosch.com/
- CiA: CAN in Automation: http://www.can-cia.de/

7. Website and Support Center

- Renesas Technology Corp. website.

  http://www.renesas.com/

- Inquires for all Renesas products and technical inquiries for the M32R Family products:

  Customer Support Center: csc@renesas.com

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Dec.09.05	—	First edition issued