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Renesas Electronics Corporation

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H8SX Family

Multiprocessor Communication

Introduction

The multiprocessor communication function of the serial communications interface (SCI) is used to transmit data to each processor.

Target Device

H8SX/1582F

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1. Specifications

Using the multiprocessor communication function, data H'B8 is transmitted to receiving station A and data H'DE is transmitted to receiving station B.

In multiprocessor communication, data can be transferred to the desired receiving station among the multiple serially-connected stations by transmitting an ID, uniquely assigned to each receiving station, followed by data. A receiving station compares the ID sent first with its own ID and receives the data that comes next only if the IDs match. If the IDs do not match, the receiving station does not receive the data that follows.

- Figure 1 shows an example of connection for inter-processor communication using multiprocessor format communication.
- The communication format is shown in table 1. A break is output when data transmission has finished.
- In this sample task, asynchronous transmission and reception of 128 bytes of data is controlled by software through the interrupt exception processing.

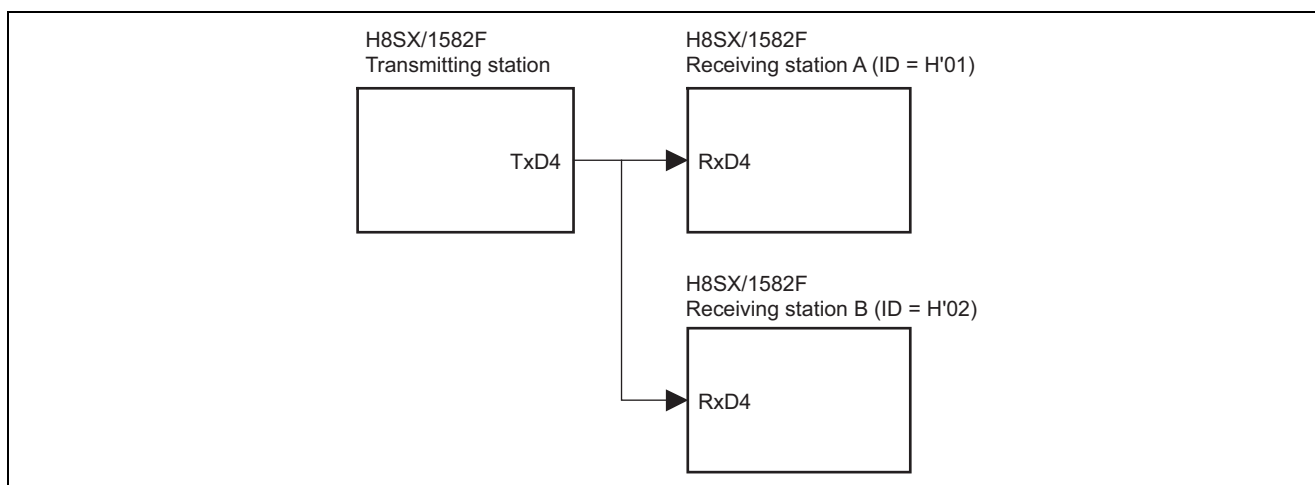


Figure 1 Inter-Processor Communication Using Multiprocessor Format Communication

Table 1 Multiprocessor Transmit Format in Asynchronous Mode

Format Item	Setting
Pφ	16 MHz
Bit rate	19200 bps
Data length	8 bits
Parity bit	None
Stop bit	1 bit
Multiprocessor bit	1 bit
Serial/parallel conversion format	LSB-first

2. Conditions for Application

Table 2 Conditions for Application

Item	Contents
Operating frequency	Input clock: 5 MHz System clock (I ϕ): 40 MHz Peripheral module clock (P ϕ): 20 MHz External bus clock (B ϕ): 20 MHz
Operating mode	Mode 3 (MD1 = 1, MD0 = 1)
Development tool	High-performance Embedded Workshop Version 4.00.02
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler Version 6.01.00 (from Renesas Technology Corp.)
Compile option	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3, -speed = (register, shift, struct, expression)

Table 3 Section Settings

Address	Section Name	Description
H'001000	P	Program area
	C	Constant area
H'FF9000	B	Uninitialized data area (RAM area)

3. Description of Modules Used

3.1 Description of SCI_4

In this sample task, serial data transmission is performed in asynchronous mode using the SCI_4. Figure 2 shows a block diagram of the SCI_4 and the functions regarding figure 2 are described below.

- On-chip peripheral module clock P ϕ
P ϕ is a reference clock used to drive the on-chip peripheral functions and is generated by the clock pulse generator.
- Receive shift register_4 (RSR_4)
RSR_4 is a register used to receive serial data. When RSR_4 receives one frame of serial data input from the RxD4 pin, that data is automatically transferred to receive data register_4 (RDR_4). RSR_4 cannot be directly accessed by the CPU.
- Receive data register_4 (RDR_4)
RDR_4 is an 8-bit register that stores receive data. When one frame of data has been received, the data is automatically transferred from RSR_4 to RDR_4. RSR_4 and RDR_4 form a double buffer, thus enabling continuous reception of data. Since RDR_4 is a register used only for data reception, RDR_4 can only be read by the CPU.
- Transmit shift register_4 (TSR_4)
TSR_4 is a register used to transmit serial data. When transmitting data, data is first transferred from transmit data register_4 (TDR_4) to TSR_4, and then the transmit data is output from the TxD4 pin. TSR_4 cannot be directly accessed by the CPU.
- Transmit data register_4 (TDR_4)
TDR_4 is an 8-bit register that stores transmit data. When TSR_4 is detected as empty, the data written to TDR_4 is automatically transferred to TSR_4. Since TDR_4 and TSR_4 form a double buffer, if the next data has been written to TDR_4 when one frame of data is transmitted, the written data is transferred to TSR_4, thus enabling continuous transmission of data. TDR_4 can always be read from or written to by the CPU. However, be sure to confirm that the TDRE bit in serial status register_4 (SSR_4) is 1 before writing to TDR_4.
- Serial mode register_4 (SMR_4)
SMR_4 is an 8-bit register used to set the serial data transfer format and select the clock source for the on-chip baud rate generator.
- Serial control register_4 (SCR_4)
SCR_4 is a register used to enable or disable transmission/reception or interrupt requests, and to select the transmit/receive clock source.
- Serial status register_4 (SSR_4)
SSR_4 consists of the SCI_4 status flags and multiprocessor bits for transmission/reception. The TDRE, RDRF, ORER, PER, and FER bits in this register can only be cleared.
- Smart card mode register_4 (SCMR_4)
SCMR_4 is a register used to select the smart card interface and its format. In this sample task, this register is set to select normal asynchronous or clock synchronous mode.

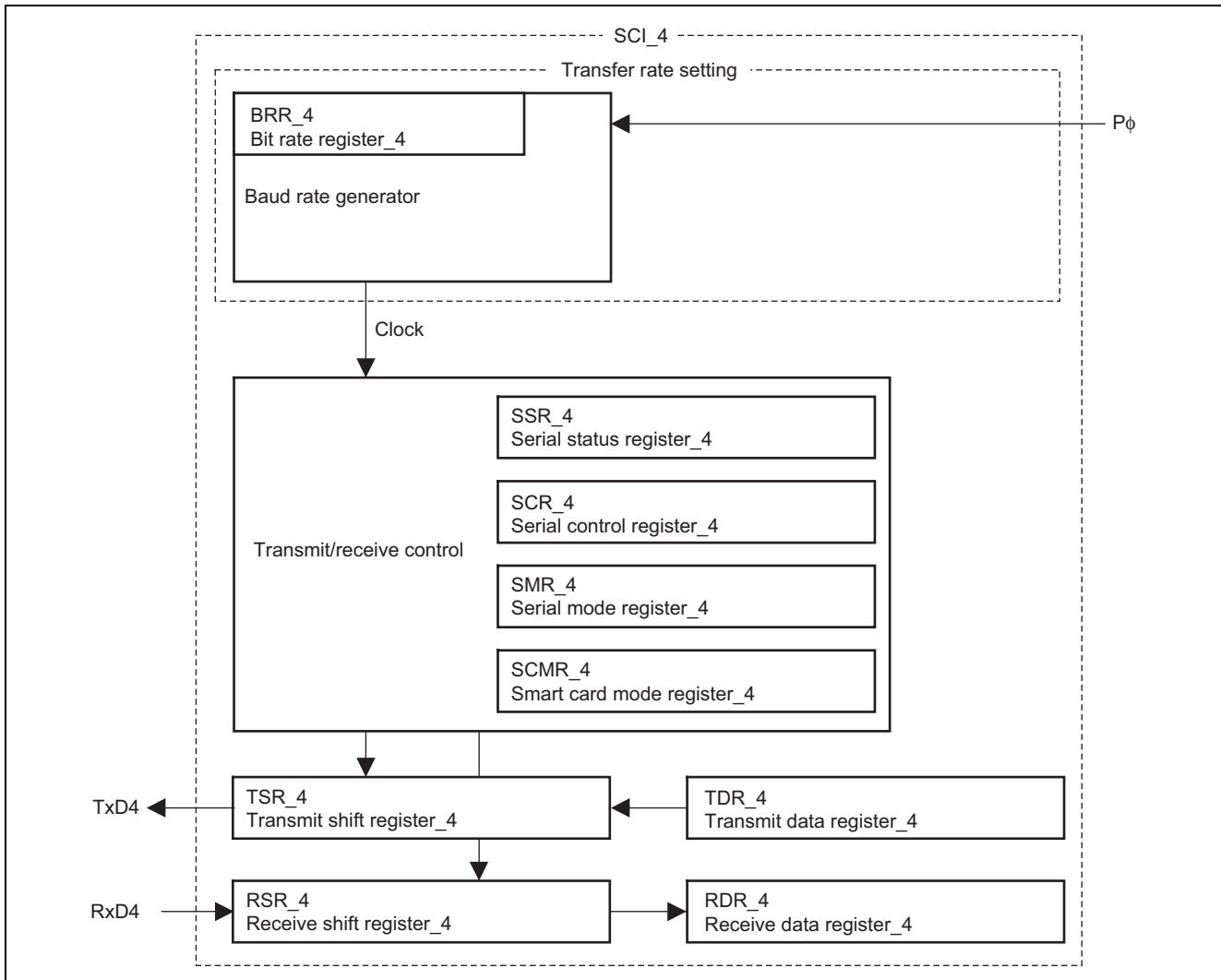


Figure 2 Block Diagram of SCI_4

3.2 Multiprocessor communication function

Multiprocessor communication is to perform data transmission and reception between multiple processors via a shared communication line by serial communication in asynchronous mode with a format (multiprocessor format) in which the multiprocessor bit is added.

When performing multiprocessor communication, a unique ID code is assigned to each receiving station. A serial communication cycle consists of an ID transmit cycle which specifies the receiving station and a data transmit cycle which transmits data to the specified receiving station.

The ID transmit cycle and data transmit cycle are distinguished by the multiprocessor bit. The multiprocessor bit is 1 for the ID transmit cycle and 0 for the data transmit cycle.

The transmitting station first transmits the ID code of the receiving station to which serial data is to be transmitted with a 1-valued multiprocessor bit added. Next, the transmitting station transmits the data with a 0-valued multiprocessor bit added.

A receiving station receives the communication data in which the multiprocessor bit is 1. It compares it with its own ID, and receives the subsequently transmitted data on a match. If the IDs do not match, the receiving station ignores the communication data until communication data with a 1-valued multiprocessor bit is transmitted again.

The transmit/receive format can be selected from four types when the multiprocessor format is specified. In these formats, parity bit setting is not available.

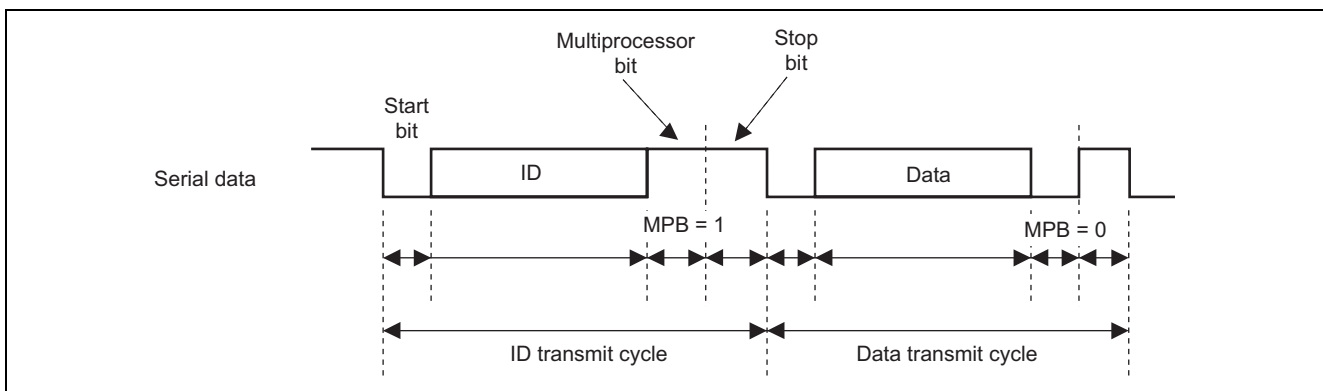


Figure 3 Multiprocessor Format

Table 4 Multiprocessor Communication Format

SMR			Multiprocessor communication format and frame length													
CHR	MP	STOP	1	2	3	4	5	6	7	8	9	10	11	12		
0	1	0	START	8-bit data						MPB	STOP	*				
0	1	1	START	8-bit data						MPB	STOP	STOP				
1	1	0	START	7-bit data					MPB	STOP						
1	1	1	START	7-bit data					MPB	STOP	STOP					

[Legend]

START: Start bit

STOP: Stop bit

MPB: Multiprocessor bit

Note: * This format is selected in this sample task.

4. Description of Operation

4.1 Overview of Operation

Receive operation when the IDs do not match is shown in figure 4 and receive operation when the IDs match is shown in figure 5. The hardware processing and software processing are shown in tables 5 and 6 for describing figures 4 and 5, respectively.

Transmit operation is the same as that for data transmission in asynchronous mode except for setting the MPBT bit in SSR_4 to 1 when transmitting the ID.

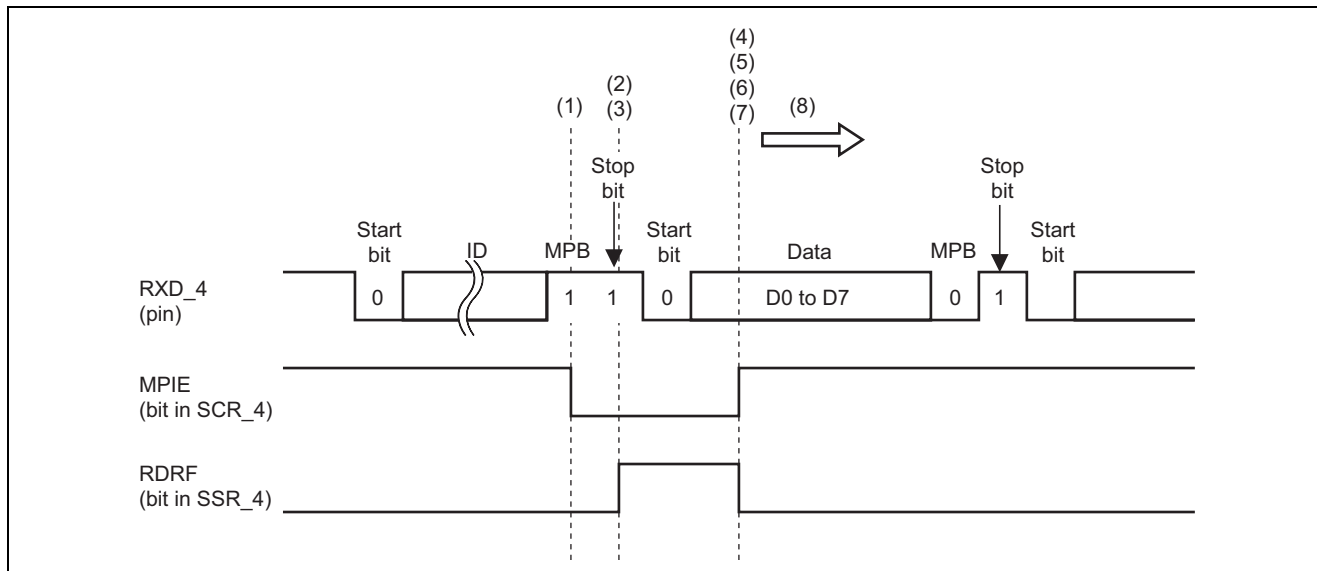


Figure 4 Receive Operation with Non-Matching IDs

Table 5 Hardware and Software Processing

	Hardware Processing	Software Processing
(1)	Clear the MPIO flag in SCR_4 to 0 (ID data reception).	—
(2)	RSR_4 receives serial data and transfers it to RDR_4.	—
(3)	Set the RDRF flag in SSR_4 to 1.	—
(4)	—	Read the data in RDR_4.
(5)	—	Clear the RDRF flag in SSR_4 to 0.
(6)	—	Compare the data read from RDR_4 with the ID of its own.
(7)	—	Set the MPIO flag in SCR_4 to 1.
(8)	Does not receive data because the MPB bit of the data sent while the MPIO flag being 1 is 0.	—

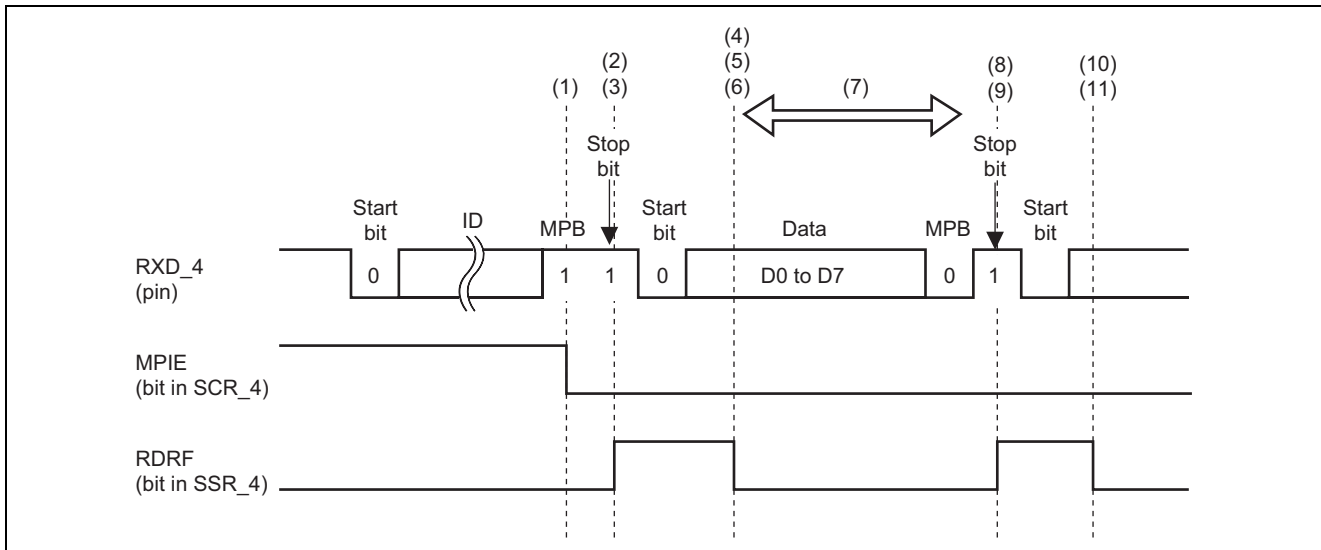


Figure 5 Receive Operation with Matching IDs

Table 6 Hardware and Software Processing

	Hardware Processing	Software Processing
(1)	Clear the MPIE flag in SCR_4 to 0 (ID data reception).	—
(2)	RSR_4 receives serial data and transfers it to RDR_4.	—
(3)	Set the RDRF flag in SSR_4 to 1.	—
(4)	—	Read the data in RDR_4.
(5)	—	Clear the RDRF flag in SSR_4 to 0.
(6)	—	Compare the data read from RDR_4 with the ID of its own.
(7)	Receive data.	—
(8)	RSR_4 receives serial data and transfers it to RDR_4.	—
(9)	Set the RDRF flag in SSR_4 to 1.	—
(10)	—	Read the data in RDR_4.
(11)	—	Clear the RDRF flag in SSR_4 to 0.

5. Description of Software

5.1 List of Functions

Table 7 List of Functions

Function Name	Functions
init	Initialization routine Cancels module stop mode, sets the clocks, and calls the main function.
main	Main routine Makes the initial settings for the SCI and performs communication with multiple devices at a transfer rate of 19200 bps.
sci4_rcv1byte	1-byte reception by receiving station Checks the received ID code and receives one byte of data.
sci4_trs1byte	1-byte transmission by transmitting station Transmits an ID code and one byte of data.

5.2 RAM Usage

Table 8 RAM Usage

Type	Label Name	Description	Used In
unsigned char	r_buf	Stores the receive data	main

5.3 Constants

Table 9 List of Constants

Constant Name	Description	Used In
ID1	ID number of receiving station A Setting: H'01	main
ID2	ID number of receiving station B Setting: H'02	main

5.4 Data Table

Table 10 Data Table

Type	Array Name	Description	Used In
unsigned char	t_buf[2]	Stores the transmit data t_buf[0] = H'B8, t_buf[1] = H'DE	main

5.5 Macro Definition

Table 11 Macro Definition

Identifier	Description	Used In
TRSSTA	Generates a program for the transmitting station	main
RCVSTA_A	Generates a program for receiving station A	main
RCVSTA_B	Generates a program for receiving station B	main

5.6 Description of Functions

5.6.1 init Function

(1) Functional overview

Initialization routine which cancels module stop mode, sets the clocks, and calls the main function.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. The setting values shown below are the values used in this sample task and differ from their initial values.

- System clock control register (SCKCR) Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Function
10	ICK2	0	R/W	System Clock (I ϕ) Select
9	ICK1	0	R/W	These bits select the system clock frequency. The CPU, DMAC, and DTC modules are driven by the system clock. 000: Input clock \times 8
8	ICK0	0	R/W	
6	PCK2	0	R/W	Peripheral Module Clock (P ϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module clock. 001: Input clock \times 4
4	PCK0	1	R/W	
2	BCK2	0	R/W	External Bus Clock (B ϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock. 001: Input clock \times 4
0	BCK0	1	R/W	

- MSTPCRA, MSTPCRB, and MSTPCRC are the registers that control module stop mode. Setting the bits in these registers places the corresponding modules in module stop mode, and clearing the bits cancels module stop mode.

- Module stop control register A (MSTPCRA) Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Function
15	ACSE	0	R/W	All-module-clock-stop mode enable Enables or disables transition to all-module-clock-stop mode. If this bit is set to 1, all-module-clock-stop mode is entered when the SLEEP instruction is executed by the CPU while all the modules under control of the MSTPCR registers are placed in module stop mode. In all-module-clock-stop mode, even the bus controller and I/O ports are stopped to reduce the supply current. 0: Disables transition to all-module-clock-stop mode. 1: Enables transition to all-module-clock-stop mode.
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
4	MSTPA4	1	R/W	A/D converter (unit 1)
3	MSTPA3	1	R/W	A/D converter (unit 0)
1	MSTPA1	1	R/W	16-bit timer pulse unit (TPU channels 11 to 6)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

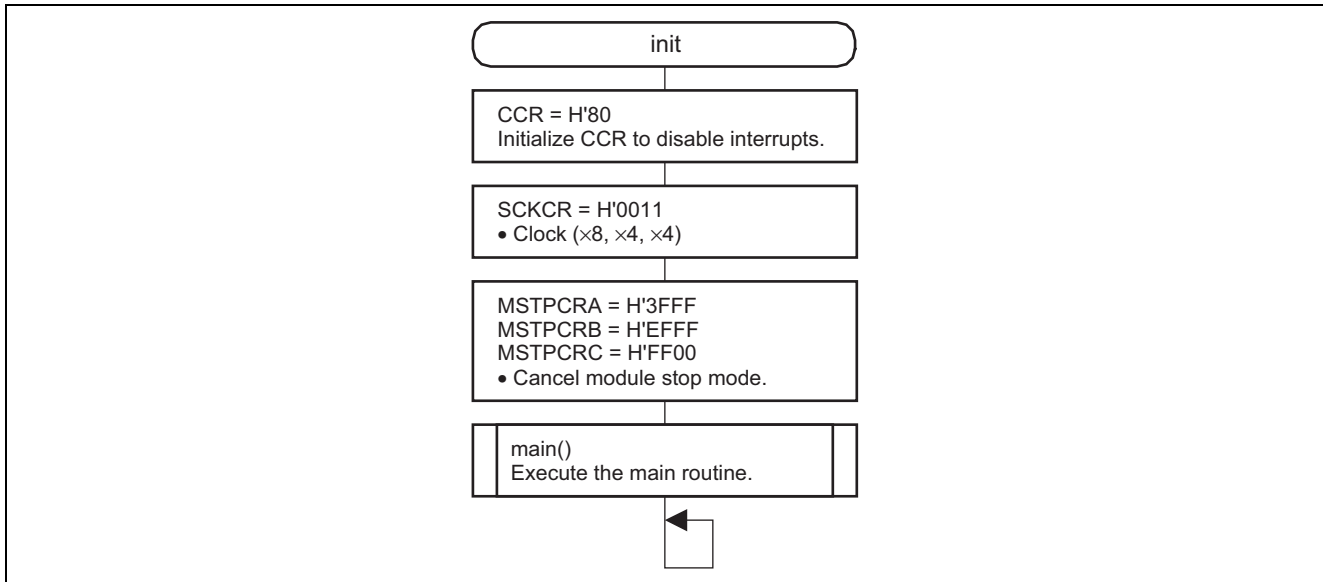
- Module stop control register B (MSTPCRB) Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Function
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	0	R/W	Serial communication interface_4 (SCI_4)
11	MSTPB11	1	R/W	Serial communication interface_3 (SCI_3)

- Module stop control register C (MSTPCRC) Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Function
10	MSTPC10	1	R/W	Synchronous serial communication unit 2 (SSU_2)
9	MSTPC9	1	R/W	Synchronous serial communication unit 1 (SSU_1)
8	MSTPC8	1	R/W	Synchronous serial communication unit 0 (SSU_0)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF9000 to H'FFBFFF)
0	MSTPC0	0	R/W	Always write the same value to the MSTPC1 and MSTPC0 bits.

(5) Flowchart



5.6.2 main Function

(1) Functional overview

Main routine which transmits and receives one byte of data.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. The setting values shown below are the values used in this sample task and differ from their initial values.

- Serial mode register_4 (SMR_4) Address: H'FFFE90

Bit	Bit Name	Setting	R/W	Function
7	C/ \bar{A}	0	R/W	Communication Mode 0: Operates in asynchronous mode 1: Operates in clock synchronous mode
6	CHR	0	R/W	Character Length 0: 8-bit length data is transmitted 1: 7-bit length data is transmitted
3	STOP	0	R/W	Stop Bit Length Selects the stop bit length for transmission. 0: 1 stop bit 1: 2 stop bits In reception, only the first stop bit is checked, regardless of the setting of this bit. If the second stop bit is 0, it is treated as the start bit of the next transmit frame.
2	MP	1	R/W	Multiprocessor Mode 0: Multiprocessor function is disabled 1: Multiprocessor function is selected
1	CKS1	0	R/W	Clock Select 1, 0
0	CKS0	0	R/W	00: Clock source of on-chip baud rate generator is P ϕ .

- Bit rate register_4 (BRR_4) Address: H'FFFE91
Function: 8-bit register for adjusting the bit rate. When P ϕ = 20 MHz, CKS1 and CKS0 bits = B'00 in SMR_4, and BRR_4 = 32, the bit rate is set at 19200 bps.
Setting: 32

- Serial control register_4 (SCR_4)

Address: H'FFFE92

Bit	Bit Name	Setting	R/W	Function
7	TIE	0	R/W	Transmit Interrupt Enable 0: TXI interrupt is disabled 1: TXI interrupt is enabled
6	RIE	0	R/W	Receive Interrupt Enable 0: RXI and ERI interrupts are disabled 1: RXI and ERI interrupts are enabled
5	TE	0	R/W	Transmit Enable 0: Transmission is disabled 1: Transmission is enabled
4	RE	0	R/W	Receive Enable 0: Reception is disabled 1: Reception is enabled
3	MPIE	0	R/W	Multiprocessor Interrupt Enable (Valid when the MP bit in SMR is 1 in asynchronous mode) When this bit is set to 1, receive data whose multiprocessor bit is 0 is skipped and setting of the RDRF, FER, and OER status flags in SSR is disabled. When receiving data whose multiprocessor bit is 1, this bit is automatically cleared and normal receive operation is resumed. For details, refer to section 13.5, Multiprocessor Communication Function, in the hardware manual. When data with a 0-valued multiprocessor bit is being received, transfer of receive data from RSR to RDR, receive error detection, and setting of the RDRF, FER, and OER flags in SSR are not performed. When data with a 1-valued multiprocessor bit is received, the MPB bit in SSR is set to 1, the MPIE bit is automatically cleared to 0, RXI and ERI interrupt requests are enabled (when the TIE and RIE bits in SCR are set to 1), and setting of the RDRF, FER and ORER flags is enabled.
2	TEIE	0	R/W	Transmit-End Interrupt Enable 0: TEI interrupt is disabled 1: TEI interrupt is enabled
1	CKE1	0	R/W	Clock Enable 1, 0
0	CKE0	0	R/W	These bits select the clock source. 00: On-chip baud rate generator

- Transmit data register_4 (TDR_4)

Address: H'FFFE93

Function: 8-bit readable/writable register that stores transmit data

Setting: Undefined

- Serial status register_4 (SSR_4)

Address: H'FFFE94

Bit	Bit Name	Setting	R/W	Function
7	TDRE	Undefined	R/(W)*	<p>Transmit Data Register Empty</p> <p>Indicates whether TDR contains transmit data.</p> <p>[Setting conditions]</p> <ul style="list-style-type: none"> When the TE bit in SCR is 0 When data is transferred from TDR to TSR <p>[Clearing conditions]</p> <ul style="list-style-type: none"> When 0 is written to TDRE after reading TDRE = 1 When the DMAC transfers transmit data to TDR due to a TXI interrupt
6	RDRF	0	R/(W)*	<p>Receive Data Register Full</p> <p>Indicates whether RDR contains receive data.</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> When reception is finished successfully, and receive data is transferred from RSR to RDR <p>[Clearing conditions]</p> <ul style="list-style-type: none"> When 0 is written to RDRF after reading RDRF = 1 When the DMAC or DTC transfers data from RDR due to an RXI interrupt <p>Even if the RE bit in SCR is cleared to 0, the RDRF flag is unaffected and its previous state retained.</p> <p>If reception of the next data is completed while the RDRF flag is still set to 1, an overrun error occurs and the received data is lost.</p>
5	ORER	0	R/(W)*	<p>Overrun Error</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> When an overrun error occurs during reception <p>[Clearing condition]</p> <ul style="list-style-type: none"> When 0 is written to ORER after reading ORER = 1
4	FER	0	R/(W)*	<p>Framing Error</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> When a framing error occurs during reception <p>[Clearing condition]</p> <ul style="list-style-type: none"> When 0 is written to FER after reading FER = 1
3	PER	0	R/(W)*	<p>Parity Error</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> When a parity error occurs during reception <p>[Clearing condition]</p> <ul style="list-style-type: none"> When 0 is written to PER after reading PER = 1

Bit	Bit Name	Setting	R/W	Function
2	TEND	Undefined	R	Transmit End [Setting conditions] <ul style="list-style-type: none"> When the TE bit in SCR is 0 If the TDRE bit is 1 when the last bit in the transmit character is transmitted [Clearing conditions] <ul style="list-style-type: none"> When 0 is written to TDRE after reading TDRE = 1 When the DMAC writes transmit data to TDR due to a TXI interrupt
1	MPB	Undefined	R	Multiprocessor Bit Stores the multiprocessor bit value in the receive frame. This bit value does not change when the RE bit in SCR is 0.
0	MPBT	Undefined	R/W	Multiprocessor Bit Transfer Sets the multiprocessor bit value that is to be added to the transmit frame.

Note: * Only 0 can be written to clear the flag.

- Receive data register_4 (RDR_4) Address: H'FFFE95
Function: 8-bit read-only register that stores receive data
Setting: Undefined

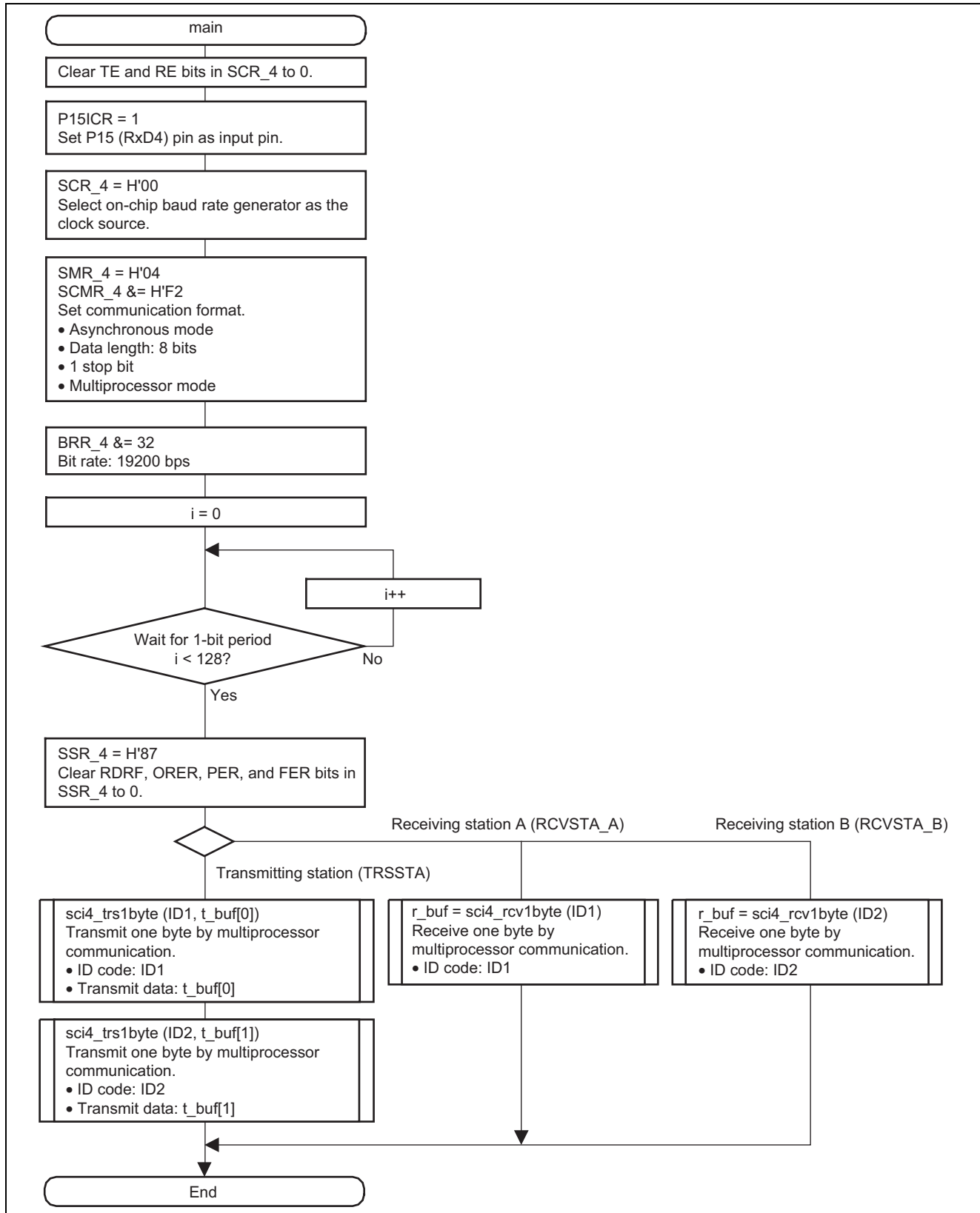
- Smart card mode register_4 (SCMR_4) Address: H'FFFE96

Bit	Bit Name	Setting	R/W	Function
0	SMIF	0	R/W	Smart Card Interface Mode Select 0: Operates in normal asynchronous or clock synchronous mode 1: Operates in smart card interface mode

- Port 1 input buffer control register (P1ICR) Address: H'FFFB90

Bit	Bit Name	Setting	R/W	Function
5	P15ICR	1	R/W	0: Input buffer of pin P15 is disabled. Input signal is fixed high. 1: Input buffer of pin P15 is enabled. Pin state is reflected in the peripheral module.

(5) Flowchart



5.6.3 sci4_rcv1byte Function

(1) Functional overview

Checks the received ID code and receives 1-byte data.

(2) Argument

Type	Variable Name	Description
unsigned char	id	ID code

(3) Return value

Type	Description
unsigned char	Receive data

(4) Description of internal registers

The internal registers used in this sample task are described below. The setting values shown below are the values used in this sample task and differ from their initial values.

- Serial control register_4 (SCR_4) Address: H'FFFE92

Bit	Bit Name	Setting	R/W	Function
4	RE	0	R/W	Receive Enable 0: Reception is disabled 1: Reception is enabled
3	MPIE	0	R/W	Multiprocessor Interrupt Enable (Valid when the MP bit in SMR is 1 in asynchronous mode) When this bit is set to 1, receive data whose multiprocessor bit is 0 is skipped and setting of the RDRF, FER, and OER status flags in SSR is disabled. When receiving data whose multiprocessor bit is 1, this bit is automatically cleared and normal receive operation is resumed. For details, refer to section 13.5, Multiprocessor Communication Function, in the hardware manual. When data including MPB = 0 is being received, transfer of receive data from RSR to RDR, receive error detection, and setting of the RDRF, FER, and OER flags in SSR are not performed. When data including MPB = 1 is received, the MPB bit in SSR is set to 1, the MPIE bit is automatically cleared to 0, RXI and ERI interrupt requests are enabled (when the TIE and RIE bits in SCR are set to 1), and setting of the FER and ORER flags is enabled.

- Serial status register_4 (SSR_4)

Address: H'FFFE94

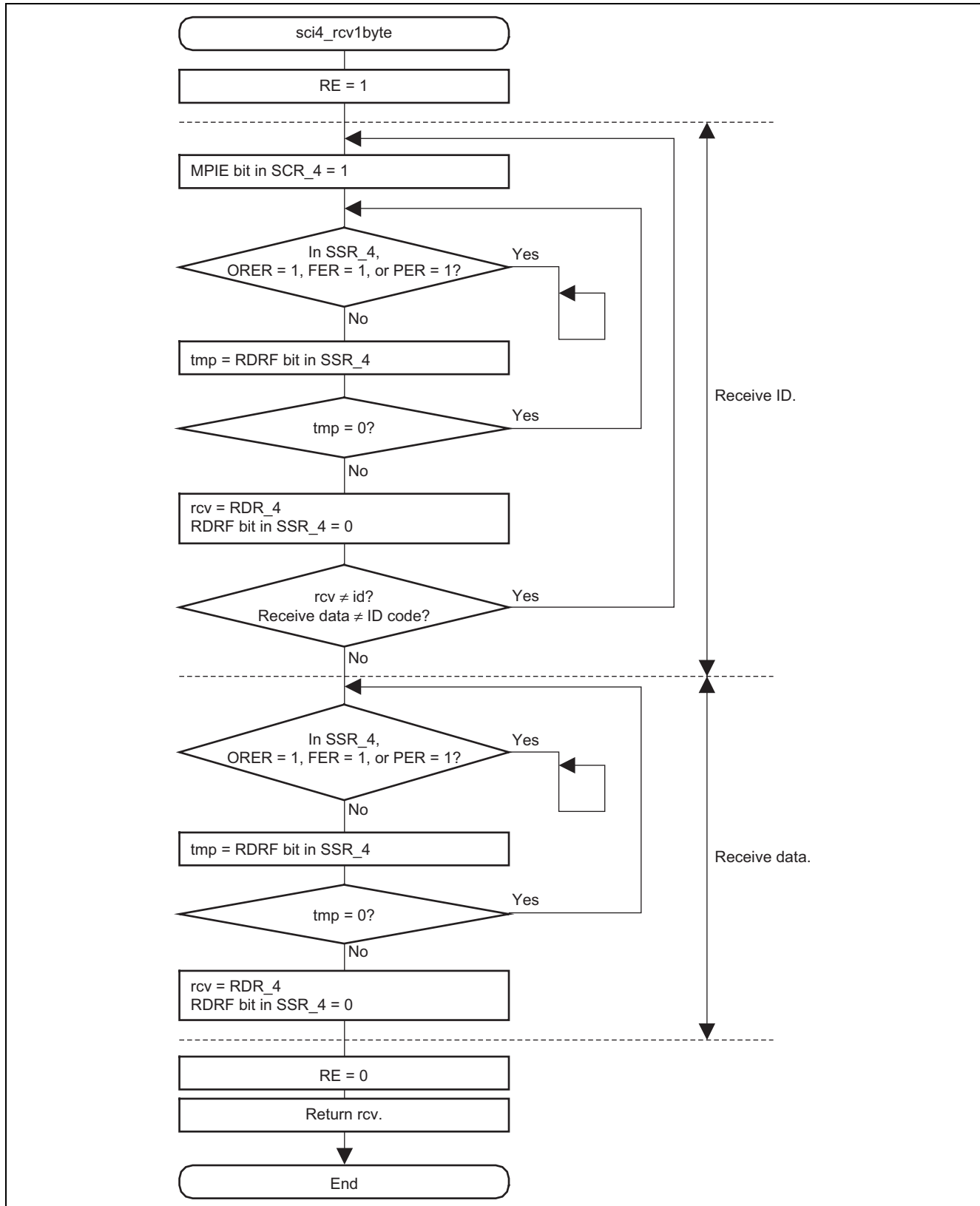
Bit	Bit Name	Setting	R/W	Function
6	RDRF	0	R/(W)*	<p>Receive Data Register Full</p> <p>Indicates whether RDR contains receive data.</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> When reception is finished successfully, and receive data is transferred from RSR to RDR <p>[Clearing conditions]</p> <ul style="list-style-type: none"> When 0 is written to RDRF after reading RDRF = 1 When the DMAC or DTC transfers data from RDR due to an RXI interrupt <p>Even if the RE bit in SCR is cleared to 0, the RDRF flag is unaffected and its previous state retained.</p> <p>If reception of the next data is completed while the RDRF flag is still set to 1, an overrun error occurs and the received data is lost.</p>
5	ORER	0	R/(W)*	<p>Overrun Error</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> When an overrun error occurs during reception <p>[Clearing condition]</p> <ul style="list-style-type: none"> When 0 is written to ORER after reading ORER = 1
4	FER	0	R/(W)*	<p>Framing Error</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> When a framing error occurs during reception <p>[Clearing condition]</p> <ul style="list-style-type: none"> When 0 is written to FER after reading FER = 1
3	PER	0	R/(W)*	<p>Parity Error</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> When a parity error occurs during reception <p>[Clearing condition]</p> <ul style="list-style-type: none"> When 0 is written to PER after reading PER = 1

Note: * Only 0 can be written to clear the flag.

- Receive data register_4 (RDR_4)
Function: 8-bit register that stores receive data
Setting: Undefined

Address: H'FFFE95

(5) Flowchart



5.6.4 sci4_trsr1byte Function

(1) Functional overview

Transmits the ID code and 1-byte data.

(2) Arguments

Type	Variable Name	Description
unsigned char	id	ID code
unsigned char	tdt	Transmit data

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. The setting values shown below are the values used in this sample task and differ from their initial values.

- Serial control register_4 (SCR_4) Address: H'FFFE92

Bit	Bit Name	Setting	R/W	Function
5	TE	0	R/W	Transmit Enable 0: Transmission is disabled 1: Transmission is enabled

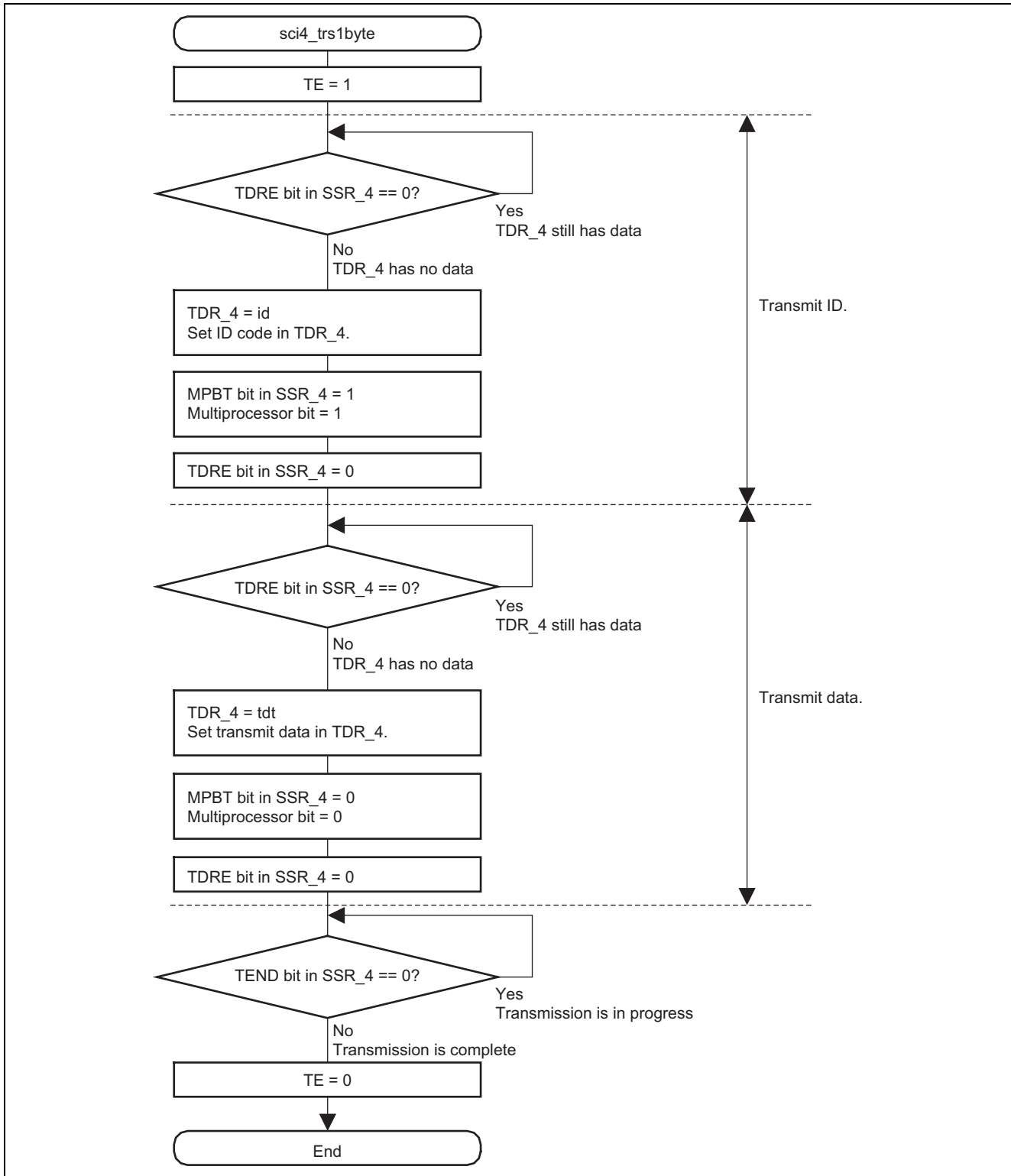
- Transmit data register_4 (TDR_4) Address: H'FFFE93
Function: 8-bit register that stores transmit data
Setting: Undefined

- Serial status register_4 (SSR_4) Address: H'FFFE94

Bit	Bit Name	Setting	R/W	Function
7	TDRE	0	R/(W)*	Transmit Data Register Empty 0: Indicates that the transmit data written to TDR has not been transferred to TSR 1: Indicates that transmit data has not been written to TDR or the transmit data written to TDR has been transferred to TSR
2	TEND	Undefined	R/(W)*	Transmit End 0: Transmission is in progress 1: Transmission has ended
0	MPBT	0/1	R/W	Multiprocessor Bit Transfer Sets the multiprocessor bit value that is to be added to the transmit frame.

Note: * Only 0 can be written to clear the flag.

(5) Flowchart



Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.10.06	—	First edition issued

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