To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

H8SX Family

Measuring High and Low Pulse Widths

Introduction

The 16-bit timer pulse unit (TPU) is used to measure the high and low pulse periods and the measured results are stored in RAM.

Target Device

H8SX/1582F

Contents

1. Specifications

- The timing of the pulse width measurement is as shown in figure 1.
- The high and low level periods of the pulse signal are measured and stored in RAM.
- At Pϕ = 20 MHz, the high and low pulse widths can be measured within the range from 50 ns to 3.27 ms with 50-ns resolution.

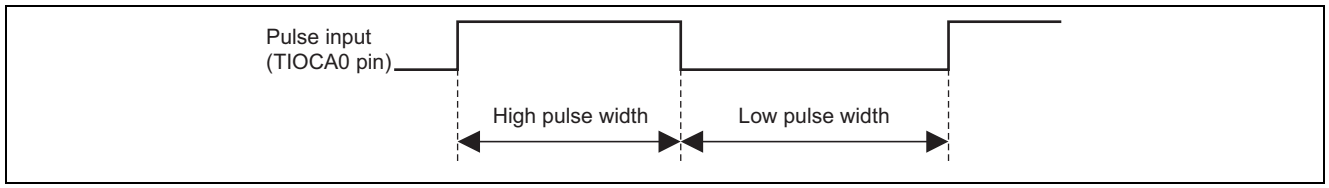


Figure 1 Timing of Pulse Width Measurement

2. Conditions for Application

Table 1 Conditions for Application

Item	Contents	
Operating frequency	Input clock:	5 MHz
	System clock (Iϕ):	40 MHz
	Peripheral module clock (Pϕ):	20 MHz
	External bus clock (Bϕ):	20 MHz
Operating mode	Mode 3 (MD1 = 1, MD0 = 1)	
Development tool	High-performance Embedded Workshop Version 4.00.02	
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler Version 6.01.00 (from Renesas Technology Corp.)	
Compile option	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3, -speed = (register, shift, struct, expression)	

Table 2 Section Settings

Address	Section Name	Description
H'001000	P	Program area
H'FF9000	B	RAM area

3. Description of Modules Used

In this sample task, the 16-bit timer pulse unit (TPU) is used to measure the high and low pulse widths. Figure 2 shows a block diagram of channel 0 of the TPU (TPU_0). This sample task uses the following features of the TPU.

— The input capture function, which detects the rising and falling edges of the pulse and places the timer value at that time in the internal register.
— Counter clearing upon input capture
— Calling an interrupt service routine upon detection of a rising or falling edge of the pulse.

The TPU registers are described below.

- Timer start register (TSTR)
  TSTR starts or stops the TCNT counters on channels 0 to 5 individually. TCNT must be stopped before setting the operating mode in the TMDR register or setting the clock source for TCNT in the TCR register.

- Timer control register_0 (TCR_0)
  TCR controls TCNT on each channel. The TPU has one TCR for each channel; i.e., a total of six TCR registers. TCR must be set while the corresponding TCNT is stopped.

- Timer I/O control register H_0 (TIORH_0)
  TIOR controls the TGR registers. The TPU has two TIOR registers each for channels 0 and 3, and one each for channels 1, 2, 4, and 5, for a total of eight TIOR registers. Note that TIOR is affected by the setting of TMDR. The initial output specified by TIOR takes effect while the counter is stopped (the corresponding CST bit in TSTR is clear).

- Timer interrupt enable register_0 (TIER_0)
  TIER enables/disables interrupt requests on each channel. The TPU has one TIER for each channel; i.e., a total of six TIER registers.

- Timer counter_0 (TCNT_0)
  TCNT is a 16-bit readable/writable counter. One TCNT is provided for each channel, which makes a total of six TCNT counters. TCNT is initialized to H'0000 when the chip is reset or enters hardware standby mode. Access to TCNT in 8-bit units is not allowed; always access in 16-bit units.

- Timer general register A_0 (TGRA_0)
  TGR is a 16-bit readable/writable register that can be used as either an output compare or input capture register. The TPU has four TGR registers each for channels 0 and 3, and two each for channels 1, 2, 4, and 5, for a total of 16 TGR registers. Access to TGR in 8-bit units is not allowed; always access in 16-bit units.

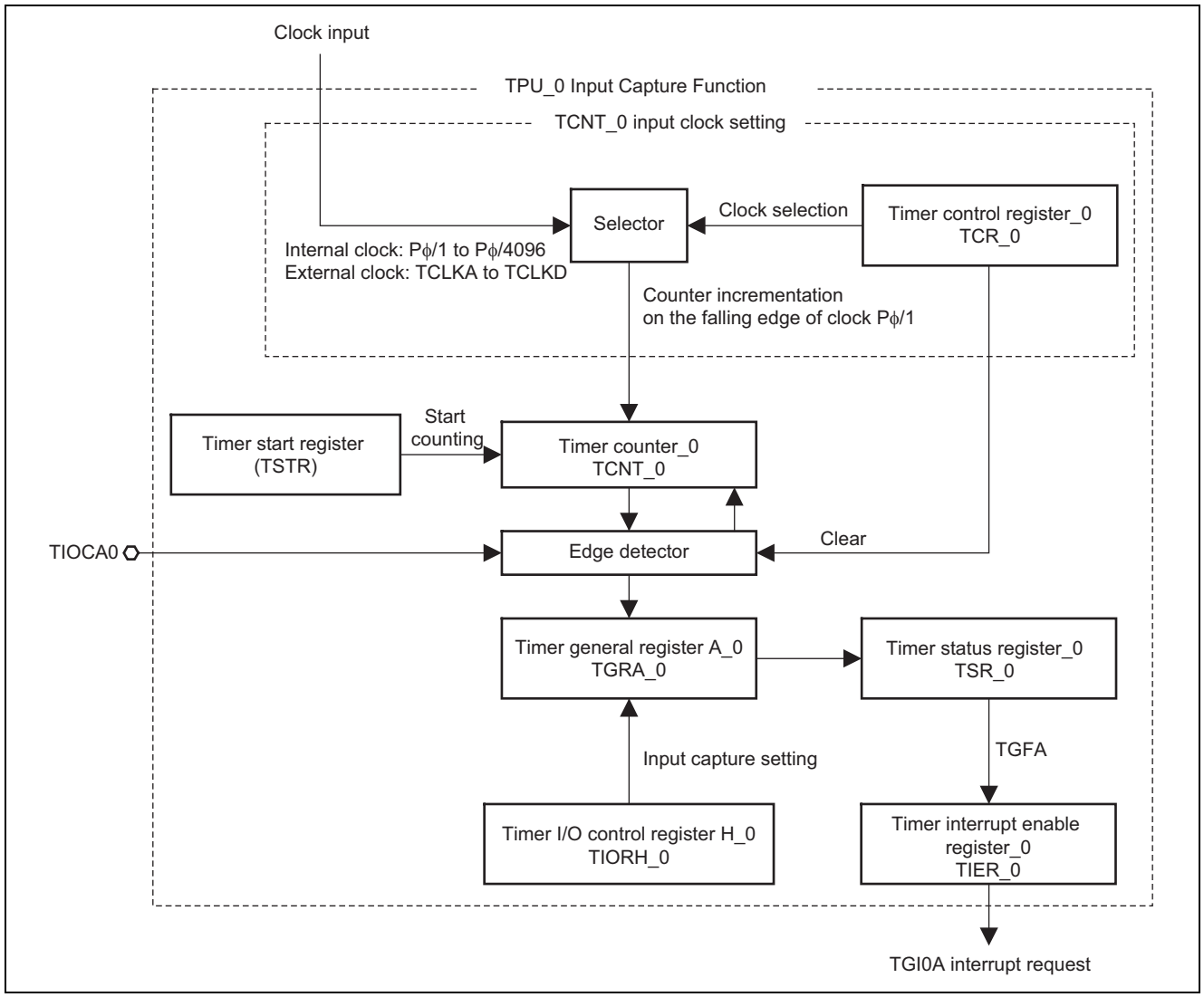


Figure 2 Block Diagram of TPU Channel 0 (TPU_0)

4. Description of Operation

Figure 3 illustrates the principles of operation of high and low pulse width measurement. The hardware processing and software processing of figure 3 are explained in table 3.

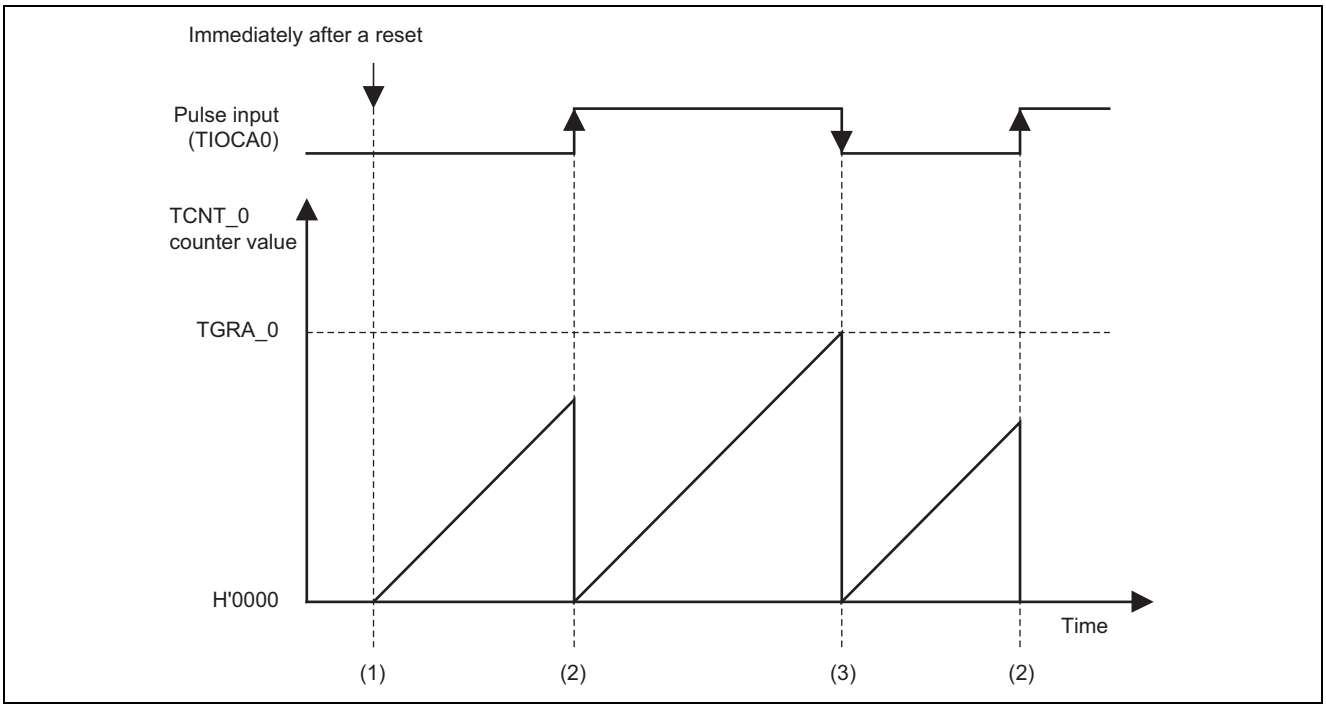


Figure 3 Operation Principles of High and Low Pulse Width Measurement

Table 3 Hardware and Software Processing

	Hardware Processing	Software Processing
(1)	No processing	Initial settings (a) Set so that TCNT_0 counts the falling edges of clock Pϕ/1. (b) Set so that TCNT_0 is cleared upon input capture of TGRA. (c) Set so that input capture takes place on the rising edge of the TIOCA0 pin. (d) Enable TGI0A interrupt generation by bit TGFA. (e) Start counting by TPU_0.
(2)	(a) Generate a TGI0A interrupt. (b) Transfer the value in TCNT_0 to TGRA_0.	TGI0A interrupt handling (a) Clear TGFA. (b) Store the value in TGRA_0 to RAM (pwh_ldata). (c) Set so that input capture takes place on the falling edge of the TIOCA0 pin.
(3)	(a) Generate a TGI0A interrupt. (b) Transfer the value in TCNT_0 to TGRA_0.	TGI0A interrupt handling (a) Clear TGFA. (b) Store the value in TGRA_0 to RAM (pwh_hdata). (c) Set so that input capture takes place on the rising edge of the TIOCA0 pin.

5. Description of Software

5.1 List of Functions

Table 4 List of Functions

Function Name	Functions
main	Main routine Specifies clearing of TCNT_0 by input capture and enables the TGI0A interrupt.
tgi0a_int	TGI0A interrupt handling routine Reads TGRA_0 and stores the value in RAM as the measurement of high or low pulse width.

5.2 Vector Table

Table 5 Exception Handling Vector Table

Exception Handling Source	Vector Number	Vector Table Address	Exception Handling Routine
Reset	0	H'000000	init
TPU_0 TGI0A	88	H'000160	tgi0a_int

5.3 RAM Usage

Table 6 RAM Usage

Type	Variable Name	Description	Used In
unsigned char	pwh_hdata	Transfer counter for PPG group 0 output	main, tgi0a_int
unsigned char	pwh_ldata	Transfer counter for PPG group 1 output	main, tgi1a_int

5.4 Formula for Pulse Width Calculation

The following formula is used to calculate the high and low pulse widths.

High or low pulse width = (timer value + 1) × period of Pϕ

5.5 Description of Functions

5.5.1 main Function

(1) Functional Overview

Main routine that specifies clearing of TCNT_0 by input capture and enables the TGI0A interrupt.

(2) Arguments

None

(3) Return value

None

(4) Internal Registers

The internal registers used in this sample task are described below. The setting values shown in these tables are the values used in this sample task and differ from their initial values.

- Port 3 Input Buffer Control Register (P3ICR) Address: H'FFFB92

Bit	Bit Name	Setting	R/W	Function
0	P30ICR	1	R/W	0: Disables the input buffer of pin P30. The input signal is tied high. 1: Enables the input buffer of pin P30. The pin state is reflected on the peripheral module.

- System Clock Control Register (SCKCR) Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Function
10	ICK2	0	R/W	System clock (Iϕ) select
9	ICK1	0	R/W	These bits select the system clock frequency. The CPU, DMAC, and DTC modules are driven by the system clock. 000: Input clock × 8
8	ICK0	0	R/W	
6	PCK2	0	R/W	Peripheral clock (Pϕ) select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module clock.
4	PCK0	1	R/W	001: Input clock × 4
2	BCK2	0	R/W	External bus clock (Bϕ) select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	1	R/W	001: Input clock × 4

- MSTPCRA, MSTPCRB, and MSTPCRC are the registers that control module stop mode. Setting the bits in these registers places the corresponding modules in module stop mode, and clearing the bits cancels module stop mode.

- Module Stop Control Register A (MSTPCRA) Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Function
15	ACSE	0	R/W	All-module-clock-stop mode enable Enables or disables transition to all-module-clock-stop mode. If this bit is set to 1, all-module-clock-stop mode is entered when the SLEEP instruction is executed by the CPU while all the modules under control of the MSTPCR registers are placed in module stop mode. In all-module-clock-stop mode, even the bus controller and I/O ports are stopped to reduce the supply current. 0: Disables transition to all-module-clock-stop mode. 1: Enables transition to all-module-clock-stop mode.
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
4	MSTPA4	1	R/W	A/D converter (unit 1)
3	MSTPA3	1	R/W	A/D converter (unit 0)
1	MSTPA1	1	R/W	16-bit timer pulse unit (TPU channels 11 to 6)
0	MSTPA0	0	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

- Module Stop Control Register B (MSTPCRB) Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Function
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communication interface_4 (SCI_4)
11	MSTPB11	1	R/W	Serial communication interface_3 (SCI_3)

- Module Stop Control Register A (MSTPCRC) Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Function
10	MSTPC10	1	R/W	Synchronous serial communication unit 2 (SSU_2)
9	MSTPC9	1	R/W	Synchronous serial communication unit 1 (SSU_1)
8	MSTPC8	1	R/W	Synchronous serial communication unit 0 (SSU_0)
1	MSTPC1	0	R/W	On-chip RAM (H'FFF9000 to H'FFFBFFF)
0	MSTPC0	0		The values written to MSTPC1 and MSTPC0 should always be the same.

- Timer Start Register (TSTR) Address: H'FFFFBC

Bit	Bit Name	Setting	R/W	Function
5	CST5	0	R/W	Counter start 5 to 0
4	CST4	0	R/W	Each of these bits starts or stops operation of the corresponding TCNT counter of the TPU.
3	CST3	0	R/W	
2	CST2	0	R/W	If 0 is written to the CST bit while the TCNT is counting with the TIOC pin designated for output, the counter stops but the output-compare output level on the TIOC pin is retained. If a value is written to TIOR when the CST bit is clear, the output level on the pin will be changed to the set initial output value.
1	CST1	0	R/W	
0	CST0	1	R/W	0: Stops counting by TCNT_5 to TCNT_0. 1: Starts counting by TCNT_5 to TCNT_0.

- Timer Control Register_0 (TCR_0) Address: H'FFFFC0

Bit	Bit Name	Setting	R/W	Function
7	CCLR2	0	R/W	Counter clear 2 to 0
6	CCLR1	0	R/W	These bits select the counter clearing source
5	CCLR0	1	R/W	001: Clear TCNT_0 on compare match or input capture by TGRA.
4	CKEG1	0	R/W	Clock edge 1, 0
3	CKEG0	0	R/W	These bits select the edge of the input clock. 00: TCNT_0 counts falling edges.
2	TPSC2	0	R/W	Timer prescaler 2 to 0
1	TPSC1	0	R/W	These bits select the counter clock for TCNT_0.
0	TPSC0	0	R/W	000: TCNT_0 is driven by Pϕ/1.

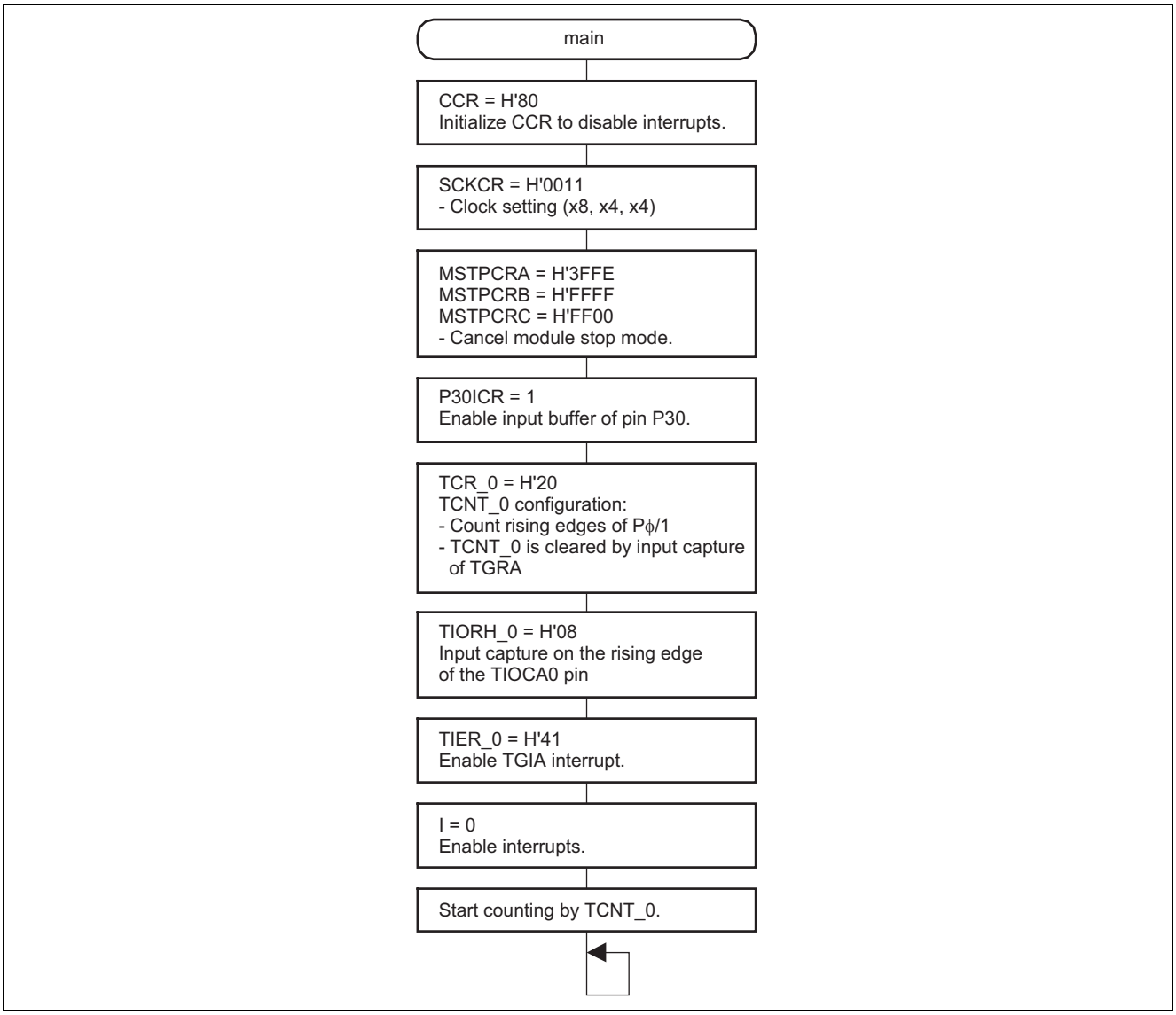
- Timer I/O Control Register H_0 (TIORH_0) Address: H'FFFFC2

Bit	Bit Name	Setting	R/W	Function
3	IOA3	1	R/W	I/O control A3 to A0
2	IOA2	0	R/W	These bits set the function of TGRA_0.
1	IOA1	0	R/W	1000: TGRA_0 operates as an input capture register. Input capture takes place on the rising edge of the TIOCA0 pin.
0	IOA0	0	R/W	

- Timer Interrupt Enable Register_0 (TIER_0) Address: H'FFFFC4

Bit	Bit Name	Setting	R/W	Function
0	TGIEA	1	R/W	TGR interrupt enable A Enables or disables interrupt request (TGIA) generation when the TGFA bit in TSR is set to 1. 0: Disables interrupt request (TGIA) generation by TGFA. 1: Enables interrupt request (TGIA) generation by TGFA.

(5) Flowchart


main
CCR = H'80
Initialize CCR to disable interrupts.
SCKCR = H'0011
- Clock setting (x8, x4, x4)
MSTPCRA = H'3FFE
MSTPCRB = H'FFFF
MSTPCRC = H'FF00
- Cancel module stop mode.
P30ICR = 1
Enable input buffer of pin P30.
TCR_0 = H'20
TCNT_0 configuration:
- Count rising edges of Pϕ/1
- TCNT_0 is cleared by input capture of TGRA
TIORH_0 = H'08
Input capture on the rising edge of the TIOCA0 pin
TIER_0 = H'41
Enable TGIA interrupt.
I = 0
Enable interrupts.
Start counting by TCNT_0.

5.5.2 tgi0a_int Function

(1) Functional Overview

TGI0A interrupt handling routine that reads TGRA_0 and stores the value in RAM as the measurement of the high or low pulse width.

(2) Arguments

None

(3) Return value

None

(4) Internal Registers

The internal registers used in this sample task are described below. The setting values shown in these tables are the values used in this sample task and differ from their initial values.

- Timer I/O Control Register H_0 (TIORH_0) Address: H'FFFFC2

Bit	Bit Name	Setting	R/W	Function
3	IOA3	B'1001	R/W	I/O control A3 to A0
2	IOA2	or	R/W	These bits set the function of TGRA_0.
1	IOA1	B'1000	R/W	1000: TGRA_0 operates as an input capture register. Input capture takes place on the rising edge of the TIOCA0 pin.
0	IOA0		R/W	1001: TGRA_0 operates as an input capture register. Input capture takes place on the falling edge of the TIOCA0 pin.

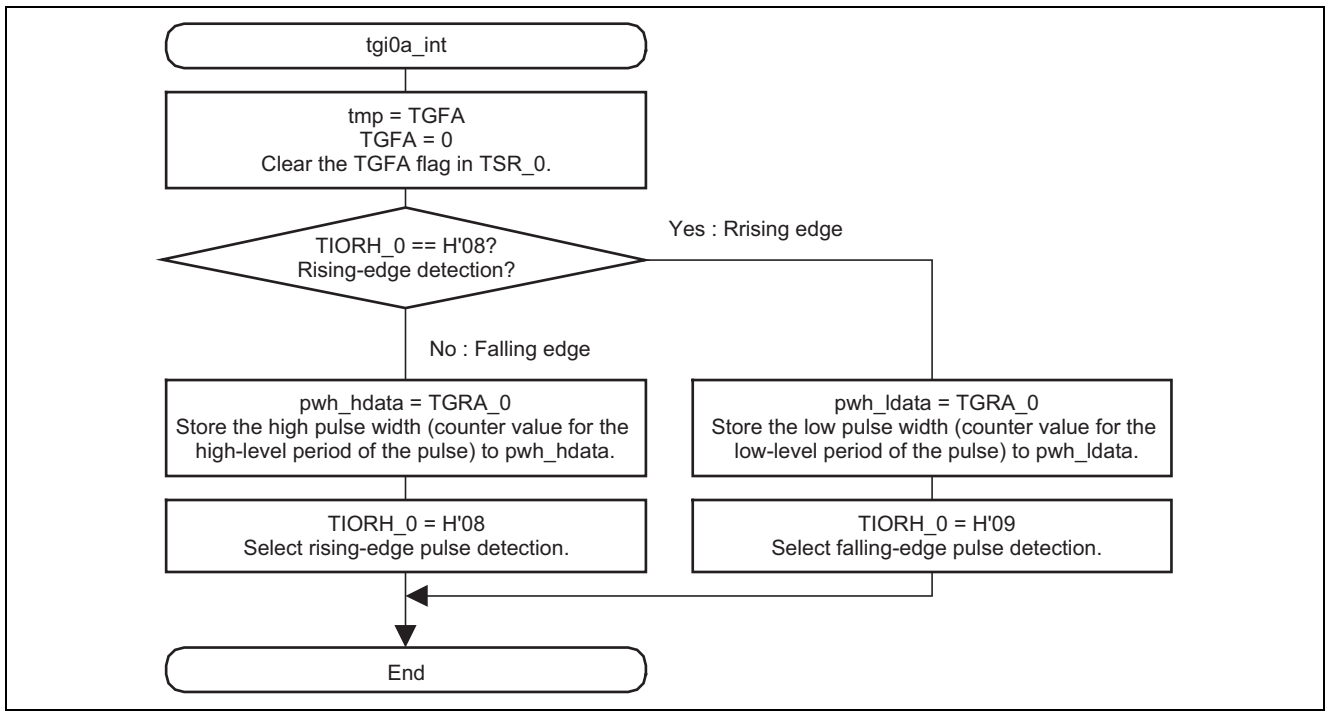
- Timer Status Register_0 (TSR_0) Address: H'FFFFC5

Bit	Bit Name	Setting	R/W	Function
0	TGFA	0	R/(W)*	Input capture/output compare flag A Status flag that indicates the occurrence of TGRA input capture or compare match. [Setting conditions] • When TCNT = TGRA while TGRA is functioning as an output compare register • When the TCNT value is transferred to TGRA by the input capture signal while TGRA is functioning as an input capture register [Clearing conditions] • When DMAC is activated by a TGIA interrupt while the DTA bit in DMDR of DMAC is 1 • When 0 is written to TGFA after TGFA = 1 is read

Note: * Only 0 can be written to clear the flag.

- Timer General Register A_0 (TGRA_0) Address: H'FFFFC8
  Function: Used as an input capture register.
  Setting: Undefined

(5) Flowchart


tgi0a_int
tmp = TGFA
TGFA = 0
Clear the TGFA flag in TSR_0.
TIORH_0 == H'08?
Rising-edge detection?
Yes : Rrising edge
No : Falling edge
pwh_hdata = TGRA_0
Store the high pulse width (counter value for the high-level period of the pulse) to pwh_hdata.
pwh_ldata = TGRA_0
Store the low pulse width (counter value for the low-level period of the pulse) to pwh_ldata.
TIORH_0 = H'08
Select rising-edge pulse detection.
TIORH_0 = H'09
Select falling-edge pulse detection.
End

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Mar.10.06	—	First edition issued

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
   The information described here may contain technical inaccuracies or typographical errors.
   Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
   Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (http://www.renesas.com).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
   Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.