M16C/5LD, M16C/56D, M16C/5L, M16C/56, M16C/6C Group

How to Use Timer S Associated Interrupts

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1. Abstract

This application note introduces how to use timer S associated interrupts in the M16C/5LD, M16C/56D, M16C/5L, M16C/56, and M16C/6C Groups.

2. Introduction

The application example described in this document applies to the following microcomputers (MCUs):

- MCUs: M16C/5LD Group
  M16C/56D Group
  M16C/5L Group
  M16C/56 Group
  M16C/6C Group

The application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above groups. Check the user's manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Outline

Timer S has an input capture/output compare function (IC/OC). The interrupts have multiple request sources. Figure 3.1 shows the block diagram of the IC/OC interrupts, and Table 3.1 lists the Interrupt Assignments.

When a base timer reset request by the RST4 bit or a base timer overflow request is generated, the IR bit in the interrupt control register corresponding to the IC/OC base timer interrupt (bit 3 in the BTIC register) becomes 1 (interrupt requested).
When an interrupt is generated for channel j, the G1IRj bit in the G1IR register becomes 1 (interrupt requested) (j = 0 to 7). When the G1IE0j bit in the G1IE0 register is 1 (IC/OC interrupt 0 request enabled), the IR bit corresponding to IC/OC interrupt 0 (bit 3 in the ICOC0IC register) becomes 1 (interrupt requested). When the G1IE1j bit in the G1IE1 register is 1 (IC/OC interrupt 1 request enabled), the IR bit corresponding to IC/OC interrupt 1 (bit 3 in the ICOC1IC register) becomes 1 (interrupt requested).
The G1IRj bit in the G1IR register does not automatically become 0 when an interrupt is received. Write 0 by a program to set it to 0. If any of the bits in the G1IR register is left as 1, the subsequent IC/OC interrupt 0 request source or IC/OC interrupt 1 request source generated will be ignored.
When an IC/OC channel k interrupt request is generated, the IR bit corresponding to the IC/OC channel k interrupt (bit 3 in registers ICOCH0IC to ICOCH3IC) becomes 1 (interrupt requested) (k = 0 to 3).

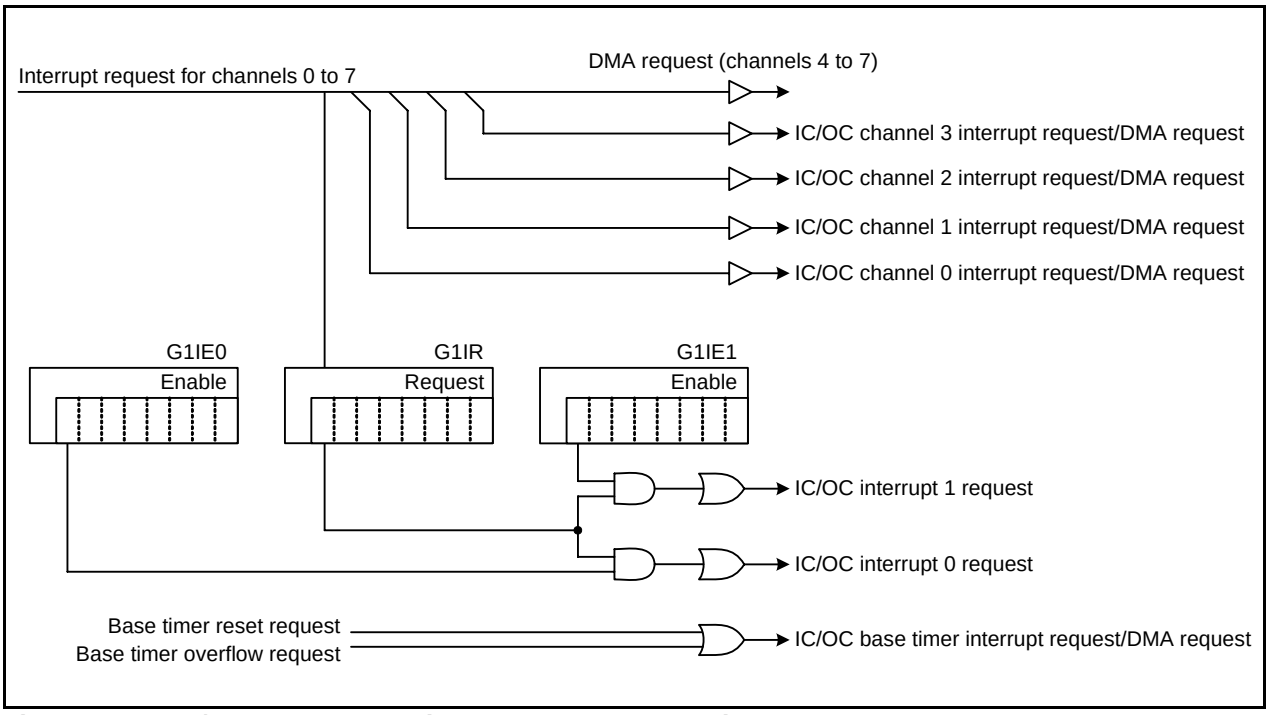


Figure 3.1 IC/OC Interrupts and DMA Request Generation

Table 3.1 Interrupt Assignments

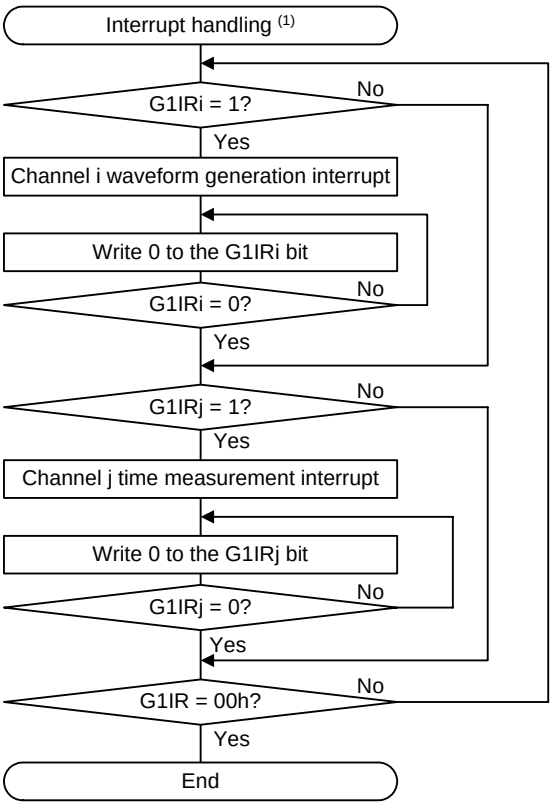
Interrupt	Interrupt Control Register
IC/OC base timer interrupt	BTIC (007Fh)
IC/OC interrupt 0	ICOC0IC (0079h)
IC/OC interrupt 1	ICOC1IC (007Bh)
IC/OC channel 0 interrupt	ICOCH0IC (007Ah)
IC/OC channel 1 interrupt	ICOCH1IC (007Ch)
IC/OC channel 2 interrupt	ICOCH2IC (007Dh)
IC/OC channel 3 interrupt	ICOCH3IC (007Eh)

4. Notes on Timer S

4.1 Changing the G1IR Register

The G1IRi bit in the G1IR register does not automatically become 0 (interrupt not requested) even when the requested interrupt is acknowledged (i = 0 to 7). Set the G1IRi bit to 0 by a program after an interrupt request is acknowledged.
The IC/OC interrupt 0/1 is generated when the G1IRi bit changes from 0 to 1 (interrupt requested).
When the G1IE0i bit in the G1IE0 register or G1IE1i bit in the G1IE1 register is 0 (IC/OC interrupt 0/1 request disabled), IC/OC interrupt 0/1 is not generated even if the G1IRi bit changes from 0 to 1.
Set the G1IRi bit in the G1IR register to 0 to acknowledge IC/OC interrupt 0/1 again.
When any bit in the G1IR register is left as 1 (the G1IR register is a value other than 00h) and the corresponding bit in the G1IE0 or G1IE1 register is 1, the subsequent IC/OC interrupt 0/1 is not generated.
To set the G1IR register to 00h by individually setting each bit to 0, use the AND or BCLR instruction.

Figure 4.1 shows the IC/OC Interrupt 0/1 Operation.



i = 0 to 7
j = 0 to 7
G1IRi, G1IRj: Bits in the G1IR register

Note:
1. This is an example of using the channel i waveform generation interrupt and channel j time measurement interrupt.

Figure 4.1 IC/OC Interrupt 0/1 Operation

4.2 Changing Registers ICOCiIC and ICOCHjIC (i = 0, 1; j = 0 to 7)

When changing registers ICOCiIC and ICOCHjIC, if an interrupt request is generated for a corresponding register while executing an instruction, the IR bit may not become 1 (interrupt requested) and the interrupt request may be ignored. In this case, if the G1IRj bit in the G1IR register remains 1, a new IC/OC interrupt will not be generated. Use the AND, OR, BCLR, or BSET instruction to rewrite registers ICOCiIC and ICOCHjIC.

When timer S is initialized, use the AND, OR, BCLR, or BSET instruction to rewrite registers ICOCiIC and ICOCHjIC after setting registers ICOCiIC, ICOCHjIC, and G1IR to 00h.

5. Application Example

5.1 Explanation of the Sample Program

The following shows an example of the PWM output from pins OUTC1_0 (P2_0) and OUTC1_4 (P2_4) when single-phase waveform output mode is used. Also, the measured value is stored to RAM when a rising edge is input to the INPC1_6 (P2_6) pin using time measurement mode.
Table 5.1 lists the Functions and Interrupt Assignments at Each Channel.

Table 5.1 Functions and Interrupt Assignments at Each Channel

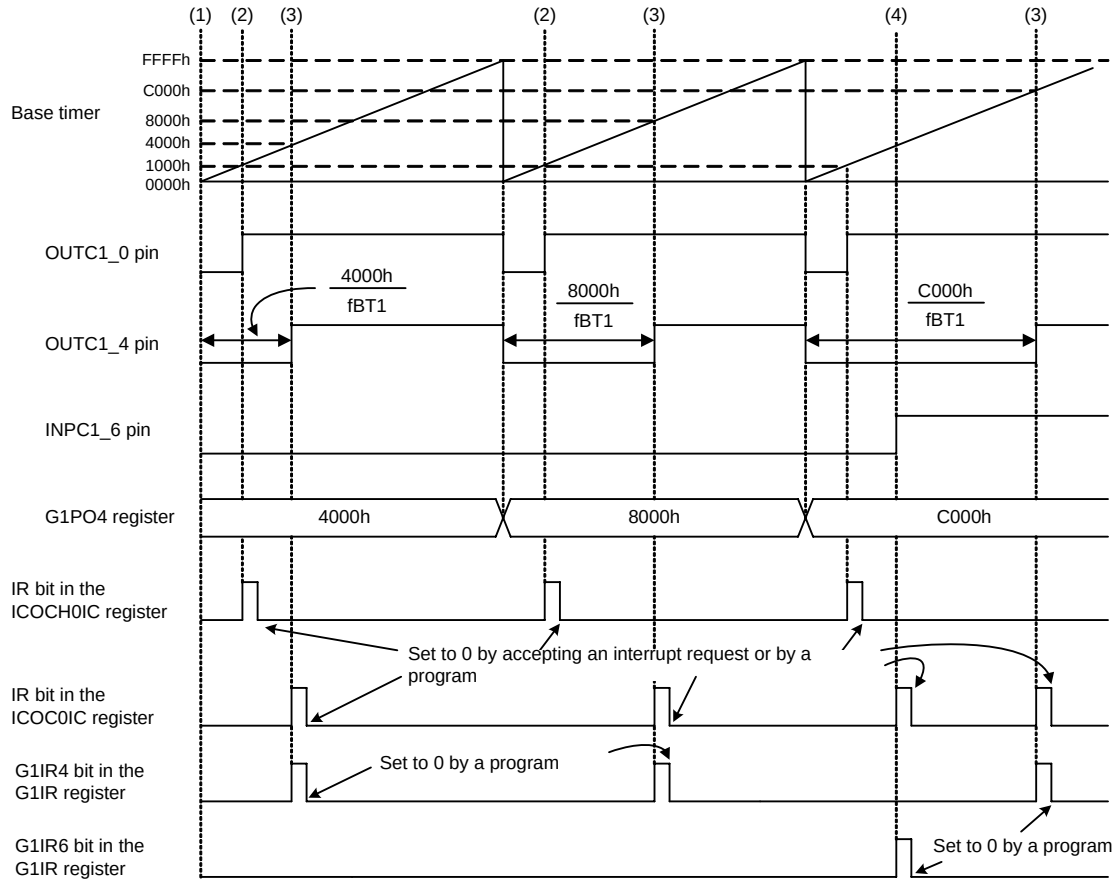
Channel	Function	Interrupt
Channel 0	Waveform generation function (single-phase output mode)	IC/OC channel 0 interrupt
Channel 4	Waveform generation function (single-phase output mode)	IC/OC interrupt 0
Channel 6	Time measurement function	IC/OC interrupt 0

The clock conditions are as follows:

- Main clock: 20 MHz
- Base timer operation clock (fBT1): 1 MHz

Figure 5.1 shows the Sample Program Operation.

(1) After performing the initial setting, the BTS bit in the G1BCR1 register is set to 1 (base timer count starts).
(2) When the base timer and G1PO0 register values match, high level is output from the OUTC1_0 pin.
Channel 0 interrupt confirming port (P10_0) is inverted in IC/OC channel 0 interrupt processing.
(3) When the base timer and G1PO4 register values match, high level is output from the OUTC1_4 pin.
Channel 4 waveform generation interrupt processing is chosen and the G1PO4 register value is set to modify low level output width from the OUTC1_4 pin in IC/OC interrupt processing.
Channel 4 interrupt confirming port is inverted, and the G1IR4 bit in the G1IR register is written to 0.
(4) Channel 6 time measurement interrupt process is chosen and the C1TM6 register value is stored to RAM in IC/OC interrupt processing at the rising edge is input to the INPC1_6 pin.
Channel 6 interrupt confirming port (P10_6) is inverted, and the G1IR6 bit in the G1IR register is written to 0.

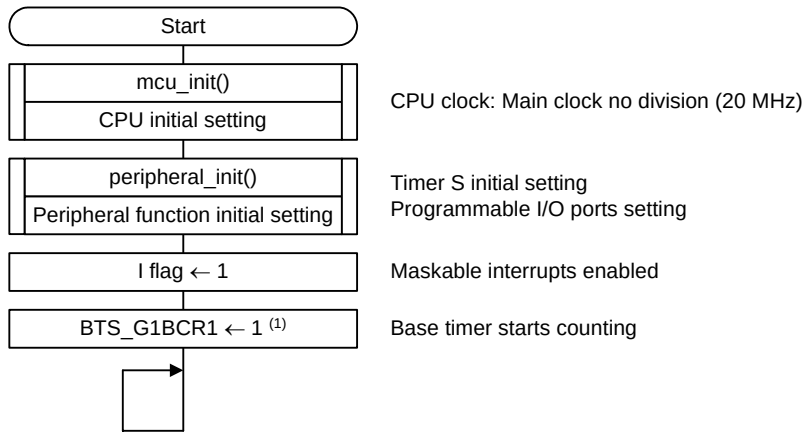


The above assumes the following:
- The RST4 bit in the G1BCR0 register is 0 (the base timer is not reset when the base timer and G1BTRR register values match).
- The RST2 bit in the G1BCR1 register is 0 (the base timer is not reset when low is input to the $\overline{\text{INT1}}$ pin), and the RST1 bit is 0 (the base timer is not reset when the base timer and G1PO0 register values match).
- The IVL bit in registers G1POCR0 and G1POCR4 is 0 (output low as default value), the INV bit is 0 (output level not inverted), the RLD bit in the G1POCR0 register is 0 (reload the G1PO0 register on a write access), and the RLD bit in the G1POCR4 register is 1 (reload the G1PO4 register when the base timer is reset).
- Bits CTS1 to CTS0 in the G1TMCR6 register are 01b (rising edge), bits DF1 to DF0 are 00b (no digital filter), the GT bit is 0 (gate function not used), and the PR bit is 0 (prescaler not used).
- Bits EOC0 and EOC4 in the G1OER register are 0 (output enabled), and the EOC6 bit is 1 (output disabled).

Figure 5.1 Sample Program Operation

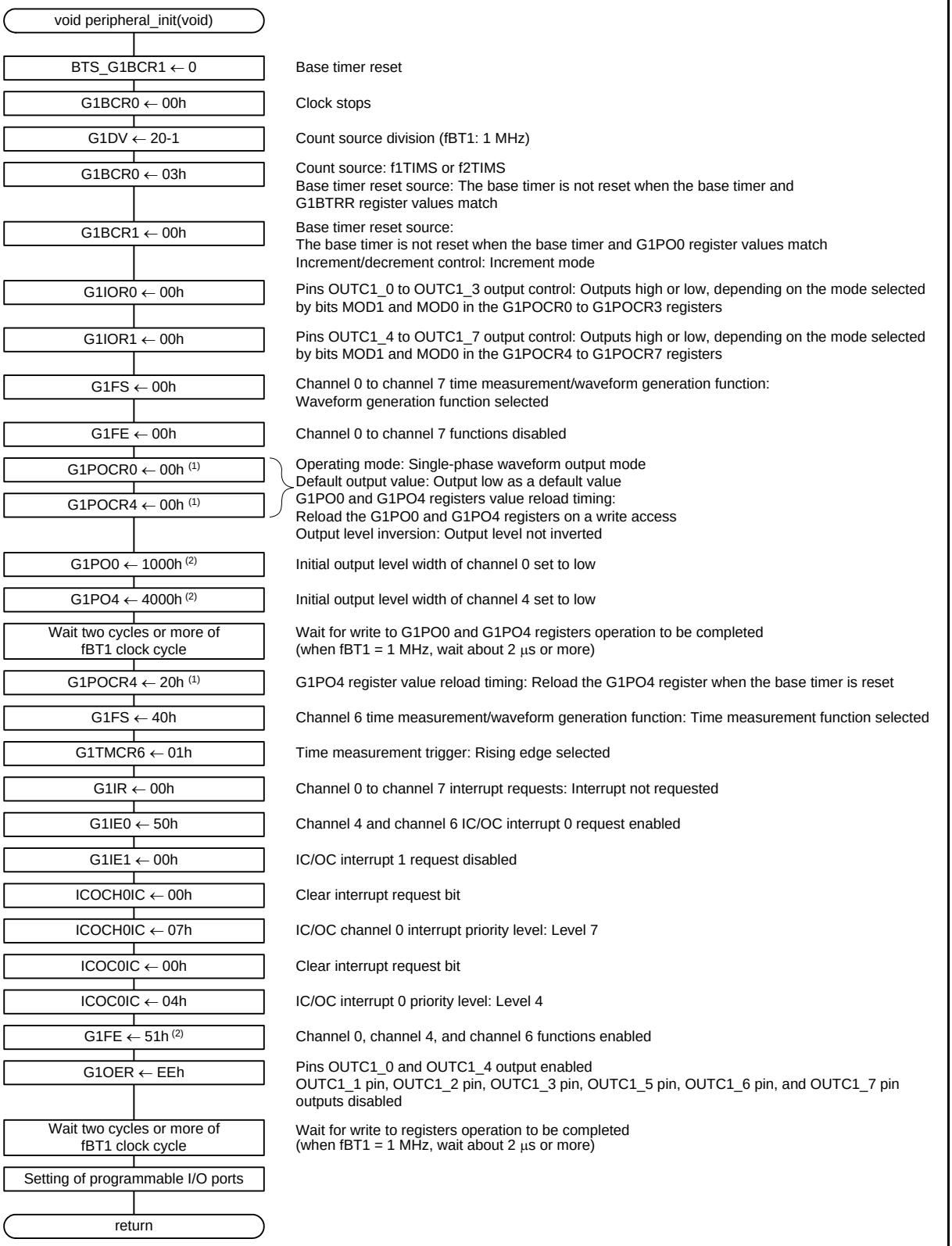
5.2 Settings

5.2.1 Main Function



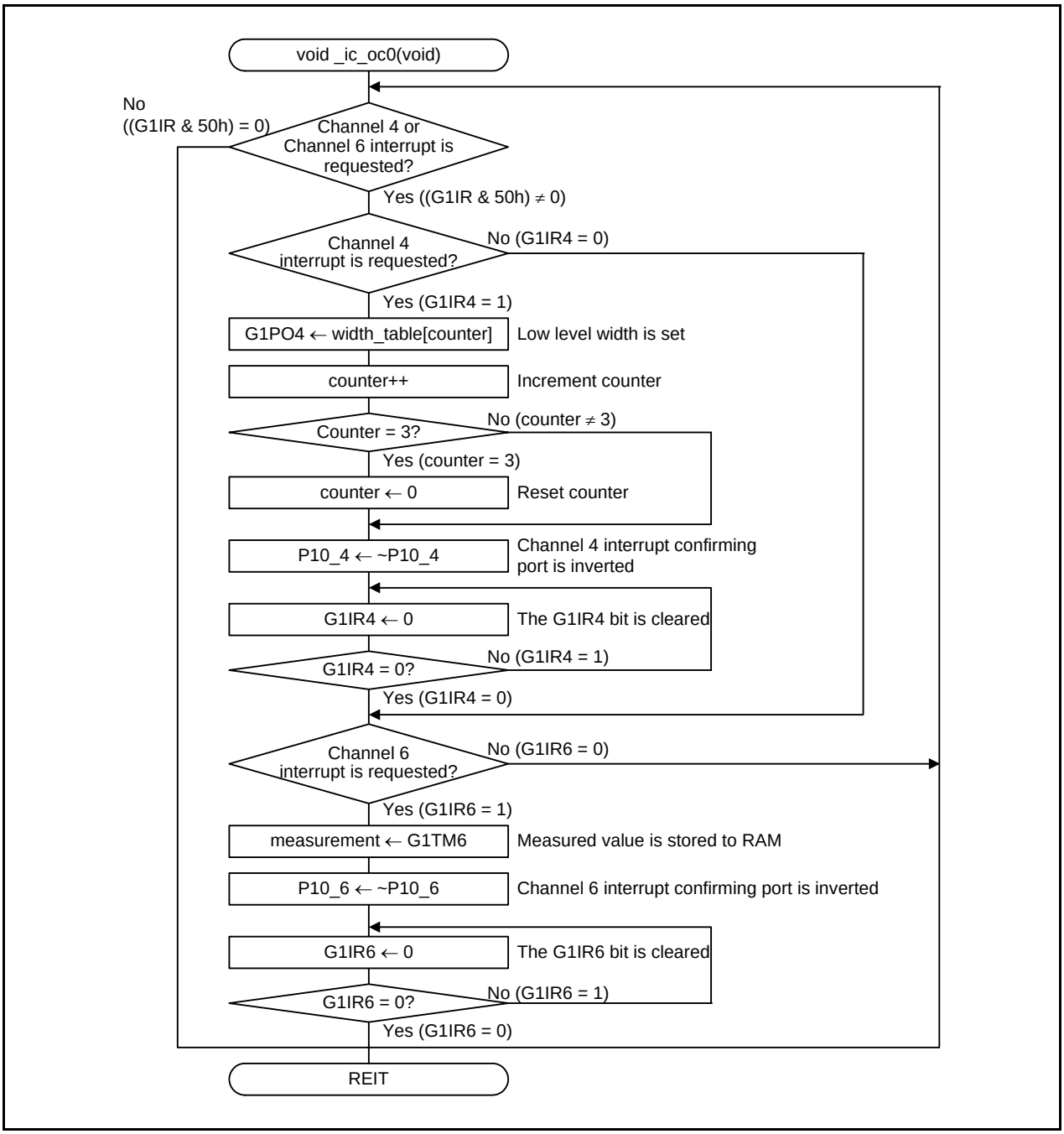
Note:
1. When registers G1POCR0 to G1POCR7 are changed, set the BTS bit to 1 after one or more fBT1 clock cycles.

5.2.2 Peripheral Function Initial Setting

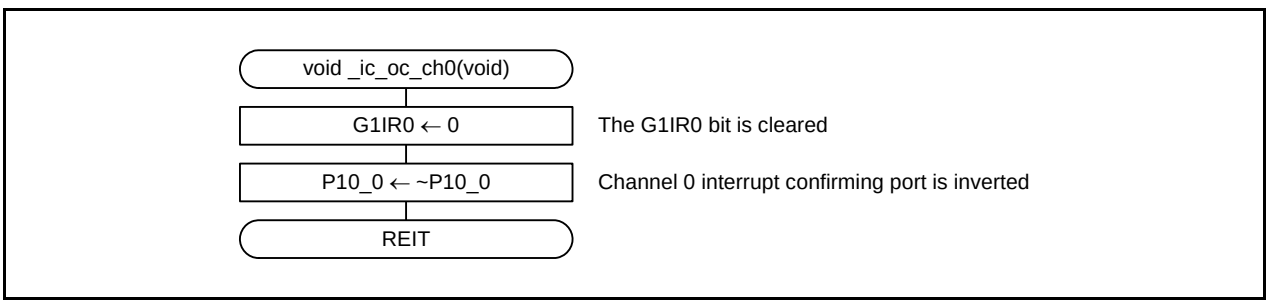


Notes:
1. When the register is changed, set the BTS bit to 1 after one or more fBT1 clock cycles.
2. The values written to the registers are reflected when the clock is synchronized with the base timer count source (fBT1).

5.2.3 IC/OC Interrupt 0 Function



5.2.4 IC/OC Channel 0 Interrupt Function



6. Sample Program

A sample program can be downloaded from the Renesas Electronics website.
To download, click “Application Notes” in the left-hand side menu of the M16C Family page.

7. Reference Documents

M16C/5LD, 56D Group User’s Manual: Hardware Rev.1.10
M16C/5L, M16C/56 Group User’s Manual: Hardware Rev.1.00
M16C/6C Group User’s Manual: Hardware Rev.1.00
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler User’s Manual
M16C Series, R8C Family C Compiler Package V.5.45
C Compiler User’s Manual Rev.1.00
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Revision History	M16C/5LD, M16C/56D, M16C/5L, M16C/56, M16C/6C Group How to Use Timer S Associated Interrupts

Rev.	Date	Description	
		Page	Summary
1.00	Jun 30, 2010	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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