Interfacing the Tsi384 and the Tsi148: Clocking and Reset Considerations

80E1000_AN006_04

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1. Interfacing the Tsi384 and the Tsi148: Clocking and Reset Considerations

This application note details the hardware requirements specific to clocking and reset when designing a board that interfaces the IDT Tsi384 and Tsi148 devices on the PCI/X bus. The following topics are discussed:

Revision History

80E1000_AN006_04, Formal, September 2009

This document was rebranded as IDT. It does not include any technical changes.

80E1000_AN006_03, Formal, October 2008

The "Slave Mode Clocking" section has been updated to show that this mode is the preferred mode of operation.

80E1000_AN006_02, Formal, February 2008

This document includes a slight correction in the units for "Reset Timing".

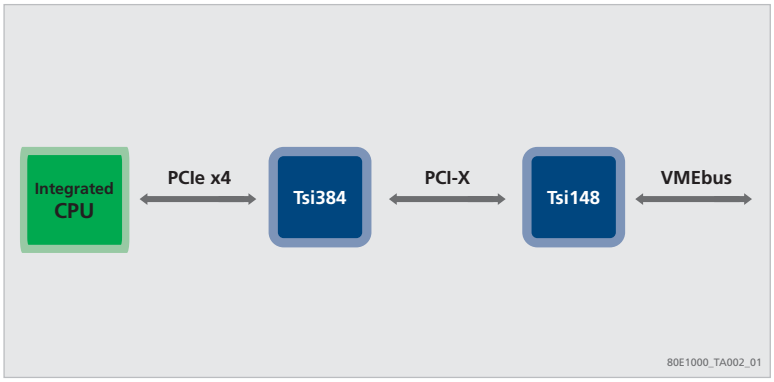
80E1000_AN006_01, Formal, September 2007

This was the first version of this document.

1.1 Overview

The Tsi384 is a PCI Express-to-PCI/PCI-X Bridge designed for forward bridging applications. The Tsi148 is a PCI/X-to-VMEbus Bridge used in applications that require PCI/X access to the VMEbus. The Tsi384 and Tsi148 can be combined and used in designs that require access to the VMEbus when only a PCIe port is available (see Figure 1).

Figure 1: Tsi384 and Tsi148 Typical Application



This document addresses the clocking and reset timing requirements in the following cases:

- Slave Mode Clocking
  - In this mode, an external clock buffer is added to the design and both PCI/X clock inputs to the Tsi384 and Tsi148 are provided externally.
  - This mode is the preferred mode because it allows for flexibility in performing local PCI resets
- Master Mode Clocking
  - In this mode, the Tsi384 provides PCI/X clock outputs to source the PCI/X clock inputs for both the Tsi384 and Tsi148

1.2 Tsi148 Power-on Reset Requirements

The Tsi148 has some specific requirements for power-on reset that must be followed for proper device operation.

At power-up, there are three reset inputs to the Tsi148 that must meet specific timing requirements. The Tsi148 PLL_RSTI_, PURSTI_ and LRSTI_ inputs must be asserted and negated as follows:

- PLL_RSTI_
  - The Tsi148 PLL reset input (PLL_RSTI_) is required to reset the internal PLL and must be held asserted until both power and the PCI/X reference clock (PCLK) are stable
- PURSTI_
  - The Tsi148 power-up reset input (PURSTI_) is a full device reset. The PURSTI_ reset must be held a minimum of 150 us after the de-assertion of PLL_RSTI_ so that the internal PLLs within the Tsi148 can lock.
- LRSTI_
  - At power-up, the Tsi148's local reset (PCI/X reset) input must be held asserted until the PCI/X initialization pattern is stable. Once the pattern is stable, the LRSTI_ input can be negated.

The Tsi384's initialization pattern is stable at a very specific time (see Figure 3 and Figure 2). For more information about timing values, see the *Tsi384 User Manual*.

1.3 Tsi384 Clocking Modes

The system requirements dictate which clocking mode, master or slave, to use in a Tsi384 and Tsi148 application. How the PCI/X clocks are provided dictates the system functionality and the reset requirements between the Tsi384 and Tsi148.

The Tsi148 has a very flexible reset architecture that allows for the PCI/X and VMEbus interfaces to be reset completely asynchronously from each other. However, when the Tsi384 is configured in master mode clocking, the Tsi148 effects VMEbus resources because the Tsi148 must be completely reset when the Tsi384 is reset (see “Master Mode Clocking” on page 6). When the Tsi384 is configured in slave mode clocking, the Tsi148’s local bus (PCI/X) can be independently reset when the Tsi384 is reset (see “Slave Mode Clocking” on page 5).

1.3.1 Slave Mode Clocking

When the Tsi384 is configured to use slave mode clocking, an external clock buffer is required to supply the PCI/X clock inputs to the Tsi384 and the Tsi148. Since the PCI/X clock remains stable through local bus reset (PCI/X), the Tsi148 does not require a complete power-on reset. Operating the Tsi384 with slave mode clocking allows complete flexibility in resetting the Tsi148 after the initial power-on reset.

The Tsi384 inputs reset from upstream devices and drive reset to downstream devices. In the event of a PCIe reset (Cold, Warm, or Hot) the Tsi384 drives its PCI reset output signal (PCI_RSTn). After the initial power-on reset, the PCI_RSTn output can be used to reset the Tsi148 local resources (PCI/X) without effecting the VMEbus resources.

The Tsi148 requires a full power-on reset at initial power-up in order to sample the PCI/X initialization pattern and its internal PLLs can lock to the incoming PCI/X clock (once stable). After the initial power-up reset, the Tsi148’s local reset (PCI/X) input (LRSTI_) can be driven to reset Tsi148 local resources (PCI/X).

Figure 2 describes the required reset timing between the Tsi384 and Tsi148 when operating in clock slave mode. In addition to the external clock buffer, the reset timing requires the use of on-board logic to properly generate the reset inputs to the Tsi148.

Figure 2: Slave Mode Clocking Reset Timing

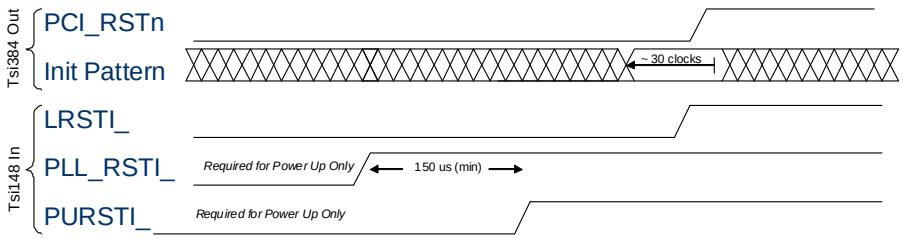


Figure 2 notes:

1. PLL_RSTI_ is de-asserted when the power and clocks are stable

The assertion of PLL_RSTI is only required during power-up reset.

2. PURSTI_ is de-asserted 150 us (minimum after PLL_RSTI is de-asserted
   — This satisfies the timing requirement between PLL_RST_ and PURSTI_.

The assertion of PURSTI_ is only required during power-up reset.

3. LRSTI_ is de-asserted with PCI_RSTn
   a. This latches the Initialization Pattern within the Tsi148.
   b. Initialization Pattern is stable approximately 30 clock cycles prior to the de-assertion of PCI_RSTn
   c. Initialization Pattern is held for two additional PCI/X clock cycles following PCI_RSTn de-assertion

1.3.2 Master Mode Clocking

When the Tsi384 is configured to operate in master mode clocking, the Tsi384 can provide up to five PCI/X clock outputs (PCI_CLKO[4:0]). In a Tsi384 and Tsi148 application, the Tsi384 provides the PCI/X clock source for the Tsi148. When the Tsi384 provides the PCI/X system clocks, the Tsi148 requires a full power-on reset when the is Tsi384 reset. When the Tsi148 receives a full power-on reset the entire device is reset, including both local (PCI/X) and VMEbus resources.

The Tsi148 drives the SRSTO signal to reset the VME bus backplane. Since SRSTO feeds back into the Tsi148's SRSTI input this causes the Tsi148's local reset output (LRSTO) to be asserted. Additional external reset gating logic may be required to ensure the desired system behavior.

1.3.2.1 PCIe Reset

The Tsi384 receives reset notification from upstream devices and drive reset to downstream devices. In the event of a PCIe reset (Cold, Warm, or Hot), the Tsi384 drives its PCI reset output signal (PCI_RSTn). When the Tsi384 is configured to operate in master mode clocking and it receives a PCIe reset, the internal clock logic is reset. This causes the clock generator to go into bypass mode, which generates a 25 MHz output on all its external PCI/X clocks.

Tsi148 and PCIe Reset

Operating the Tsi384 in master mode clocking limits the reset capabilities of the Tsi148 because the Tsi148 must receive a full power-on reset in the event of a Tsi384 reset. When the Tsi384 receives a PCIe reset, the Tsi148's PCLK input changes from its normal operating frequency to 25 MHz. When the operating frequency is reduced to 25 MHz, the Tsi148's internal PLL loses lock and the entire device must be reset. When the internal PLL loses lock, the Tsi148 requires a full power-on reset so that it can re-sample the PCI/X initialization pattern and its internal PLLs can lock to the incoming PCI/X clock (once stable).

The Tsi148 uses its PCI/X clock input (PCLK) as the reference clock for the entire device. All Tsi148 logic is clocked from the output of an internal PLL that uses PCLK as its reference.

A full, power-on reset means the Tsi148's local resources (PCI/X), as well as VMEbus resources are reset. If the intended application requires that VME resources remain stable during local bus (PCI/X) resets, then slave mode clocking must be used (see "Slave Mode Clocking" on page 5).

1.3.2.2 Reset Timing

Figure 3 describes the required reset timing between the Tsi384 and Tsi148 when operating in master mode clocking. The reset timing requires the use of on board logic to properly generate the reset inputs to the Tsi148.

Figure 3: Master Mode Clocking Reset Timing

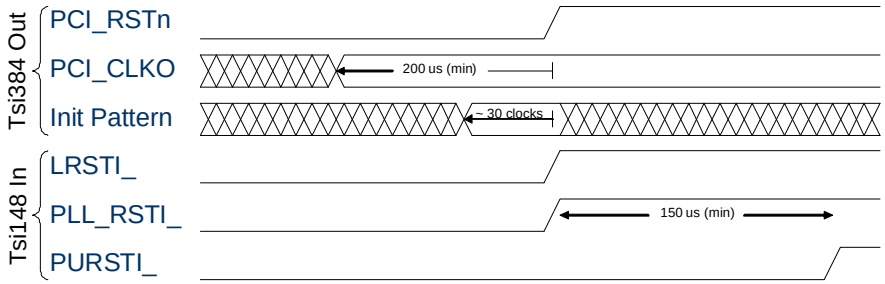


Figure 3 notes:

- Both PCI_CLKO and the Initialization Pattern are stable when PCI_RSTn is de-asserted and the following occurred:
  - PCI_CLKO is stable approximately 200 microseconds prior to the de-assertion of PCI_RSTn
  - Initialization Pattern is stable approximately 30 clock cycles prior to the de-assertion of PCI_RSTn
  - The Initialization Pattern is held for two additional PCI/X clock cycles following PCI_RSTn de-assertion
- LRSTI_ is de-asserted with PCI_RSTn
  - This latches the Initialization Pattern within the Tsi148.

- PLL_RSTI_ is de-asserted with PCI_RSTn
  - This guarantees that both clock and Initialization Pattern are stable.
- PURSTI_ is de-asserted for a minimum of 150 us after PCI_RSTn is de-asserted.
  - This satisfies the timing requirement between PLL_RST_ and PURSTI_.

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