Application Note

Dynamic Range Audio Compressor

AN-CM-327

Abstract

This application note illustrates how to use the SLG47004 to implement a dynamic range audio compressor and describes some of the user-adjustable control parameters and features used to adjust compression.
The application note comes complete with design files which can be found in the References section.

Contents

Figures

Tables

1 Terms and Definitions

CLK	Clock
CNT	Counter
DFF	D Flip-Flop
DLY	Delay
HD	High Drive
LUT	Look Up Table
Op Amp	Operational Amplifier
OSC	Oscillator

2 References

For related documents and software, please visit:

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Download our free GreenPAK Designer software [1] to open the .aap files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Find out more in a complete library of application notes [4] featuring design examples, as well as explanations of features and blocks within the GreenPAK IC.

[1] GreenPAK Designer Software, Software Download and User Guide

[2] AN-CM-327 Dynamic Range Audio Compressor.aap, GreenPAK Design File

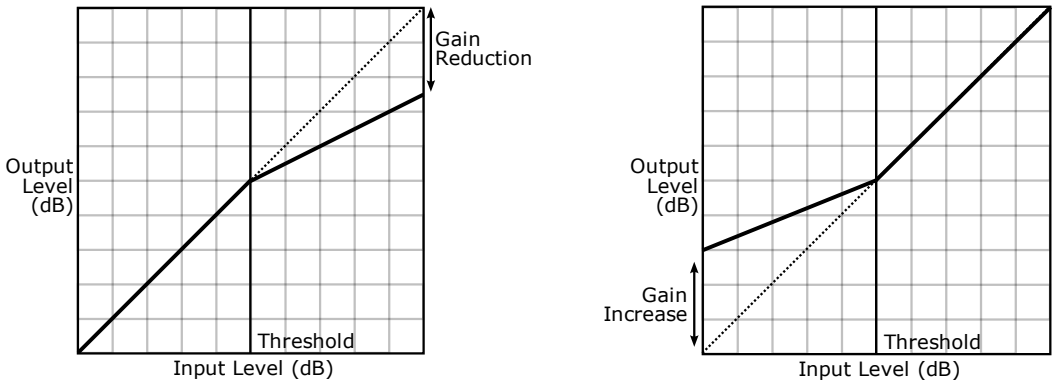
[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage

3 Introduction

Dynamic range compression or simply compression is an audio signal processing operation that reduces the volume of loud sounds or amplifies quiet sounds, therefore reducing or compressing an audio signal's dynamic range. Compression is commonly used in sound recording and reproduction, broadcasting, hearing aid, live sound reinforcement, and in some instrument amplifiers.

There are two types of compression, downward and upward. Both downward and upward compression reduce the dynamic range of the audio signal (see Figure 1).



a) Downward **b) Upward**

Figure 1: Two Methods of Dynamic Range Compression

SLG47004 contains high-performance analog blocks, which can be controlled by customer-defined logic blocks. This combination allows to implement a compressor with adjustable parameters.

This application note illustrates a downward compression, but SLG47004 also allows to implement an upward compression. The downward compression reduces the volume of loud sounds above a certain threshold. The quiet sounds below the threshold remain unaffected. This is the most common type of compressor.

4 System Overview

Figure 2 shows a simplified design based on a feedback layout, where the signal level is measured after an amplifier.

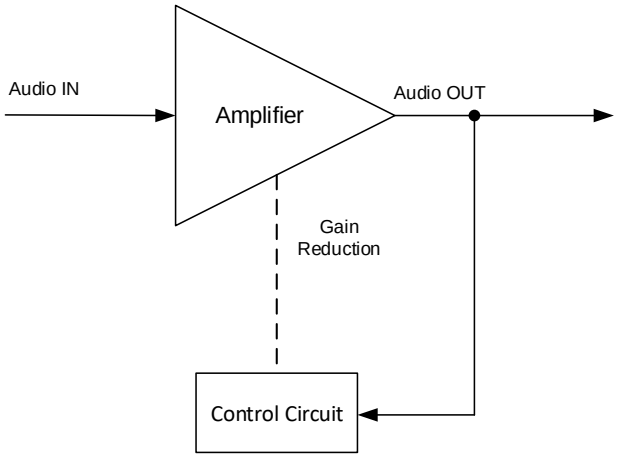


Figure 2: Simplified Design of the Compressor

The full design based on SLG47004 is shown in Figure 3.

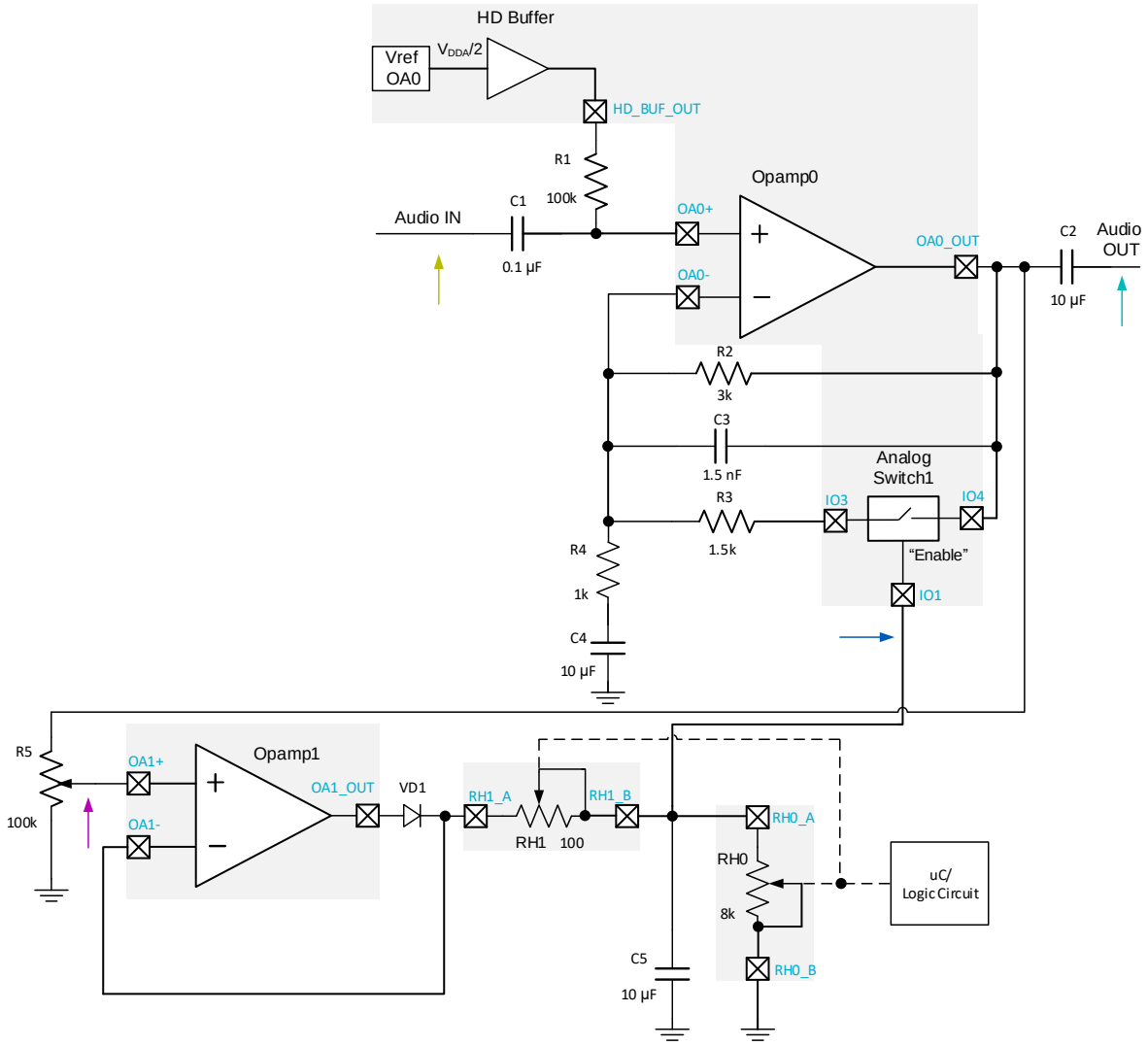


Figure 3: Full Design Based on SLG47004

In this compressor circuit, Op Amp0 is a non-inverting AC amplifier that amplifies input audio signals. A peak detector is based on Op Amp1 and rectifies and determines the peak value of an output amplified signal. An external potentiometer R5 allows to adjust the level of the peak detector output signal. When this level exceeds Pin15 (IO1) threshold voltage, High level voltage on "Enable" input opens Analog Switch and connects resistor R3 to Op Amp0 feedback circuit, as a result reducing the gain. That is, when the output signal reaches the value set by the external resistor R5, the gain decreases from 4 to 2, and when the output signal drops below the value set by that resistor, the gain increases from 2 to 4.

Figure 4, Figure 5, and Figure 6 demonstrate the principle of work of the circuit (yellow curve – input audio signal, light blue curve – output audio signal, purple curve – peak detector input signal, blue curve – peak detector output signal).

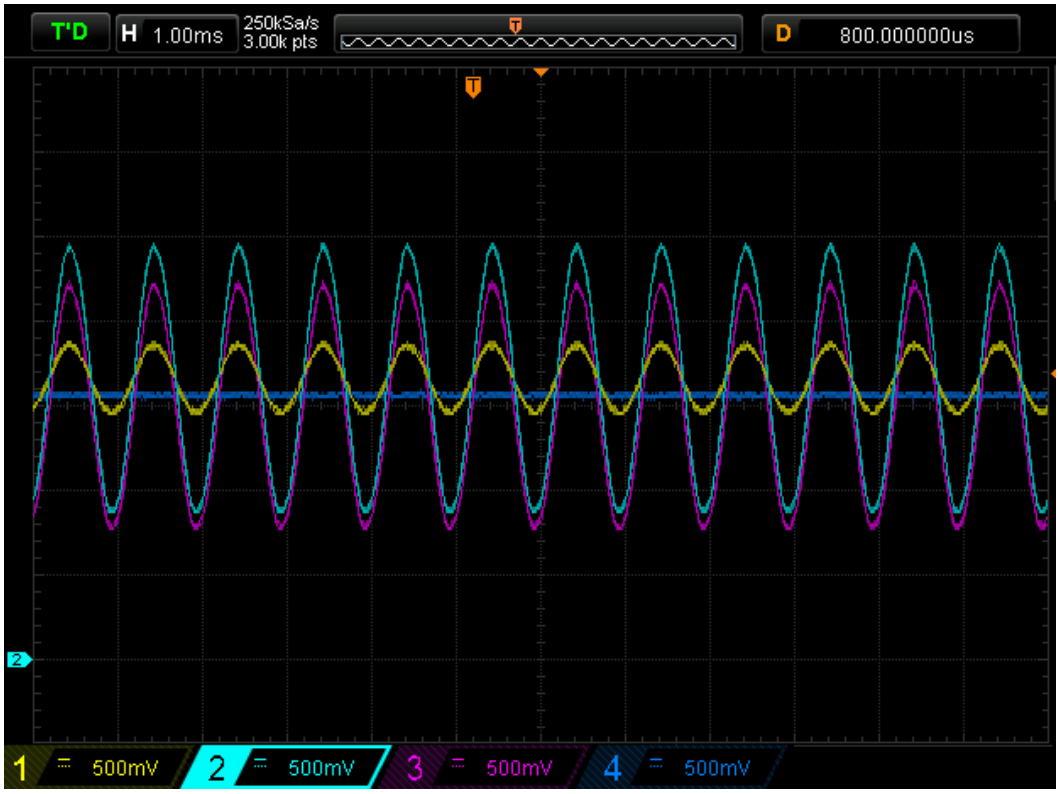


Figure 4: Waveforms before Compressing at V_{IN} = 150 mV, RH0 = 1 kΩ, RH1 = 8 kΩ (Gain = 4)

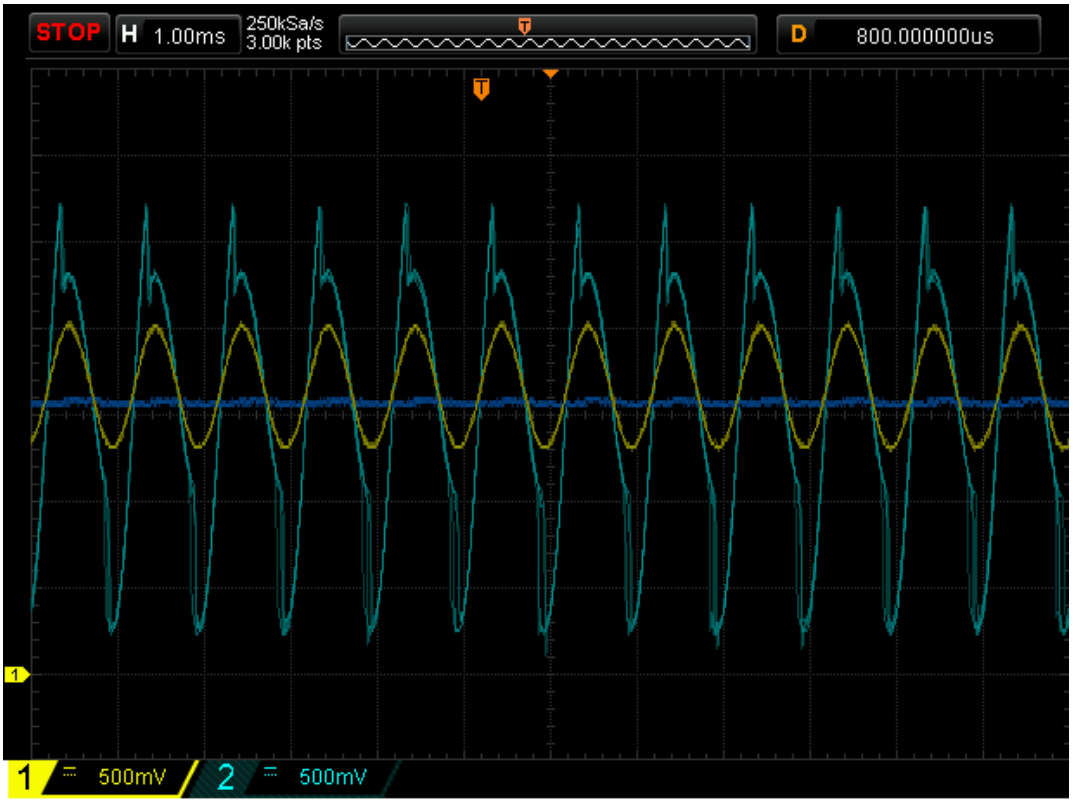


Figure 5: Waveforms during Compressing at V_{IN} = 250 mV, RH0 = 1 kΩ, RH1 = 8 kΩ

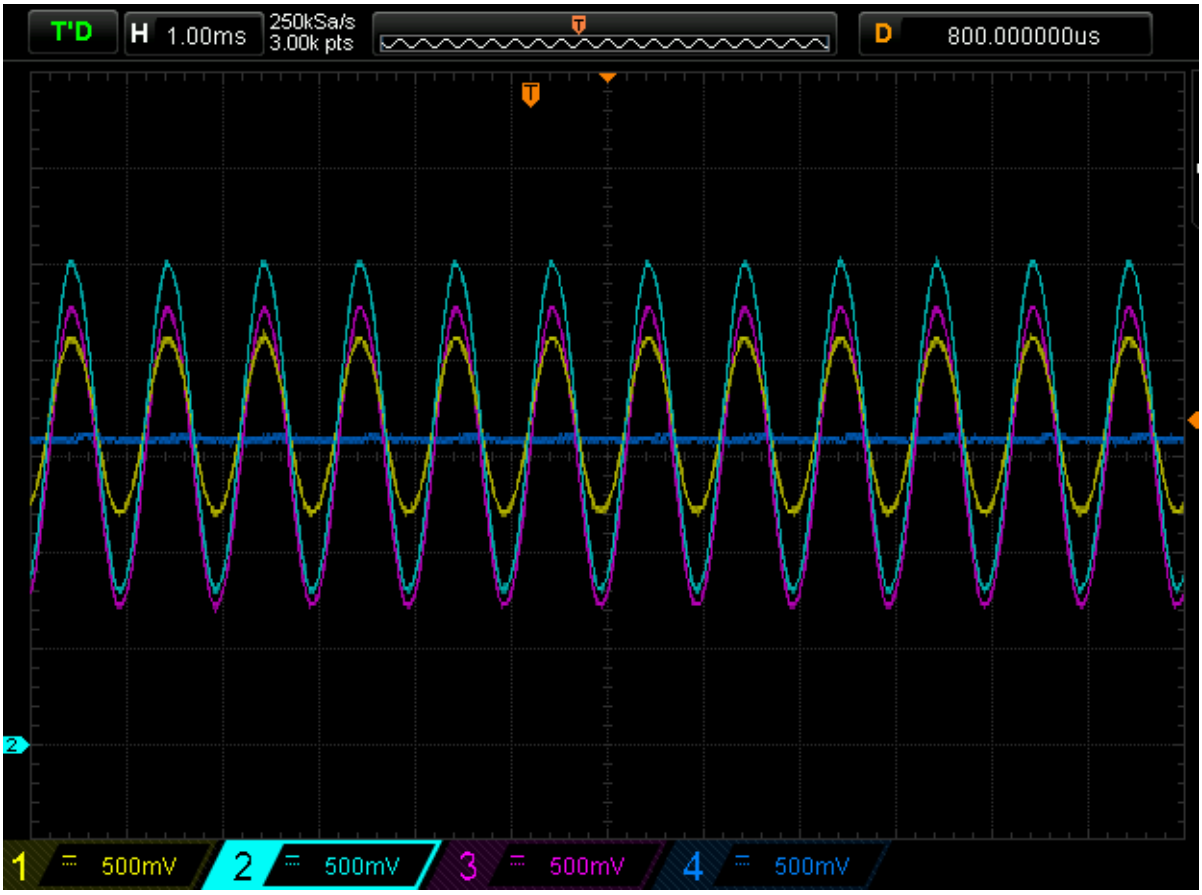


Figure 6: Waveforms after Compressing at V_{IN} = 350 mV, RH0 = 1 kΩ, RH1 = 8 kΩ (Gain = 2)

4.1 AC Amplifier

Op Amp0 amplifies an AC signal, and HD Buffer shifts the input signal, so that it is centered at one-half the power supply voltage. The key benefit of this circuit is that it accepts signals which swing below ground, even though the amplifier does not have a negative power supply.

Resistors R4 and R2 set the amplifier's voltage gain. The voltage gain by default will be equal to:

$$K = \frac{V_{out}}{V_{inp}} = 1 + \frac{R_2}{R_4} = = 1 + \frac{3000}{1000} = 4$$

And after dynamic range compression:

$$K = \frac{V_{out}}{V_{inp}} = 1 + \frac{R_2||R_3}{R_4} = = 1 + \frac{1000}{1000} = 2$$

Capacitor C1 galvanically isolates the amplification circuit from the signal source. It decouples the DC level at input from the DC level the Op Amp is biased at. Its value was chosen to provide a lower cutoff frequency equal to f_L = 16 Hz:

$$C_1 = \frac{1}{2\pi R_1 f_L} = \frac{1}{2\pi * 100000 * 16} = 0.1\ \mu F$$

C2 is another DC blocking capacitor that decouples the Op Amp DC bias level from the output. With the two DC blocking capacitors (C1, C2) the overall amplifier works on AC and whatever DC biases may be at input and output are irrelevant. C2 forms a high-pass filter with whatever impedance is

connected to the output. Because you might not know it, you want to make it reasonably large. That is why the capacitor's value was chosen 10 µF.

If only AC signals are being amplified, it is often a good idea to “roll-off” the gain to unity at DC, to reduce the effect of finite input offset voltage. For this purpose, capacitor C4 was used, which provides a lower cutoff frequency 3 dB point of 16 Hz, the frequency at which the impedance of the capacitor C4 equals R4.

Capacitor C3 intends to reduce noise during compression. Its value was chosen not to influence the frequency response of the amplifier and to filter excessive noise.

4.2 Peak Detector

The peak detector is based on Op Amp 1, capacitor C5, and diode VD1.

Op Amp1 works as a buffer circuit. To avoid an output voltage droop, its good to use a low-leakage diode and capacitor. The value of C5 is a compromise. Leakage currents cause the voltage droop, so C5 should be large to minimize it. But high values generally cannot be used, because they require too much energy to charge and, respectively, high output slew rate. The characteristics of high-value capacitors are largely inconsistent with the requirements of peak detectors. Therefore, the value of C5 was chosen 10 µF.

Resistors RH0 and RH1 allow to change charging and discharging time. Furthermore, RH0 resets the output of the peak detector.

4.3 Attack and Release Control

The compressor may provide a degree of control over how quickly it acts. The attack is the period when the compressor is decreasing gain in response to the increased level at the input to reach the gain determined by the ratio. The release is the period when the compressor is increasing gain in response to the reduced level at the input to reach the output gain determined by the ratio, when the input level has fallen below the threshold.

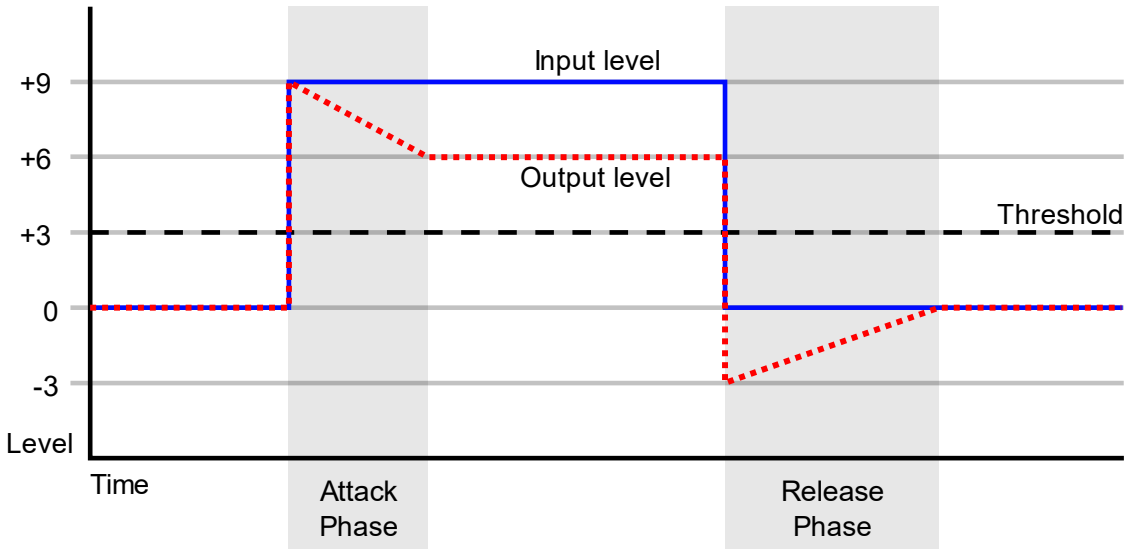


Figure 7: The Attack and Release Phases in a Compressor

The length of each period is determined by the rate of change and the required change in gain. There is no industry standard for the exact meaning of these time parameters.

In the compressor in this application note, the attack and release times are adjustable by the user.

As an example, for the attack time was chosen 10 values: 1 ms, 2 ms, 3 ms, 4 ms, 5 ms, 6 ms, 7 ms, 8 ms, 9 ms, and 10 ms. And for the release time was also chosen 10 values: 80 ms, 90 ms, 100 ms, 110 ms, 120 ms, 130 ms, 140 ms, 150 ms, 160 ms, and 170 ms.

Rheostat RH1 determines the time required to charge capacitor C5, so by changing the value of its resistance can be adjusted the attack time. Rheostat RH0 determines the time required to discharge the capacitor C5, so by changing the value of its resistance can be adjusted the release time.

Due to the flexibility of the SLG47004, there is a possibility to implement two methods of changing the attack/release time independently. The first method requires using an I^2C master.

4.3.1 Changing Attack/Release Time via I^2C

The SLG47004 has an I^2C macrocell that allows reading and writing data to Digital Rheostats. The rheostats resistance data is stored in the registers [C0, C1] for RH0 and [D0, D1] for RH1. I^2C master can write data to these registers and adjust the resistance value of the RH0 and RH1 rheostats. Note that to read the rheostat data I^2C master should read the registers [C2, C3], [D2, D3].

Table 1 summarizes the rheostats digital codes to implement 10 attack and release sets for I^2C control. Moreover, the values of both rheostats can be independently changed.

Table 1: Rheostats Digital Codes and Resistance Values to Adjust Attack/Release Time

Attack Time, ms	Approximate RH1 Value, Ω	Digital Rheostat RH1 Code	Release Time, ms	Approximate RH0 Value, Ω	Digital Rheostat RH0 Code
1	98	0	80	8036	82
2	196	1	90	9016	92
3	294	2	100	9996	102
4	392	3	110	10976	112
5	490	4	120	11956	122
6	588	5	130	12936	132
7	686	6	140	13916	142
8	784	7	150	14896	152
9	882	8	160	15876	162
10	980	9	170	16856	172

This method is simple and allows to connect an LCD and shows on its screen the release and attack time values.

4.3.2 Changing Attack/Release Time via Logic Circuit

Adjusting the attack/release time by I^2C is a convenient method, but it requires an I^2C master. A much simpler method can be implemented with two buttons. Figure 8 shows the attack time control by a button. In the initial time, RH1 = 0 (Digital Code) and the attack time is equal to 1 ms. The button

allows to move up and down from 1ms to 10ms with a 1ms step.

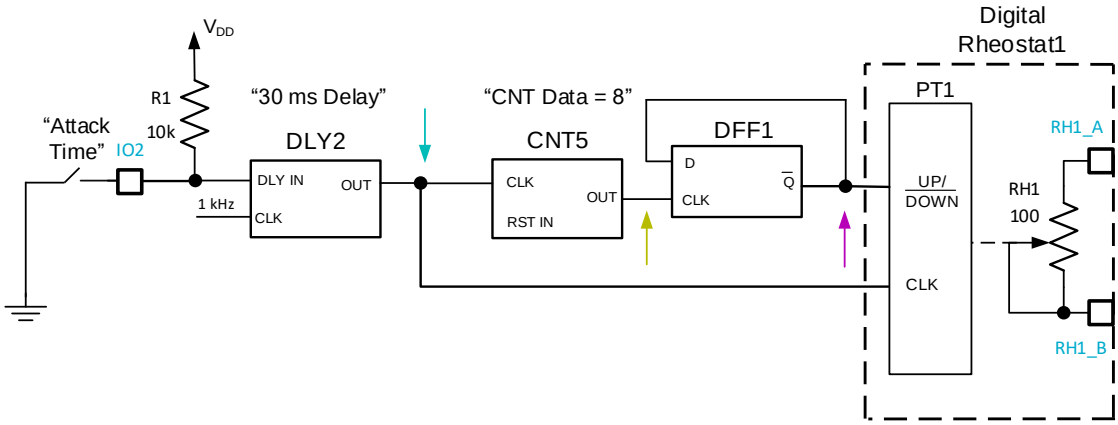


Figure 8: The Attack Time Control by the Button

Delay macrocell works like a deglitch filter to eliminate a switch bouncing. DFF output is High in initial time and this causes increasing Digital rheostat internal counter's value with each press of the button (Up mode). CNT5 counts to 8 and then sets High level on its output. That changes DFF output value to Low and sets Digital rheostat internal counter to Down mode. Figure 9 shows a detailed waveform (light blue curve – button delayed signal, yellow curve – counter output signal, purple curve – DFF output signal).

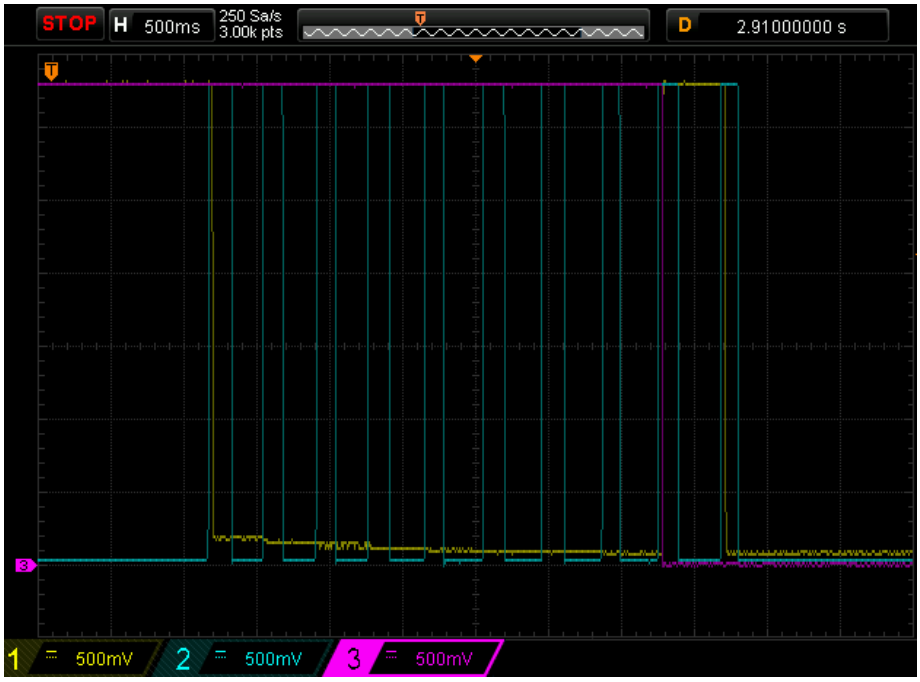


Figure 9: Waveforms for the Attack Time Control by the Button

Figure 10 shows circuitry for the release time control by the button.

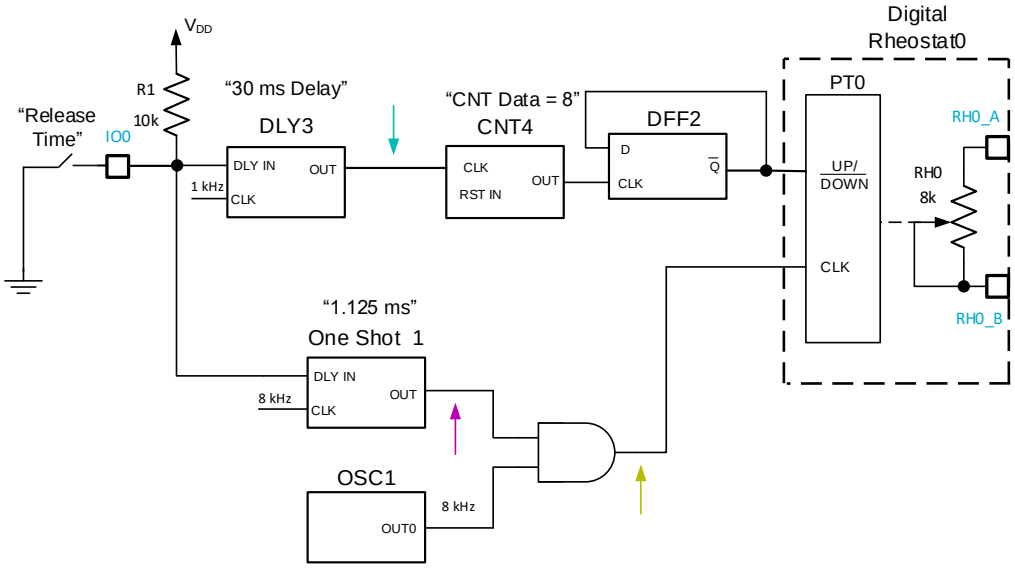


Figure 10: The Release Time Control by the Button

Delay macrocell works like a deglitch filter to eliminate a switch bouncing. DFF output is High in initial time and this causes increasing Digital rheostat internal counter's value with each press of the button (Up mode). CNT4 counts to 8 and then sets High level on its output. That changes DFF output value to Low and sets Digital rheostat internal counter to Down mode. One Shot was used to implement the change of 10 digital codes at once at the press of the button. 1.125 ms pulse duration allows to pass 10 pulses with the frequency equal to 8 kHz. AND gate allows these 10 pulses to pass to the CLK Input of Digital Rheostat.

Figure 11 shows the waveform for the circuit for the formation of 10 pulses at one press of the button (light blue curve – button delayed signal, yellow curve – AND gate output signal, purple curve – One Shot output signal).

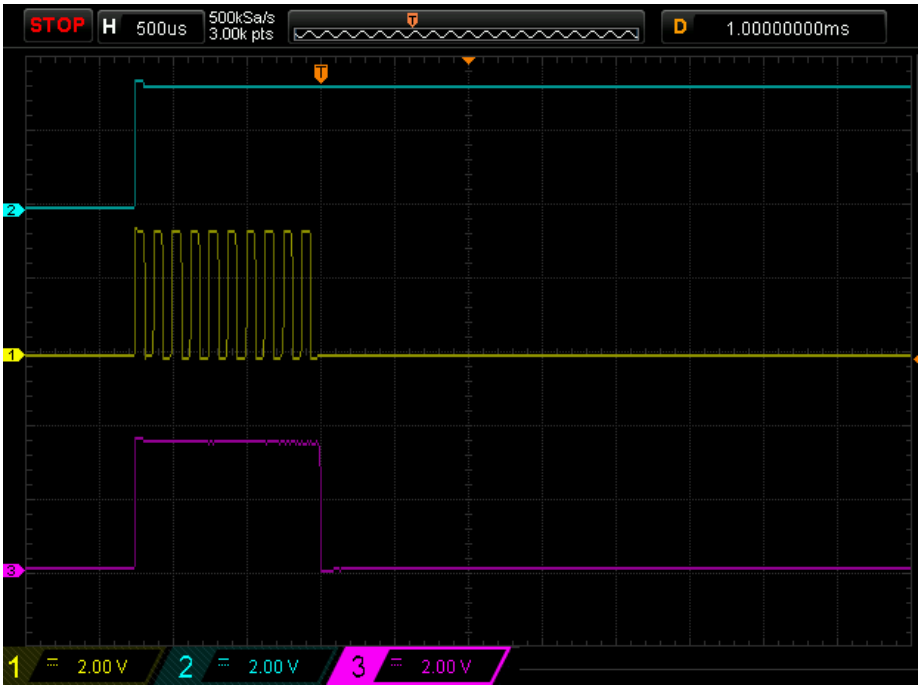


Figure 11: Waveform for Circuit for the Formation of 10 Pulses at One Press of the Button

The advantage of this method is its simplicity, but it has one drawback. The user will not be able to see which time value has been selected and in which of the ten states are the rheostats.

4.4 Compressor Gain Reduction Ratio

The amount of gain reduction is determined by a ratio. Earlier this application note illustrated the ratio of 2:1. But because of the flexibility of the SLG47004, there is a possibility to implement any other gain redaction ratios (see Figure 12).

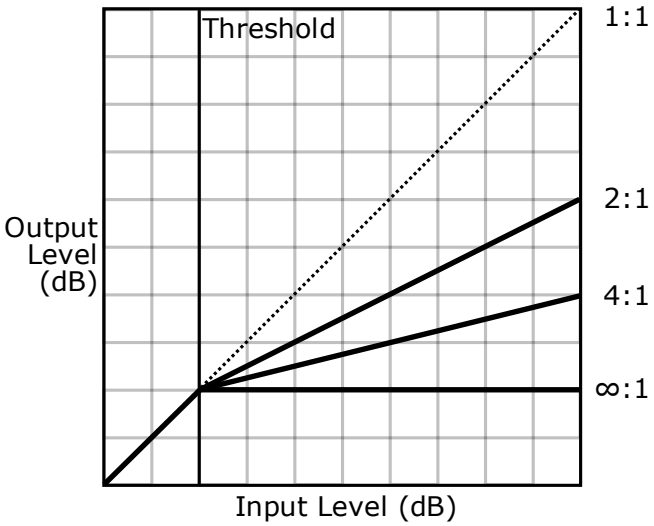


Figure 12: Different Compression Ratios for a Signal Level above the Threshold

The highest ratio of ∞:1 is often known as limiting and effectively denotes that any signal above the threshold is brought down to the threshold level when the attack time has expired.

For example, it can be implemented an audio compressor with the possibility to choose a gain reduction ratio between 2:1 and 3:1 (see Figure 13). In this compressor, one extra button allows to change the ratio. When the peak detector output signal reaches Pin15 (IO1) threshold voltage and the button is not pressed, the counter output keeps Low level of voltage, but LUT1 output becomes High, and respectively, causes High level voltage level on "Enable" input of Analog Switch 1 and opens this switch. The opened switch connects resistor R4 to Op Amp0 feedback circuit, setting the gain reduction ratio to 2:1. Figure: 14 shows detailed waveforms for this design. After pressing the button, the Delay macrocell filters the input pulse to eliminate bouncing. That delayed signal causes a High level signal on the counter's output. In this case, LUT output is Low, but AND gate output – High. This High voltage level on Analog Switch 0 "Enable" input opens it and connects resistor R5 instead of R4, changing the ratio from 2:1 to 3:1.As a result, the alternate pressing of the button causes the alternate switching between analog switches, and accordingly, between the reduction ratios.

To implement this circuitry two external resistors R1, R2 are added instead of HD Buffer to bias the operational amplifier. This is done because HD buffer output and the Analog Switch 0 output A share the same Pin 20 (IO6).

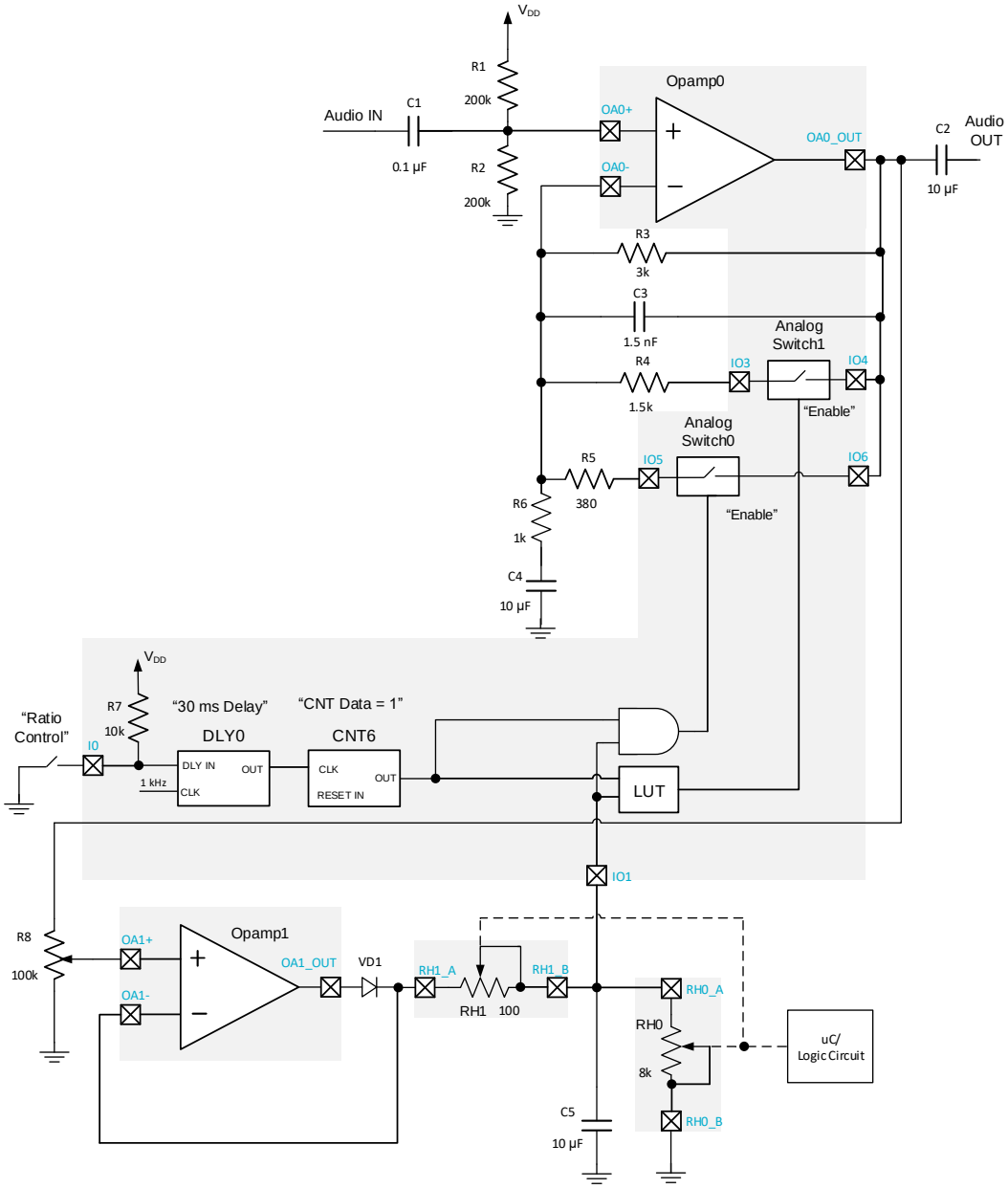


Figure 13: Audio Compressor Design with Gain Reduction Ratio Control

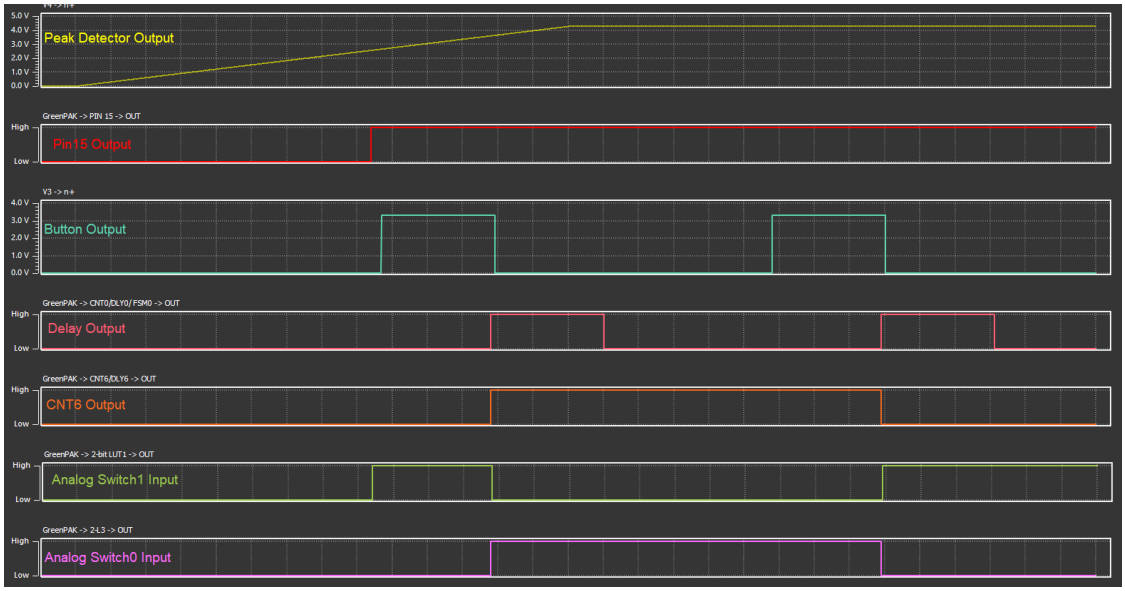


Figure: 14 Waveforms for Audio Compressor with Gain Reduction Ratio Control

5 GreenPAK Design

Figure 15 shows an internal design of the project in GreenPAK Designer software and the second version of the project with the gain reduction ratio control is shown in Figure 16.

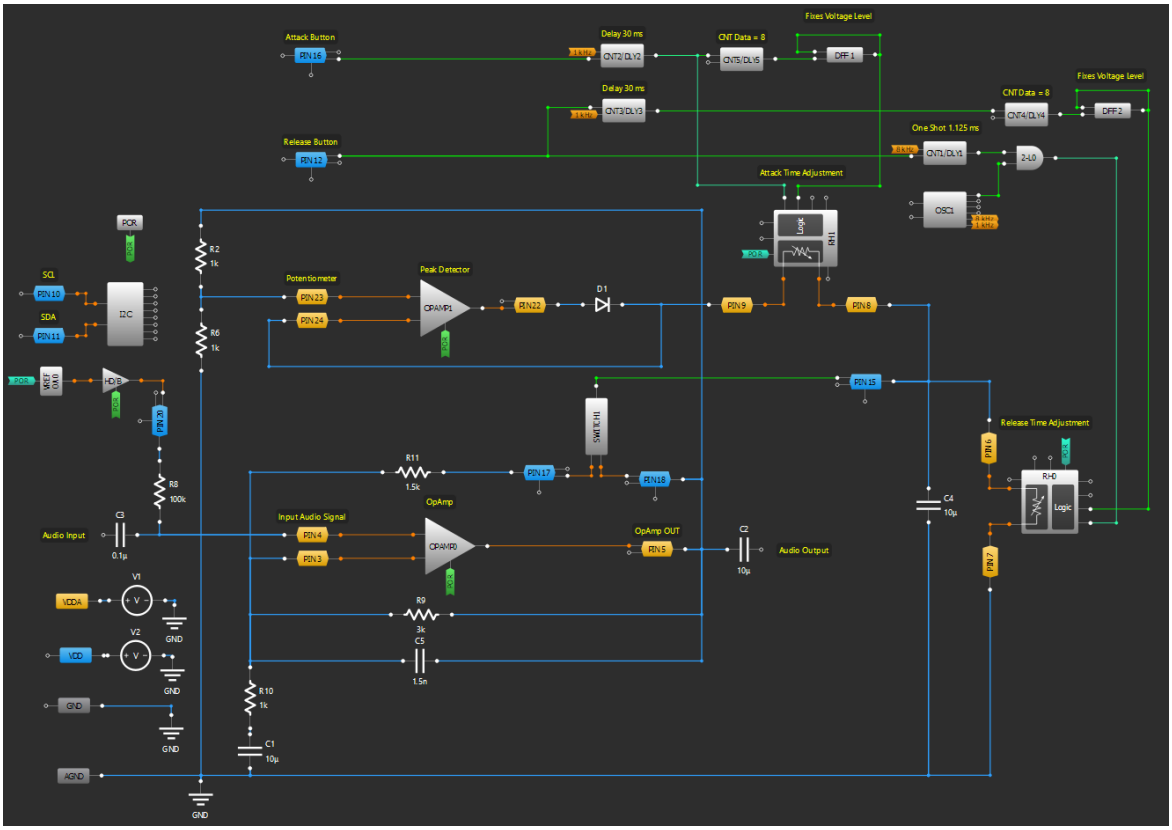


Figure 15: GreenPAK Designer Basic Schematic

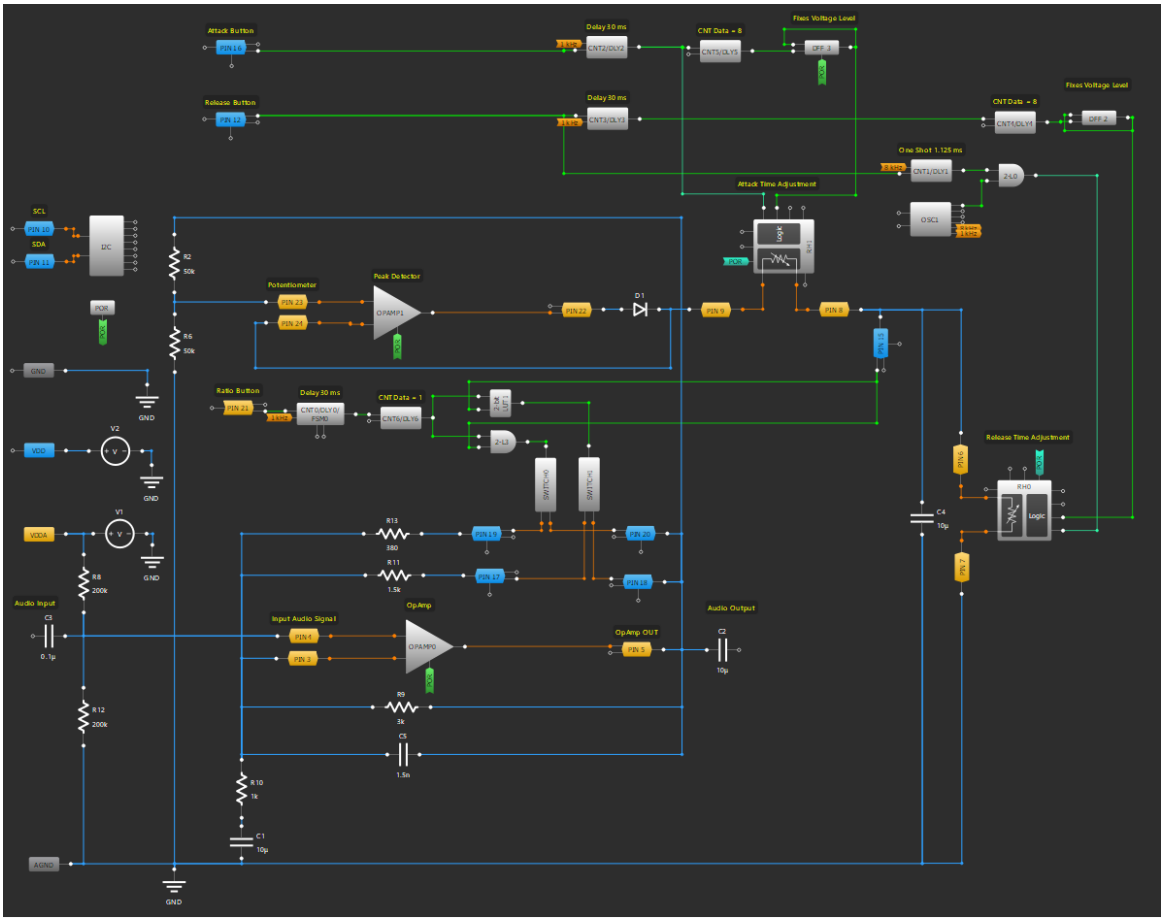


Figure 16: GreenPAK Designer Circuitry with Gain Reduction Ratio Control

5.1 Macrocells Settings

Table 2: LUTs Settings

IN1	IN0	2-bit LUT0 OUT	2-bit LUT1 OUT	2-bit LUT3 OUT
0	0	0	0	0
0	1	0	0	0
1	0	0	1	0
1	1	1	0	1

Table 3: DFFs Settings

Properties	DFFs 2,3
Type	DFF/LATCH
Mode	DFF
Initial polarity	Low
Q output polarity	Inverted (nQ)

Table 4: PINs Settings

Properties	PINs 3, 4, 5, 6, 7, 8, 9, 17, 18, 19, 20, 22, 23, 24	PINs 10, 11, 15	PINs 12, 16, 21
I/O Selection	Analog input/output	Digital input	Digital input
Input Mode	Analog input/output	Digital in without Schmitt Trigger	Digital in with Schmitt Trigger
Output Mode	Analog input/output	None	None
Resistor	Floating	Floating	Pull-up
Resistor Value	Floating	Floating	10 kΩ

Table 5: Counters/Delays Settings

Properties	CNT/DLY 0, 2, 3	CNT/DLY 1	CNT/DLY 4, 5	CNT/DLY 6
Multi-function Mode	CNT/DLY	CNT/DLY	CNT/DLY	CNT/DLY
Mode	Delay	One Shot	Reset Counter	Reset Counter
Counter Data	29	8	8	1
Edge Select	Both	Rising	Rising	Rising
DLY IN init. value	Bypass the initial	Bypass the initial	Bypass the initial	Bypass the initial
Output Polarity	Non-Inverted (OUT)	Non-Inverted (OUT)	Non-Inverted (OUT)	Non-Inverted (OUT)
Mode Signal Sync	Bypass	Bypass	Bypass	Bypass
Clock	OSC1/512	OSC1/64	Ext. CLK (From matrix)	Ext. CLK (From matrix)

Table 6: Op Amps Settings

Properties	**Op Amp0**, 1
Mode	Op Amp Mode
Bandwidth Selection	512 kHz
Charge Pump	Enable CP
Supporting Blocks On/Off	Follows Op Amp
Vref Connection	Disconnected

Table 7: Analog Switches Settings

Properties	Analog Switch 0, 1
Mode	Analog Switch
Big PMOS Control	By Matrix
Small NMOS Enable	Enable by Matrix

Table 8: Digital Rheostats Settings

Properties	Digital Rheostat 0	Digital Rheostat 1
Mode	None	Rheostat
Charge Pump Enable	Always On	Always On
Charge Pump Clock	Auto Selection	Auto Selection
Auto-Trim Disable	Disable	Disable
Active Level for UP/DOWN	Up when High	Up when High
Resistance (Initial Data)	82	0
Up/Down Source	Ext. (From matrix)	Ext. (From matrix)
Clock	Ext. (From matrix)	Ext. (From matrix)

Table 9: OSC Settings

Properties	OSC1
Control Pin Mode	Power-Down
OSC Power Mode	Auto Power-On
Clock Selector	OSC
OSC1 Frequency	2.048 MHz
CLK Pre-divider by	4
OUT0 Second Divider by	64
OUT1 Second Divider by	8

Table 10: HD Buffer Settings

Properties	HD Buffer
Power-Up Source	From Matrix
Power-Up Register	Enable

Table 11: Vref Op Amp0 Settings

Properties	HD Buffer
Enable Selection	From Matrix
Register Enable	Vref Enable
Input Voltage Selection	V_{DDA}
Output Selection	V_{DDA} * (32/64)

Table 12: I²C Settings

Settings	HD Buffer
IO Latching	Disable
Mode Selection	Standard/Fast Mode
Control Code	0001
Control Byte, read/write	0x11/0x10
Device Address, dec/hex	8/0x08

Conclusions

SLG47004 contains high-performance analog blocks, which can be controlled by customer-defined logic blocks. This combination allows to implement the dynamic range audio compressor with user-adjustable control parameters and features. This application note illustrates adjusting attack/release time, compressor threshold, and gain reduction ratio. Furthermore, there were implemented two ways to adjust attack and release time depending on the characteristics of your system and requirements.

Revision History

Revision	Date	Description
1.0	13-Oct-2021	Initial Version

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