Application Note

DA1470x HW Guidelines

AN-B-087

Abstract

This document contains hardware description of the DA14706 PRO development kit, including DA14706 or DA14708 PRO daughterboards, PRO motherboard and the accompanying boards which mounted on the motherboard, namely the LCD module and the power measurement module.

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1 Terms and Definitions

BLE	Bluetooth Low Energy
CS	Chip Select
DCR	DC Resistance
DK	Development Kit
GPIO	General Purpose Input Output
JEITA	Japan Electronics and Information Technology Industries
LDO	Low Drop Out
MAC	Medium Access Controller
OTP	One Time Programmable
PCB	Printed Circuit Board
PDC	Power Domain Controller
PMU	Power Management Unit
PTH	Plated Through Hole
PWM	Pulse Width Modulation
QFN	Quad-Flat No-leads
SDK	Software Development Kit
SIMO	Single Inductor Multiple Outputs (DCDC converter type)
SPI	Serial Peripheral Interface
SRAM	Static Random-Access Memory
SWD	Serial Wire Debug
UART	Universal Asynchronous Receiver/Transceiver
USB	Universal Serial Bus
XIP	Execute in Place

2 References

[1] DA1470x Datasheet (version 3.1)

3 Introduction

This section introduces the subject or problem described in this document. The DA1470x is a family of multi-core wireless microcontrollers, combining:The latest Arm Cortex M33™ application processor with floating-point unit

- Advanced power management functionality
- A Graphic Processing Unit (GPU) for advanced graphics processing
- A cryptographic security engine, analog and digital peripherals
- A dedicated sensor node controller
- A software configurable protocol engine with a radio that is compliant to the Bluetooth® 5.2 low energy standard.

The DA1470x is based on an Arm Cortex-M33™ CPU with an 8-segments Memory Protection Unit (MPU), DSP extensions and a single-precision Floating Point Unit (FPU) offering up to 240 dMIPS. The dedicated application processor executes code from an external Octa/Quad SPI FLASH device.

Bluetooth 5.2 connectivity is implemented by a new software-configurable Bluetooth low energy protocol engine (MAC) with an ultra-low-power radio transceiver. Radio transceiver is capable of +6dBm output power and -97 dBm sensitivity, achieving a total link budget of 103 dB.

2D GPU presents an integrated two-layer display controller with multiple display output options like MIPI-DSI, Parallel and Single/Dual/Quad SPI.

The optimized programmable sensor node controller allows sensor node operations and data acquisition with the rest of the system in shut down mode, achieving best-in-class power consumption.

The advanced power management unit (PMU) of the DA1470x enables it to run on primary and secondary batteries, as well as provide power to external devices through the integrated low quiescent current (I_Q) SIMO DCDC and integrated LDOs. The on-chip JEITA-compliant hardware charger makes it possible to safely charge rechargeable batteries over USB.

A variety of standard and advanced peripherals enable interaction with other system components and the development of advanced user interfaces and feature-rich applications

The differentiation between the members of the DA1470x product family is presented in Figure 1.

Features	DA14701	DA14705	DA14706	DA14708
External PSRAM with Data Cache	✓	×	✓	✓
JEITA Charger	×	✓	✓	✓
Boost DCDC converter	×	✓	✓	✓
eMMC	✓	×	×	✓
Rest of features	✓	✓	✓	✓

Figure 1: DA1470x Product Family Differentiation

There is one single package, the VFBGA142, 6x6 mm, with 0.45 mm pitch and 0.25 mm ball diameter, Figure 2. The various parts of the DA1470x family use the same package but with not connected pads for the not used interfaces. For example, MIPI pins are NC (not connected) for DA14705.

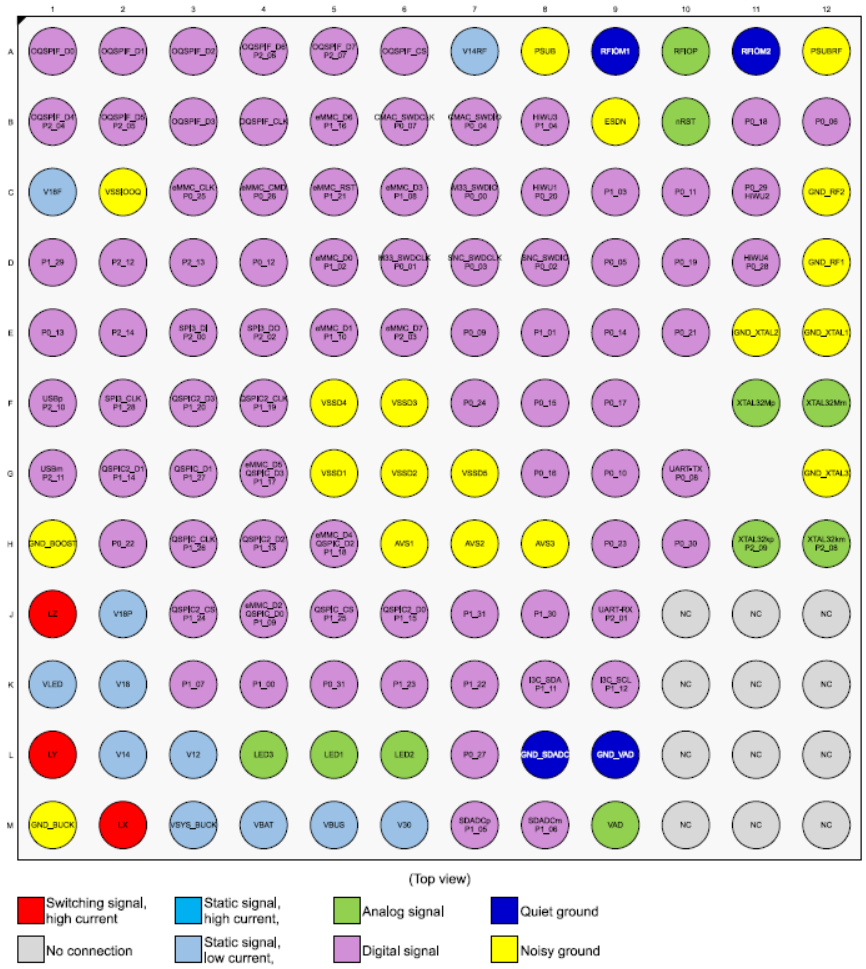


Figure 2: DA1470x Package

4 Design for DA1470x SoC

The DA1470x SoC requires a minimum number of external components for a proper operation. The necessary sections required for the minimal system operation are:

- Power section
- Digital IO
- Crystals
- UART
- JTAG
- Memory
- Radio section

The block diagram of the DA1470x minimal design and the minimal schematics are presented in Figure 3 and Figure 4.

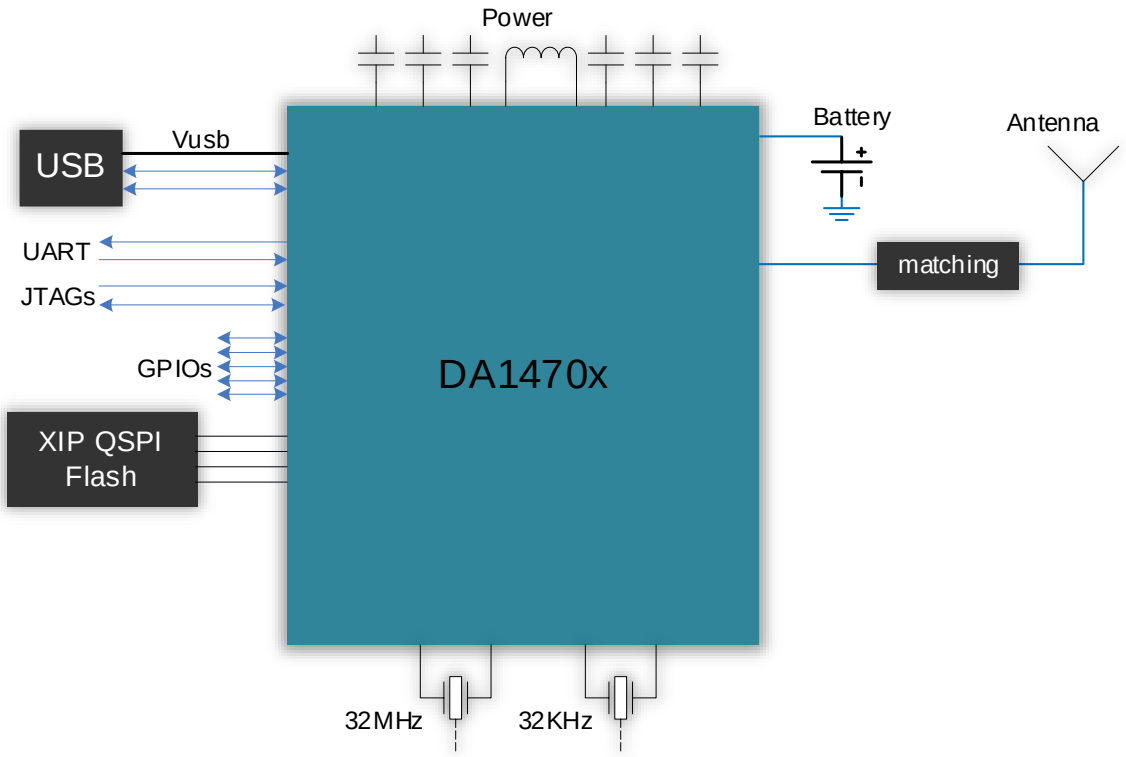


Figure 3: Block Diagram of DA1470x Minimal Design

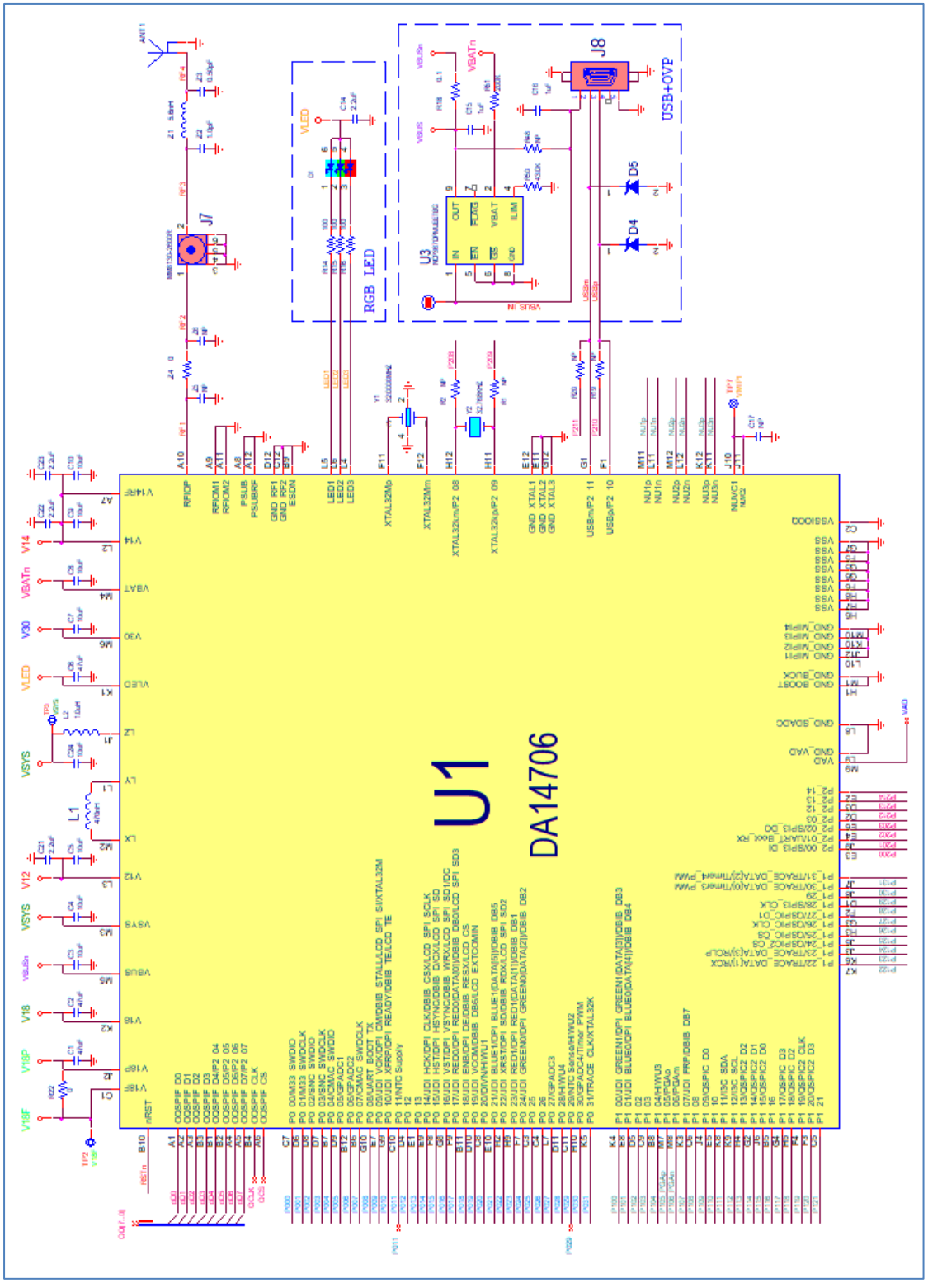


Figure 4: Minimal Design for DA14706

Optional extra functionalities are Storage Flash, PSRAM, LEDs, LCD and others, please see Figure 5.

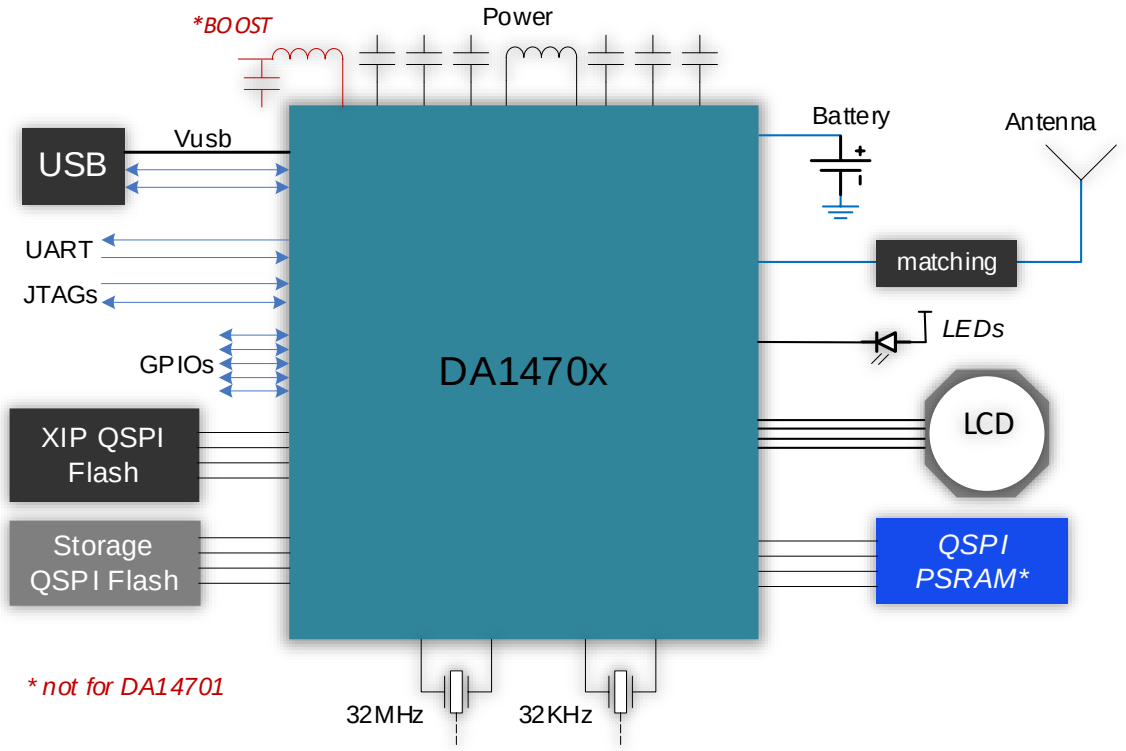


Figure 5: Block Diagram of DA1470x Application Design

4.1 Power Section of DA1470x

PMU provides power for the internal and external loads of the SoC. It is capable of supplying external devices even when the DA1470x is in sleep mode. It consists of:

- A Single Inductance Multiple Output (SIMO) Buck DCDC converter which produce the voltage rails V18, V18P/V18F, V14 and V12. The SIMO DCDC converter is also active in sleep mode and can provide same current as in the active mode to external loads
- A JEITA charger, Constant-Current-Constant-Voltage (CCCV)for battery recharging and a charge detection circuit (it is not available on DA14701)
- A number of LDOs for the different power rails of the system
- A Boost DCDC converter with bypass for powering LEDs (not available for DA14701)
- A VSYS rail. In fact, the main feature of the PMU is the existence of the VSYS pin which is used to hook up all external loads of the systems

There are two main power inputs, VBUS and VBAT. The VBUS is connected when a battery is being charged through the USB connector.

There are certain parts of the power management unit (PMU) which are always powered. They are marked red in Figure 6. HW and SW enabled blocks are marked with green and black respectively.

VBUS or VBAT (depending which is higher) supplies the always powered circuits. The rest of the power system, including SIMO DCDC converter, the LDOs and the Boost DCDC converter are supplied from VSYS power rail. VSYS is supplied from VBUS or/and VBAT.

The power rails with voltage range and current capability is presented on Table 1.

Table 1: DA1470x Generated Power Rails

Rail	Voltage Range (V)	Current Capability (mA)
VSYS	2.4 to 4.8	1000
V30	2.0 to 3.0/3.3	10/150
V18	1.2/1.8	100
V18P	1.8	100
V18F	1.8	30
V14	1.4	20
V12	0.75/0.9/1.2	150
VLED	4.5/5.0	150

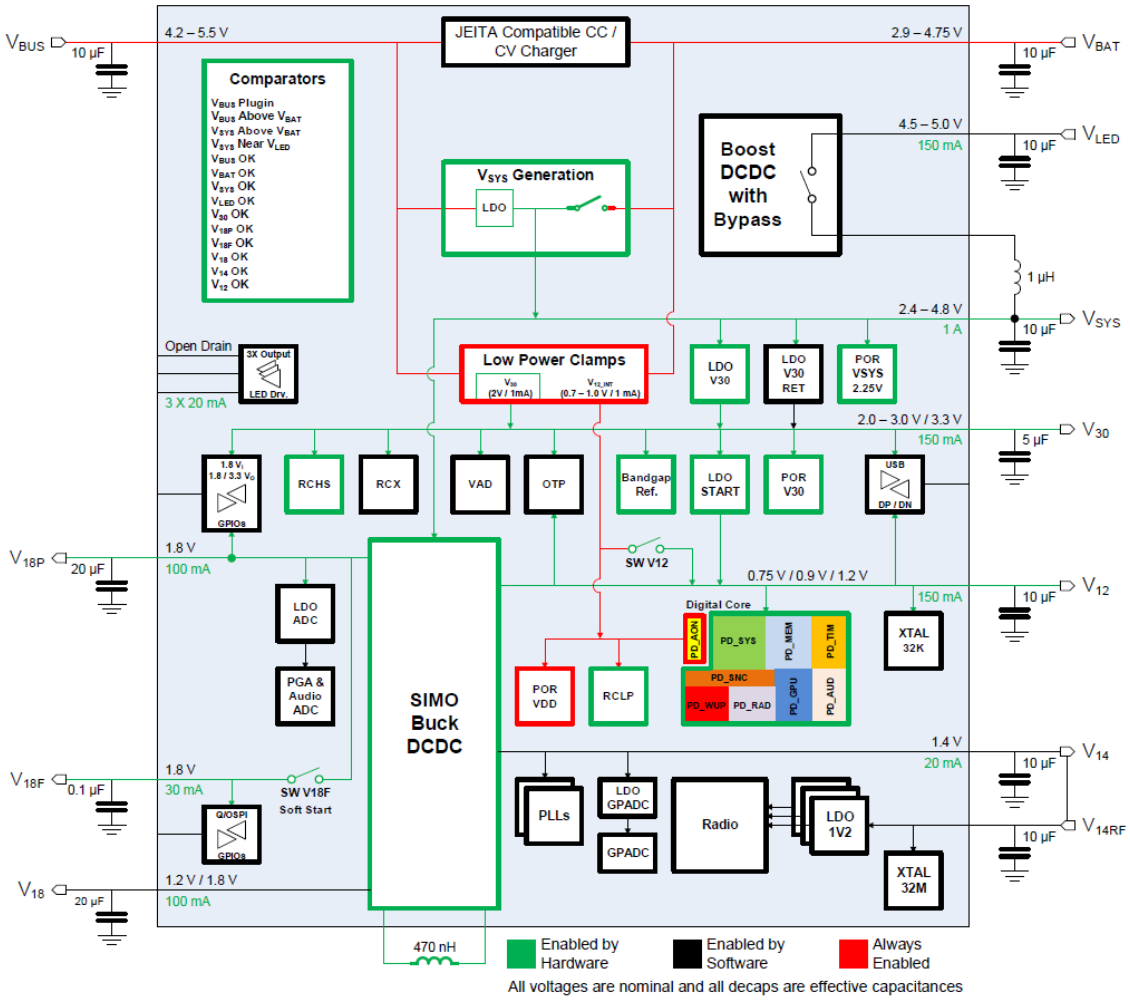


Figure 6: DA1470x Power Management Unit Block Diagram

The DA1470x SoC contains internally all power management for proper and safe system operation. Figure 7 shows the required external components, like decoupling capacitors and inductors.

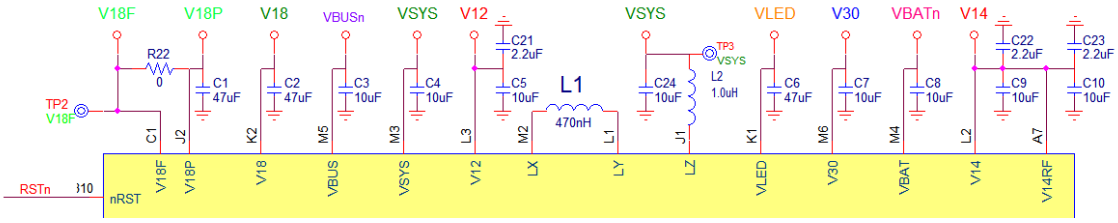


Figure 7: Power Section of DA1470x SoC

- **VBUS:** is the power input pin used for charging and VSYS supply. When VBUS is available then the battery can be charged while all system's loads (internal or external) will be supplied from VSYS.

  As the power input, a decoupling capacitor with effective capacitance between 2.2 µF and 100 µF must be used. For the case of being supplied from USB, a capacitor equal to 10 µF must be placed close to the VBUS pin.

  The voltage range for VBUS is 4.2 V to 5.5 V whereas the absolute maximum operating voltage for this pin is 6.5 V.

  A significant challenge on product level that designers need to deal with is the use of commercially available chargers for charging. The output voltage of these chargers can be as high as 20 V. To prevent damages to the DA1470x SoC or other low voltage system components, the addition of an external overvoltage protection (OVP) circuit is recommended.

  OVP also protects VBUS pin for cable damping and inrush current limiting.

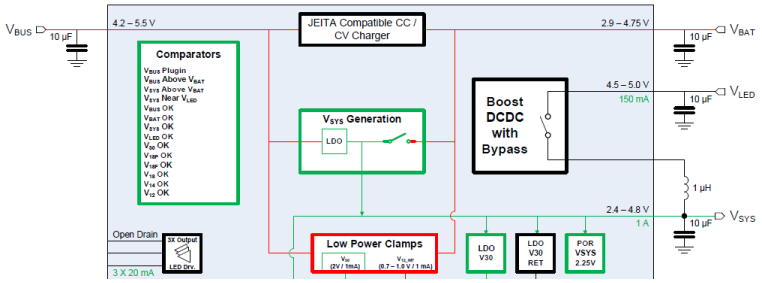
  In case however that no OVP circuit is used, it is recommended to apply an RC network of 0.39 Ω resistor in series to USB power pin and a 10 µF/10V capacitor close to VBUS pin. An alternative combination is to use 0.56 Ω with 4.7 µF/10V placed as close as possible to the VBUS pin of DA1470x SoC.

  Plugging VBUS can be used for waking up the system from sleep or hibernation mode.

  VBUS supply pads are equipped with additional snapback ESD protection devices.

- **VBAT:** The battery is connected to this pin and supplies the VSYS generation block. A decoupling capacitor with effective capacitance between 2.2 µF and 100 µF, must be placed the closest possible to the pin. A 10 µF/6.3V or higher value decoupling capacitor (C8) is recommended. The voltage range for VBAT is 2.8 V to 4.75 V.
- **VSYS:** This power rail supplies all internal (except lower power clamps) and external loads of the DA1470x SoC. It can provide up to 1 A to external loads with voltage range of 2.5 V to 4.8 V

  Internal VSYS generation block is supplied by VBUS or/and VBAT, depending on higher voltage (maximum drop out voltage 300 mV @ 1 A). During charging, the charger provides the charging current to the battery while VBUS supplies the rest of the system. If VBUS cannot provide enough current, VBAT switch closes automatically to help VSYS load



A decoupling capacitor with effective capacitance between 2.2 µF and 100 µF, must be connected to VSYS pin. A 10 µF/10 V or higher value decoupling capacitor (C4) is recommended.

- **V30:** This is the 3V LDO output rail supplied by VSYS. A decoupling capacitor with effective capacitance between 2.2 µF and 100 µF, must be placed the closest possible to the pin. A 10 µF/6.3 V or higher value decoupling capacitor (C4) is recommended.

  Notice: The V30 voltage rail cannot deliver more than 500 uA in hibernation mode. The V30 rail cannot be turned off.

- **SIMO DCDC converter:** This power the V18P, V18, V14, and V12 rails. The inductor needed for DCDC operation is connected externally. The low DC resistance inductor (L1) of 470 nH, (package 0805), is connected to the LX/ LY pins. The SIMO DCDC converter has a low quiescent current (<1 µA) and it is not turned off in sleep mode. Presenting a typical efficiency of 80 %, the SIMO DC/DC converter reduces the battery current consumption during sleep.
- **V18 and V18P:** These supply rails are generated from the SIMO DCDC converter and they can deliver up to 100 mA to external devices in active or sleep mode. They present a maximum ripple of 50 mV.

  Effective capacitance for the two rails must be between 18 µF and 22 µF. This can be met with either a 47 µF MLCC capacitor or two capacitors in parallel. For saving PCB area, 47 µF/6.3 V (0603 package) is recommended (C1 and C2). Capacitors must be placed the closest possible to V18 and V18P pins.

  The V18P voltage rail is used to supply the GPIOs when the GPIOs are set to 1.8 V.

  The V18 rail may be used for supplying external devices like sensors or RF power amplifier. Please note that the V18P and V18 power rails can be turned off.

- **V18F:** This is generated from V18P, through an internal semiconductor switch. It delivers, 1.8 V to the external XIP OQSPI FLASH (V18F) as well as the OQSPI I/Os connected to this FLASH. V18F can deliver up to 30 mA. (Figure 6).

  A decoupling capacitor with effective capacitance between 0.1 µF and 2 µF is required for this rail. The effective capacitance must be less than 10% of the effective capacitance used for V18P power rail. A 1 µF can be used for decoupling capacitors (C11). Also, more than one 0.1 µF capacitors can be used.

- **V12:** This power rail supplies the digital core of the DA1470x and delivers up to 150 mA at 1.2 V when in active or sleep mode. This rail should not be used for supplying external devices. An effective capacitance in the range of 9 µF to 11 µF must be placed on the correspondent pin. Either a 22 µF or two parallel capacitor of 10 µF/0402 (C5) and 2.2 µF/0201 (C21) can be used for meeting this requirement.
- **V14:** This supply rail is generated from SIMO DCDC converter and delivers up to 20 mA at 1.4 V. It should not be used for supplying external devices. An effective capacitance of 9 µF to 11 µF must be applied. Either a 22 µF or two parallel capacitor of 10 µF/0402 (C9) and 2.2 µF/0201 (C22) can be used for meeting this requirement.
- **V14_RF**: Input pin. It is shorted to V14 and it powers the RF circuits via several dedicated internal LDOs. An effective capacitance of 9 µF to 11 µF must be applied closest possible to the pin for best and most stable RF performance. Either a 22 µF or two parallel capacitor of 10 µF/0402 (C10) and 2.2 µF/0201 (C23) can be used for meeting this requirement.
- **VLED**: It is generated from Boost DCDC converter with programmable voltage 4.5V/4.75V/5V and current capability up to150 mA. Boost is supplied from VSYS with an external connection and it is enabled when it is needed. An inductor 1 µH (ESR_{MAX} = 0.15 Ω and maximum saturation current of 1 A) and 10 µF is recommended.

In tables below you can see a selection of decoupling capacitors for cost (Table 2) and PCB area optimization (Table 3). In some cases, a capacitor's value is higher than the recommended due to derating degradation being taken into account.

Table 2: Example of Decoupling Capacitors for Cost Optimization

DA1470x	Specification Effective Load Capacitance			Capacitors		
PIN	**Min**	**Typ**	**Max**	**Value**	**Effective Capacitance**	**Part Number**
VBAT	2.2 µF	10 µF	100 µF	10 µF 0402 6.3 V X5R	2.45 µF for 4.75 V	GRJ155R60J106ME11
VBUS	2.2 µF	10 µF	100 µF	10 µF 0402 6.3 V X5R	2.24 µF for 5 V	GRJ155R60J106ME11
VSYS	2.2 µF	10 µF	100 µF	10 µF 0402 6.3 V X5R	2.38 µF for 4.8 V	GRJ155R60J106ME11
VLED	9 µF	10 µF	11 µF	47 µF 0603 6.3 V X5R	9.5 µF for 5.3 V	GRM188R60J476ME15
V30	2.2 µF	5 µF	100 µF	10 µF 0402 6.3 V X5R	3.607 µF for 1.2 V	GRJ155R60J106ME11
V12*	9 µF	10 µF	11 µF	2.2 µF 0402 10 V X5R	2 µF for 1.2 V	GRM155R61A225KE01
				10 µF 0402 6.3 V X5R	7.95 µF for 1.2 V	GRJ155R60J106ME11
V14*	9 µF	10 µF	11 µF	2.2 µF 0402 10 V X5R	1.9 µF for 1.4 V	GRM155R61A225KE01
				10 µF 0402 6.3 V X5R	7.39 µF for 1.4 V	GRJ155R60J106ME11
V14RF*	9 µF	10 µF	11 µF	2.2 µF 0402 10 V X5R	1.9 µF for 1.4 V	GRM155R61A225KE01
				10 µF 0402 6.3 V X5R	7.39 µF for 1.4 V	GRJ155R60J106ME11
V18*	18 µF	20 µF	22 µF	10 µF 0402 6.3 V X5R	6.26 µF for 1.8 V	GRJ155R60J106ME11
				22 µF 0603 6.3V X5R	16 µF for 1.8 V	GRM187R60J226ME15
V18P*	18 µF	20 µF	22 µF	10 µF 0402 6.3 V X5R	6.26 µF for 1.8 V	GRJ155R60J106ME11
				22 µF 0603 6.3 V X5R	16 µF for 1.8 V	GRM187R60J226ME15
V18F	0.1 µF	0.1 µF	2 µF	0.1 µF 0201 16 V X5R	0.09 µF for 1.8 V	GRM033R61C104ME18

Note 1 Higher voltage rate can be used on capacitors if improves cost and availability.

* Implies parallel connection of the capacitors.

Table 3: Example of Decoupling Capacitors for PCB Area Optimization

DA1470x	Specification Effective Load Capacitance			Capacitors		
PIN	Min	Typ	Max	Value	Effective capacitance	Part Number
VBAT	2.2 µF	10 µF	100 µF	10 µF 0402 6.3 V X5R	2.45 µF for 4.75 V	GRJ155R60J106ME11
VBUS	2.2 µF	10 µF	100 µF	10 µF 0402 6.3 V X5R	2.24 µF for 5 V	GRJ155R60J106ME11
VSYS	2.2 µF	10 µF	100 µF	10 µF 0402 6.3 V X5R	2.38 µF for 4.8 V	GRJ155R60J106ME11
VLED	9 µF	10 µF	11 µF	47 µF 0603 6.3 V X5R	9.5 µF for 5.3 V	GRM188R60J476ME15
V30	2.2 µF	5 µF	100 µF	10 µF 0402 6.3 V X5R	3.607 µF for 1.2 V	GRJ155R60J106ME11
V12	9 µF	10 µF	11 µF	22 µF 0603 6.3 V X5R	19.6 µF for 1.2 V	GRM187R60J226ME15
V14	9 µF	10 µF	11 µF	22 µF 0603 6.3 V X5R	18.3 µF for 1.4 V	GRM187R60J226ME15
V14RF	9 µF	10 µF	11 µF	22 µF 0603 6.3 V X5R	18.3 µF for 1.4 V	GRM187R60J226ME15
V18	18 µF	20 µF	22 µF	47 µF 0603 6.3 V X5R	24.55 µF for 1.8 V	GRM188R60J476ME15
V18P	18 µF	20 µF	22 µF	47 µF 0603 6.3 V X5R	24.55 µF for 1.8 V	GRM188R60J476ME15
V18F	0.1 µF	0.1 µF	2 µF	0.1 µF 0201 16 V X5R	0.09 µF for 1.8 V	GRM033R61C104ME18

4.1.1 PMU Differences between DA1470x and DA1469x

The PMU of DA1470x presents the following new features in comparison to DA1469x

- New VSYS rail for external loads
- SIMO Buck DCDC converter is always on, presenting Low I_Q < 1 uA and typical efficiency 80 %
- Boost DCDC 4.5 V-5 V, 150 mA
- Buck SIMO, always active
- Removed all IO LDOs
- Power is provided by the always-active SIMO DC/DC converter
- Low power clamp for clockless supply (Hibernation)
- Separate LDO for MIPI supply. MIPI interface voltage can be adjusted in the range of 0.9 to 1.25 V

4.2 Reset Pin (nRST)

nRST, (reset pin B10) is active low and it is referred to V12. It contains a RC filter for spikes suppression with 400 kΩ resistor and a 2.8 pF capacitor. It also includes a 25 kΩ pull-up resistor. This pad should be driven externally using a FET or a single button connected to Ground. The typical latency of the RSTN pad is about 2 µs.

4.3 Digital I/O Pins

The DA1470x has a software-configurable I/O pin assignment organized into three ports Port0. Port1 and Port2. There are also dedicated pins for MIPI interface which are not included into the three I/O ports. The following information on the characteristics of the I/O pins operation is very useful for system designers:

- Port 0: 32 pins, Port 1: 32 pins and Port2: 15 pins
- Dedicated pins for XIP Flash QSPI interface. Pins are referenced to 1.8 V ONLY
- Fixed assignment for O/QSPI, QSPI (**QSPIC & QSIC2**), SPI3, eMMC and SDIO. These interfaces are referred to 1.8 V ONLY. So, all GPIOs multiplexed with these functions are 1.8 V ONLY
- Fixed assignment for analog pins, XTAL, NTC and ADC (General purpose and ΣΔ)
- For GPIOs functionality, selectable 25 kΩ pull-up or pull-down resistors per pin
  - Programmable open-drain functionality
  - Pull-up voltage at V30 or V18P. Voltage configurable per pin (except for fixed pins)
  - Pins can retain their last state by using always-on latches when system enters the extended, deep sleep, or hibernation mode.

In Table 4 there is a list of GPIOs that might affect radio performance when being toggled while RF activity occurs. It is recommended to use them at low speed and not to use them when radio is active. These GPIOs support a Reduced Driving Strength (RDS) capability where the rising and falling edges become less steep. If for any reason some of these GPIOs still have to be used for toggling, then RDS can be used to reduce interference to radio performance.

Table 4: Noisy GPIOs Table

GPIO	RDS
P0_02	yes
P0_03	yes
P0_04	yes
P0_06	yes
P0_07	yes
P0_09	yes
P0_11	yes
P0_18	yes
P0_20	yes
P1_01	yes
P1_03	yes
P1_04	yes
P2_09	yes

4.4 Crystals and Clocks

DA1470x clocking elements of interest on HW design are:

- **XTAL32M**: A 32 MHz capable crystal oscillator which is used to generate the 32 MHz clock required for the Analogue PHY (Radio) as well as the source of all system clocks.
- **XTAL32K:** This is a crystal oscillator which is used for the low power clock of the system and should be able to operate with external crystals of 32 kHz or 32,768 kHz. Crystal Constraint should be up to ±500 ppm.
- **RCX**: This is an XTAL32K replacement and the main frequency should be in the range of 15 kHz.
- **RCHS**: This is an internal RC oscillator running at 64 MHz or 96 MHz, used for the initial CPU clocking until the XTAL is settled.
- **RCLP**: This is an internal RC oscillator with a frequency of 32 kHz/512 kHz.

The DA1470x SoC is equipped with two Digitally Controlled Crystal Oscillators (DCXO), one at 32 MHz (XTAL32M) and the other at 32.768 kHz (XTAL32K). XTAL32K has no trimming capabilities and

is used as the low power clock for the extended/deep sleep modes. XTAL32M can be trimmed by using the internal capacitor bank.

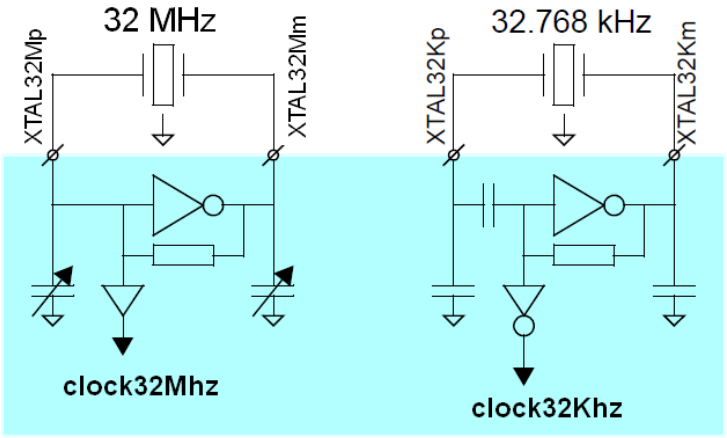


Figure 8: XTAL32M and XTAL32K Oscillator Circuits

4.4.1 32 MHz Clock

The DA1470x needs an accurate 32 MHz clock for proper operation. The clock can be generated either by an external 32 MHz crystal or by applying an external 32 MHz clock signal.

The XTAL32M crystal oscillator can be trimmed. No external components are required other than the crystal itself. If the crystal has a case connection, it is advised to connect the case to ground (Figure 9).

The C_{LOAD} value (CL) of the used 32 MHz crystal preferably would be 6 pF typical. Please check the notes on C_L below. The crystal's ESR must not exceed 100 Ω. Please refer to Table 5.

Table 5: XTAL32M Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
F_{XTAL} (32M)	crystal oscillator frequency			32		MHz
ESR (32M)	equivalent series resistance				100	Ω
C_L (32M)	load capacitance	No external capacitors are required	4	6	8	pF
C_0 (32M)	shunt capacitance				7	pF
Δf_{XTAL} (32M)	crystal frequency tolerance	After optional trimming; including aging and temperature drift (Note 1)	-15		+15	ppm
Δf_{XTAL} (32M) UNT (Note 1)	crystal frequency tolerance	Untrimmed; including aging and temperature drift	-40		+40	ppm

Note 1 Using the internal capacitor bank, a wide range of crystals can be trimmed to the required tolerance.

Note 2 This is the maximum allowed frequency tolerance for compensation by the internal capacitor bank trimming mechanism and using a typical 32 MHz crystal having a CL value of 6 pF.

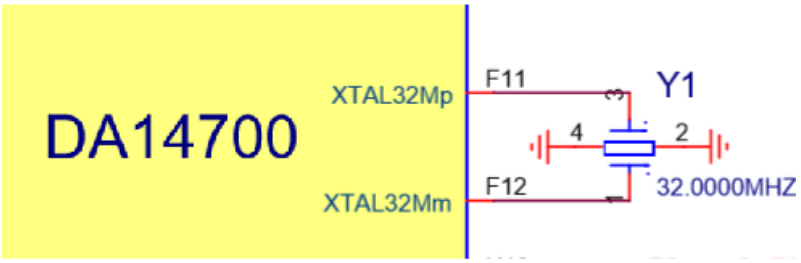


Figure 9: Physical Connection of XTAL32M

Example of crystal which meets specification is presented on Table 6.

Table 6: 32MHz Crystal Example and Characteristics

Reference Designator	Value
Part Number	XRCGB32M000F1H00R0
Frequency	32 MHz
Accuracy	±10 ppm
Load Capacitance (C_L)	6 pF
Equivalent Series Resistance (ESR)	60 Ω
Drive Level (PD)	150 µW
Size L × W × H (mm)	2.0 × 1.6 × 0.65

The XTAL32M provides the main system clock and is also used for the radio and high-speed peripherals. It can be calibrated to increase its frequency accuracy and optimize its settling time. It is recommended to trim the crystal, since this maximizes system radio performance and power efficiency. Moreover, it allows more design flexibility as crystals with a looser frequency tolerance specification can be used.

The trim operation consists of two parts: oscillator frequency adjustment and startup parameter adjustment. All trim settings are contained in XTAL32M_TRIM_REG (0x50050408). The value of this register can be stored in the configuration script area of the OTP memory. The booter or the application can then retrieve the value on cold boot and system wakeup from sleep.

The DA1470x SoC contains a bank of internal capacitors that can be used to compensate for parasitic capacitance of the IC package and PCB traces, as well as variance in the crystal parameters. Adjusting the value of the XTAL32M_TRIM field of XTAL32M_TRIM_REG sets the oscillator frequency.

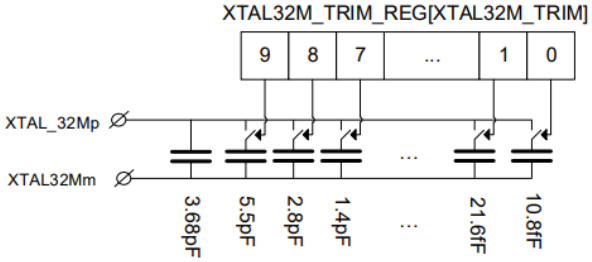


Figure 10: XTAL32M Trim Register

Frequency trimming can be done manually or automatically using the SDK's system test firmware (st_fw). In both cases an external instrument is required. In the first case a frequency counter or BLE tester can be used to verify frequency accuracy. In the second case, an instrument that generates precise 300 ms reference pulse (waveform generator).

Startup time can be optimized using a different st_fw command. A routine uses the SoC's internal ADC to measure the crystal shunt capacitance (C_0) and sets the proper values to the XTAL32M_CUR_SET, XTAL32M_AMPL_SET, XTAL32M_CMP_LVL, XTAL32M_BOOST_TRIM fields of XTAL32M_TRIM_REG. No external equipment is needed for this operation.

4.4.2 32.768 kHz Clock

The DA1470x utilizes a low power, low frequency clock for extended and deep sleep modes. This can be achieved with either the XTAL32K oscillator (using an external 32.768 kHz crystal) or the internal RCX oscillator, which presents maximum frequency drift 500 ppm.

When the RCX oscillator is used, no external crystal is needed. Using an external 32.768 kHz crystal provides tighter timing due to a higher accuracy (±50 ppm) but requires additional board space and adds the cost of the crystal.

The XTAL32K cannot be trimmed. The crystal is connected to the pins XTAL32Kp and XTAL32Km. External load capacitors are not required for a crystal with a load capacitor of 6 pF or 7 pF. When applying a crystal which requires, for instance, 9 pF load capacitance, additional capacitors must be added, one at each XTAL32K pin to ground.

The external 32.768 kHz crystal must meet the recommended operating conditions of a 32.768 kHz crystal oscillator (Table 7).

Table 7: XTAL32K Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
$f_{CLK\_EXT\_32K}$	external clock frequency	at pin 32KXTAL1/P0_3 in GPIO mode	10		100	kHz
f_{XTAL_32K}	crystal oscillator frequency		30	32.768	35	kHz
ESR	equivalent series resistance				100	kΩ
C_L	load capacitance	No external capacitors are required for a 6 pF or 7 pF crystal	6	7	9	pF
C_0	shunt capacitance			1	2	pF
Δf_{XTAL_32K}	crystal frequency tolerance (including aging)	Timing accuracy is dominated by crystal accuracy. A much smaller value is preferred.	-250		+250	ppm
$P_{DRV\_MAX\_32\ K}$	Maximum driver power	Note 1	0.1			µW

Note 1 Select a crystal that can handle a drive level of at least this specification.

Table 8 presents an example of a 32.768 kHz crystal which meets the specification described above.

Table 8: 32.768 kHz Crystal Example and Characteristics

Reference Designator	Value
Part Number	ABS07-32.768KHZ-7-T
Frequency	32.768 kHz
Accuracy	±20 ppm

Reference Designator	Value
Load Capacitance (CL)	7 pF
Shunt Capacitance (C0)	0.9 to 1.2 pF
Equivalent Series Resistance (ESR)	70 kΩ max
Drive Level (PD)	< 0.5 µW
Size L × W × H (mm)	3.2 × 1.5 × 0.9

4.4.3 Generating a Clock Output from DA1470x

The DA1470x SoC can output the internal clock signals at specific pins, please see Table 9. Enabling of the specific clock outputs is done through GPIO_CLK_SEL_REG register. The Clocks signals are avaialble in sleep mode, if they are enabled. For example, 32 kHz can be provided from pin P0_31 in active or sleep mode.

Table 9: Internal Clock Outputs

GPIO	Clock Outputs
P0_09	XTAL32M
P0_20	DIVN
P0_31	XTAL32K
P1_22	RCX
P1_23	RCLP

4.5 XIP QSPI Flash Memory

The DA1470x family uses an external low power NOR QSPI FLASH which is used to directly execute code (using the CPU cache). This is known as execute in Place (XIP).

For DA1470x a QSPI FLASH is used for XIP. This is driven the QSPI controller and uses dedicated pins which are supplied from V18F.

As already mentioned, flash is supplied from V18F. Power consumption of the flash must not exceed 30 mAs.

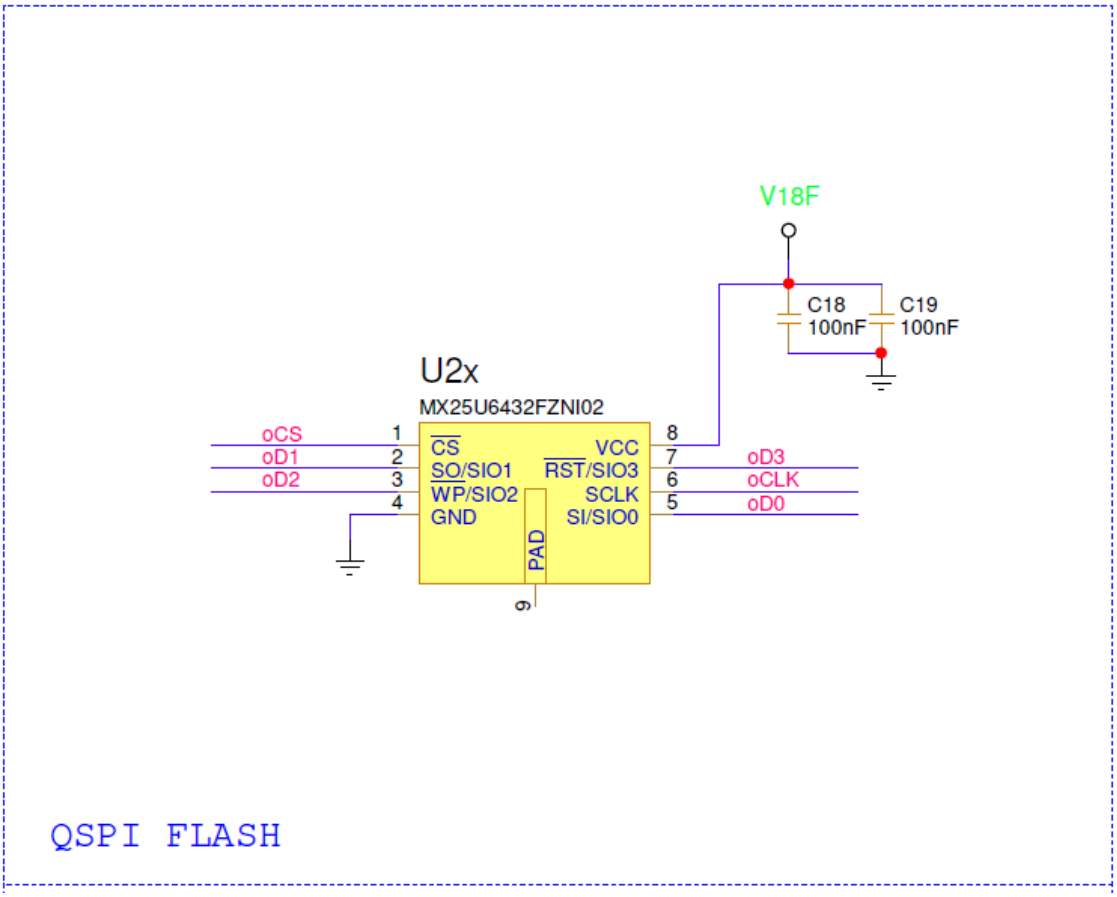


Figure 11: MX25U6432FZNI02 QSPI FLASH Schematic

As an example, in the DA1470x development kit the 64 Mbit QSPI XIP flash memory used is the MX25U6432FZNI02 from Macronix.

During read the operating current may reach the 80 mA level for beyond the V18F current capability of 30 mA. In order to ensure that the QSPI flash is properly supplied with sufficient current when operating at 96 MHz a short circuit is in place (on the DA1470x side) connecting together the two 1.8 V domains V18P and V18F.

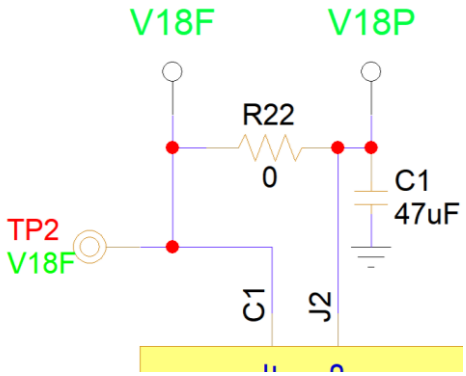


Figure 12: V18P & V18F Connection

To avoid signal integrity issues, keep the distance between the processor and the QSPI FLASH memory as short as possible, try to have the length of the traces as equal as possible, and route with enough spacing to avoid crosstalk.

If needed, apply 47 Ω to 56 Ω series resistors in all lines. The 10 K pull-up resistor on chip select pin of the memory is not mandatory.

4.6 QSPI Flash – Storage

There are two more QSPI controllers in DA1470x, QSPIC and QSPIC2. QSPIC is used for QSPI flash and QSPIC2 is used for QSPI RAM.

The QPSI Flash is for storing purposes, not for executing software. Dedicated 1.8 V GPIOs are used.

Maximum operating frequency is 96 MHz.

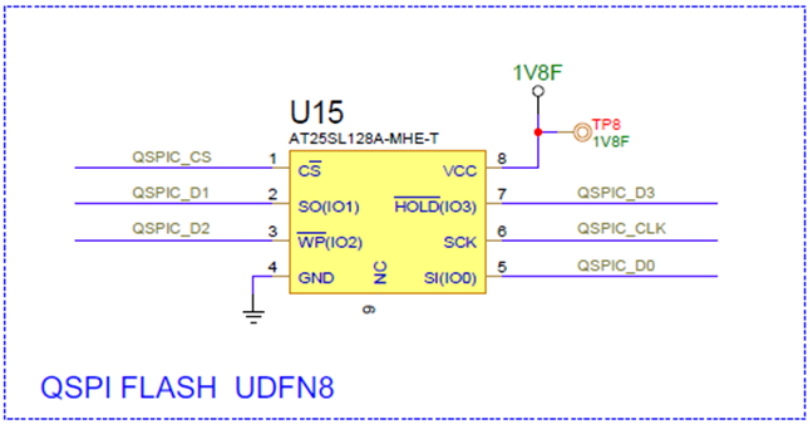


Figure 13: Example of QSPI Flash AT25SL128A-MHE-T used in the DA1470x Development Kit

Please follow the PCB design rules described on the XIP QSPI Flash section.

The following GPIO assignment is impended in the DA1470x development kit:

Table 10: DA1470x QSPI Flash GPIOs

QSPI Flash Memory Signal	Corresponded GPIO
QSPIC_D0	P1_09
QSPIC_D1	P1_27
QSPIC_D2	P1_18
QSPIC_D3	P1_17
QSPIC_CS	P1_25
QSPIC_CLK	P1_26

Please note that all QSPIC GPIOs can have their slew rate and driving strength fully configured.

4.7 QSPI RAM Memory

The QSPIC2 is available in all DA1470x except DA14705 and is used for QSPI RAM memory devices. Dedicated 1.8 V pins are used for the connection.

Please note that these pins can be configured as either QSPI RAM signals or GPIOs and can be used at 1.8 V only. These pins cannot be used at 3.0 V.

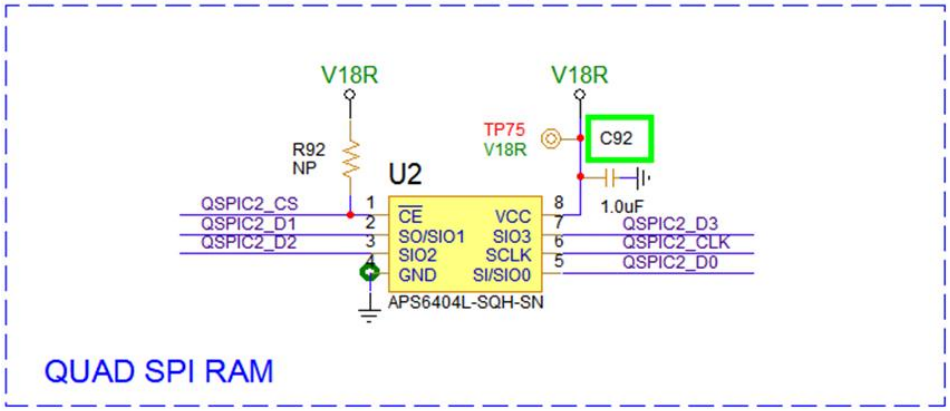


Figure 14: QSPI RAM Example APS6404L-SQH-SN used in DA1470x Development Kit

QSPI-RAM may be used in applications where we need bulk data transfers with DMA. The most common case is as LCD frame buffer. On DA1470x development kit the APS6404L-SQH-SN from APMEMORY is used.

The following GPIO assignment is impended in the DA1470x development kit:

Table 11: DA1470x QSPI RAM GPIOs

QSPI RAM memory signal	Corresponded GPIO
QSPIC2_D0	P1_15
QSPIC2_D1	P1_14
QSPIC2_D2	P1_13
QSPIC2_D3	P1_20
QSPIC2_CS	P1_24
QSPIC2_CLK	P1_19

Please note that all QSPIC2 GPIOs can have their slew rate and driving strength fully configured.

Please follow the PCB design rules described on the XIP QSPI Flash section.

4.8 PCB Layout

The PCB layout of the DA1470x Soc is defined from chip's package. Due to the fine pitch and the number of pins, HDI design must be applied. The number of layers is dependent to the number of the signals which must be routed from the chip.

4.8.1 PCB Footprint

The VFBGA142 package has a pin-to-pin pitch of 450 µm with ball diameter equal to 250 µm. The copper pad diameter used on DA1470x DK Pro is 0.200 mm. As the ball diameter is 0.250 mm, the size of the copper pad is sufficient for proper soldering of the chip in a Non-Mask-defined pad configuration.

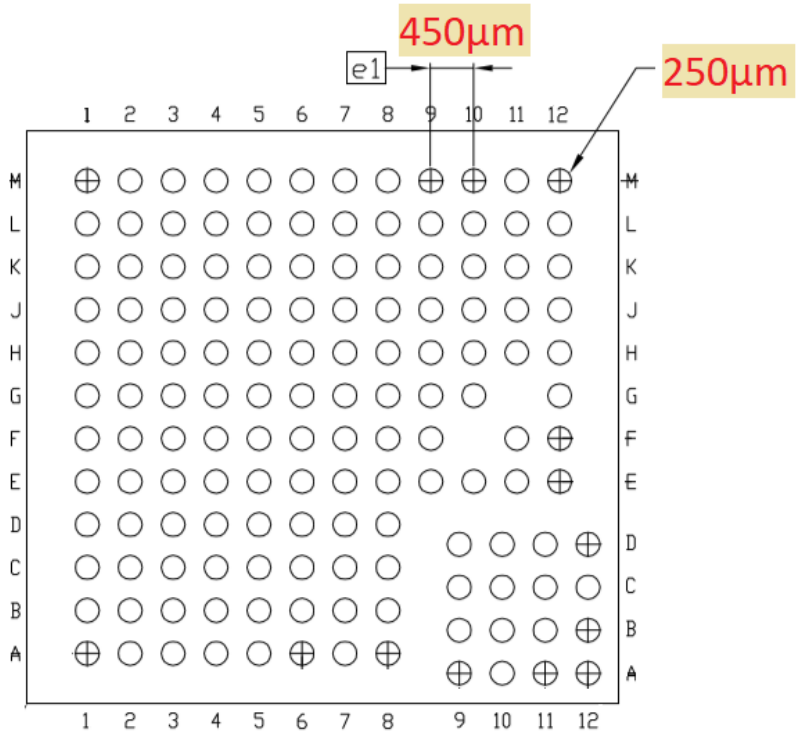


Figure 15: Bottom View of Packages VFBGA144

4.8.2 Microvias or PTH Vias

Microvias, and especially microvias on chip pads, make board design easier because of their small size. Copper filled vias offer low DC resistance. The thickness of the dielectric layer depends on the microvias aspect ratio (hole diameter to microvias depth), which is determined by PCB manufacturers' capability. For example, for an aspect ratio of 1:0.8, if the drill diameter of a microvia is 100 µm, the dielectric layer cannot be thicker than 80 µm.

The cost of producing a PCB with microvias is higher than producing a PCB with PTH vias. For copper filled vias, cost and production time are significantly higher.

4.8.3 Generic PCB Layout Guidelines

Generic guidelines for the DA1470x PCB layout are:

- Active components operating at high frequency should have layouts as compact as possible to prevent the cross-coupling between lines and to minimize the parasitic effects which has negative impacts on the operating parameters
- Always provide a solid grounding to the radio IC. Use as many vias as possible to create a solid GND under the IC itself and connect the IC to inner and bottom GND layers
- Remove GND under the pads of high speed and fast switching power components, such as QSPI data flash and crystals

The layout and PCB routing considerations to fast switching memory components:

- XIP QSPI flash, QSPI flash and QSPI RAM are considered fast switching components
- Place fast switching memory components, prioritizing QSPI XIP flash, as close as possible to the chip
- Add decoupling capacitor next to power pin
- Route traces with equal length if possible
- Have solid ground under traces
- Ensure the safe distance between traces to avoid crosstalk

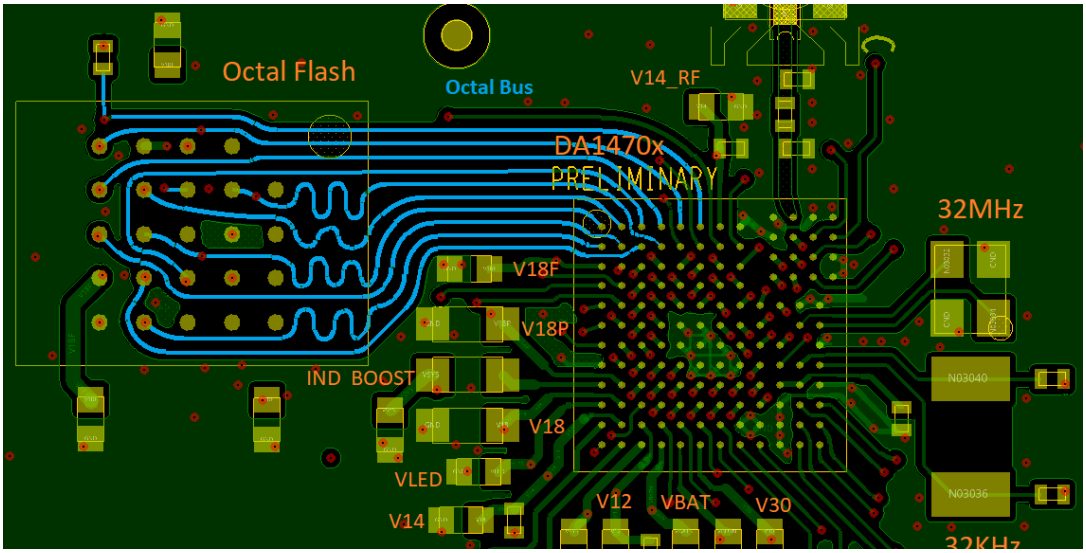


Figure 16: Example of Octal Flash Routing

The layout and PCB routing considerations for RF layout is:

- It is important to properly route the RF strip line to the antenna. The design of RF GND is also important

The layout and PCB routing considerations for XTAL are:

- Place the XTAL32M as close as possible to the IC to minimize additional capacitive load on the input pins and to reduce the chance of crosstalk and interference with other signals on the board
- Remove GND area under XTAL pads (Figure 17)
- If possible, try to create a ground shield around the crystals. XTAL32M ground is connected to the XTAL32M GND balls (Figure 18)

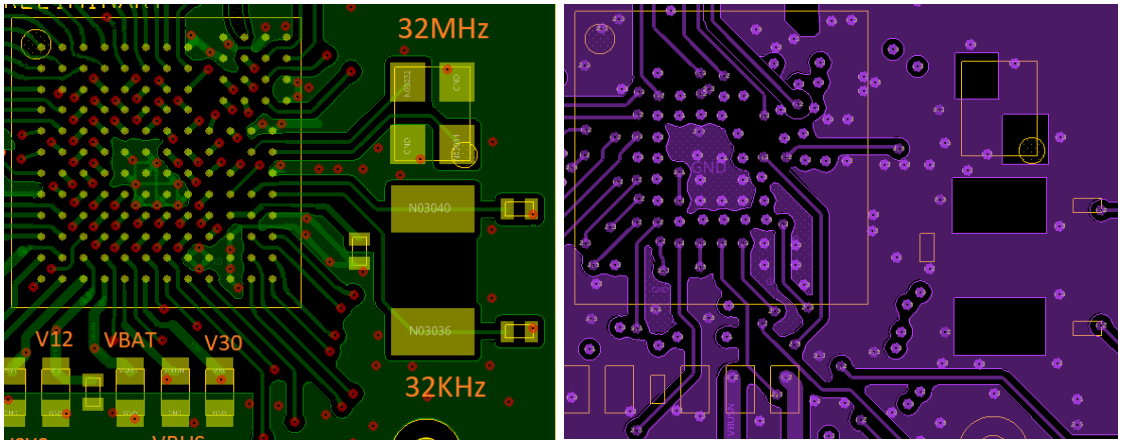


Figure 17: Remove Copper on Internal Layer (Right) under XTAL

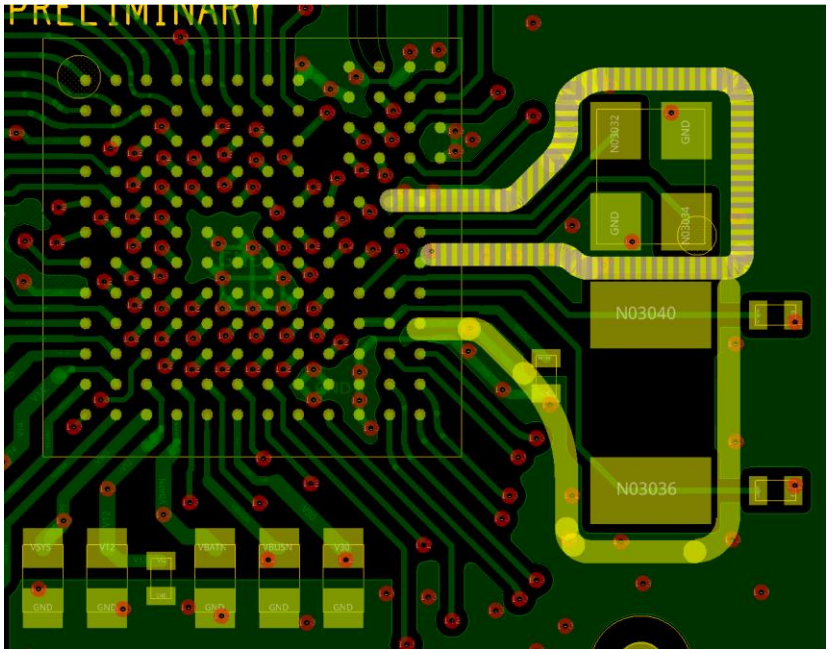


Figure 18: XTAL Grounding

4.8.4 PCB Layout

HDI structure need to be applied for ensuring all signals fan out. With the below PCB design rules design can be completed in 8Layers:

- 8-Layers
- 2-4b-2 (2 level µvia + buried via)
- Stacked µvias, µvias 250 µm/100 µm
- Mechanical drill, 450 µm/200 µm
- Min trace width 90 µm
- Min trace clearance 80 µm

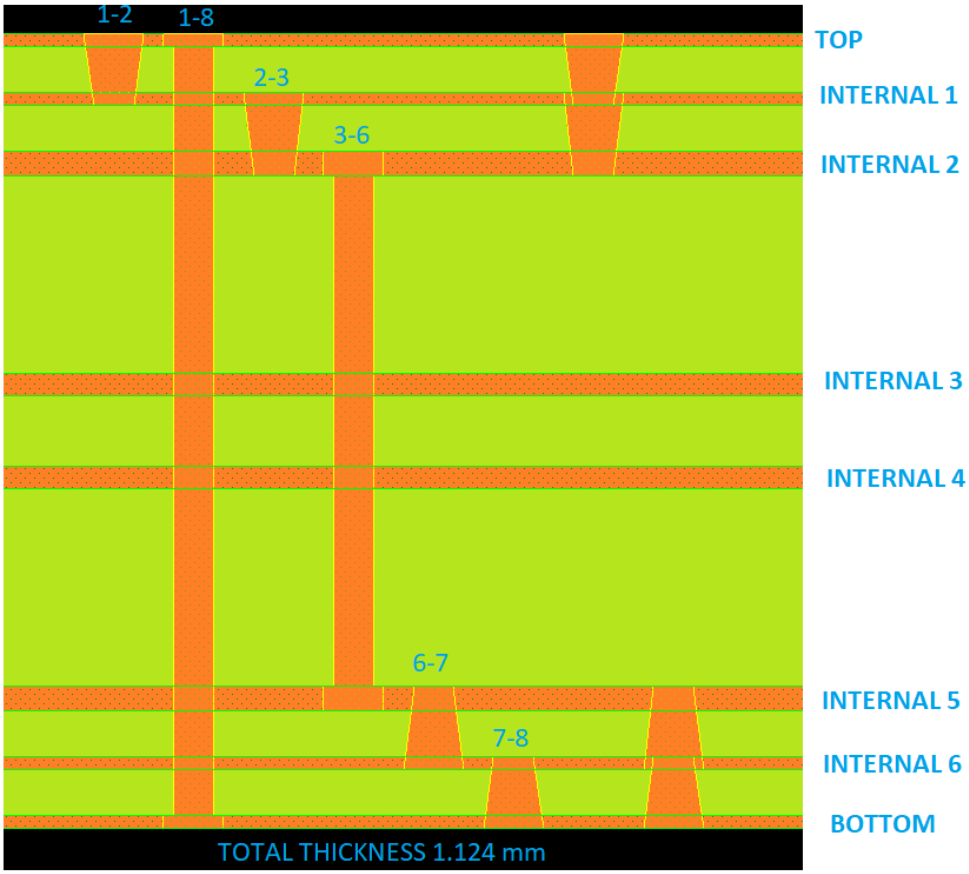


Figure 19: The HDI Structure of 8 Layers

The PCB layout example below is based on the DA1470x PRO-Daughterboard. Except the SoC, the power components, crystals, RF parts and XIP Flash Memory are included. Please notice that all GPIOs are routed out on the 3 top layers. Layer “Internal 3” is used for reference ground.

RF stripline impedance is calculated with reference the Internal 1 layer.

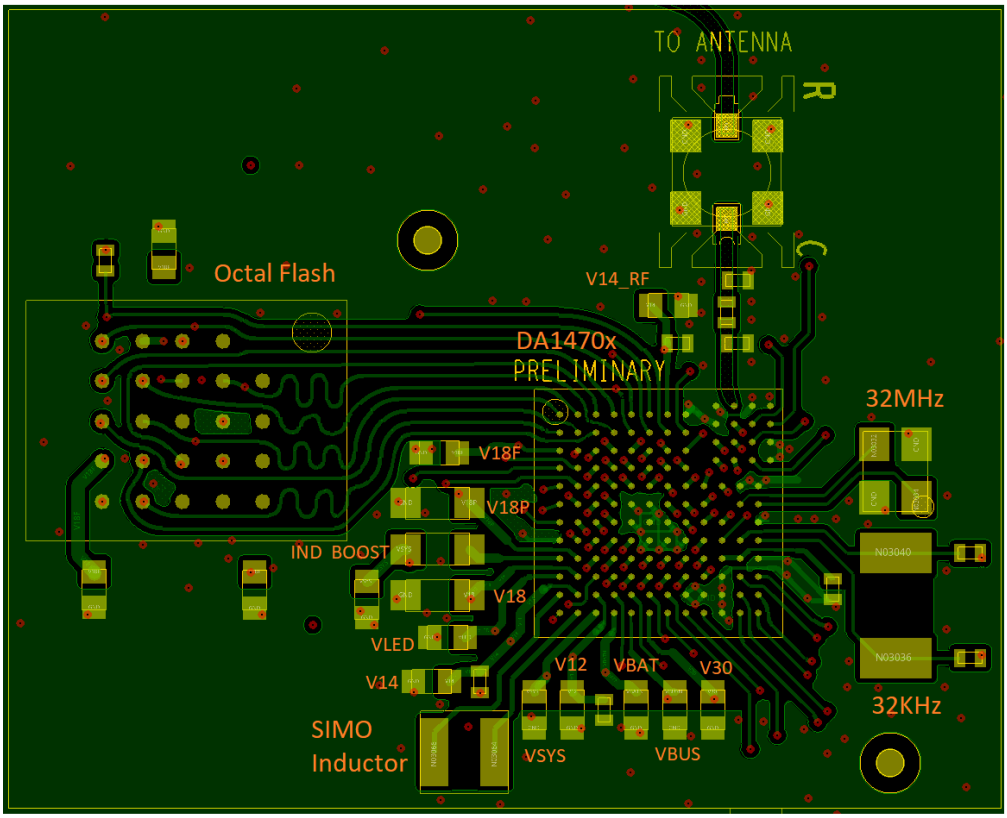


Figure 20: Top Layer and Components Placement

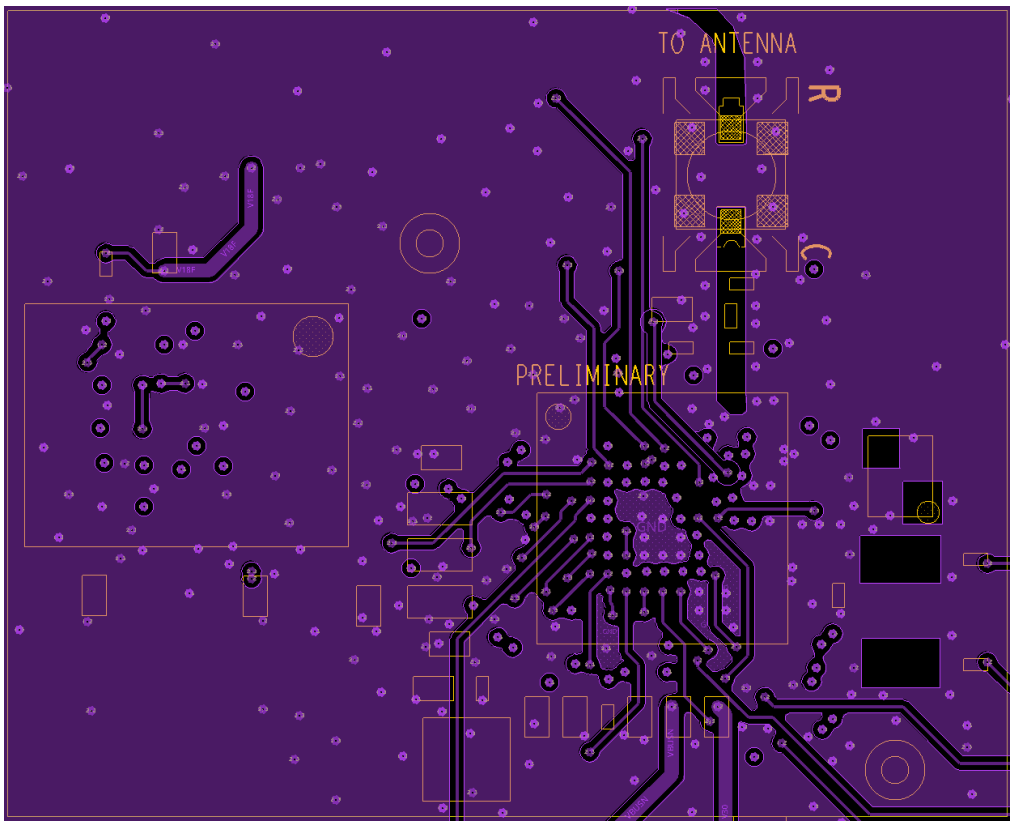


Figure 21: Internal 1 Layer Overlayered with Components on Top

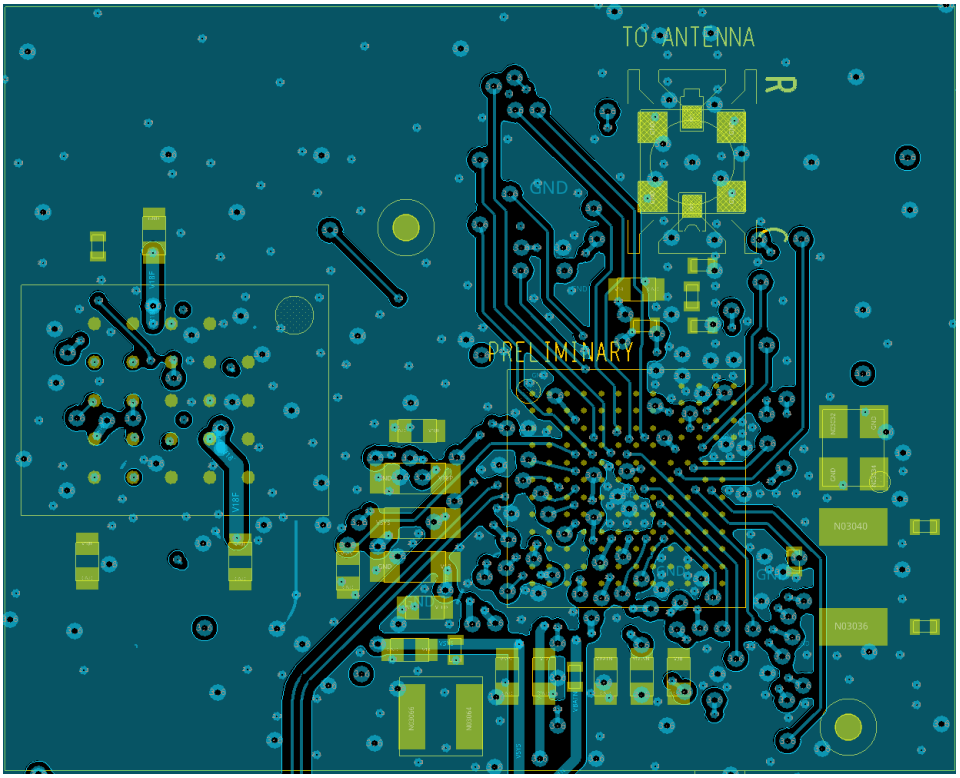


Figure 22: Internal 2 Layer Overlayered with Components on Top

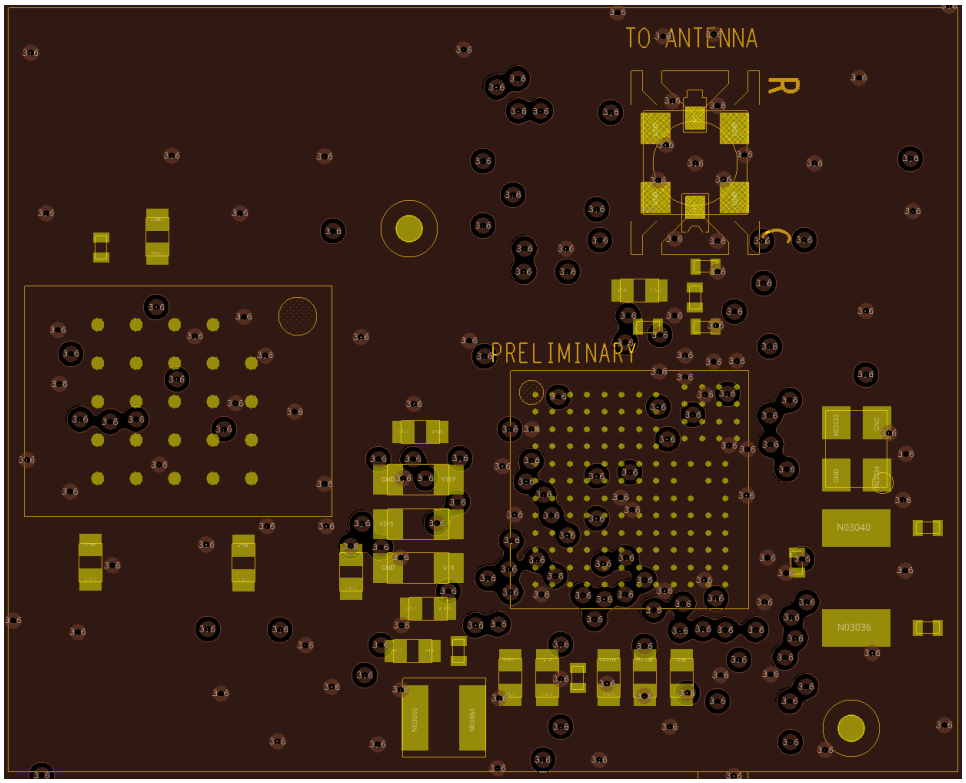


Figure 23: Internal 3 Layer (Reference GND) Overlayered with Components on Top

Revision History

Revision	Date	Description
1.0	21-Jun-2022	First Release

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
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