

Introduction

This is a collection of guidelines for the design of a data acquisition system. Its purpose is to supplement the more methodical block-by-block discussions available in numerous other papers and application notes. Emphasis in this note is on the less easily quantifiable happenings "between the blocks," rather than a description of the block components and their error contributions. This latter information may be found in the Bibliography under "General."

A data acquisition system is defined to include all the components needed to generate the electrical analogs of various physical variables, transmit these signals to a central location and digitize the information for entry into a digital computer. Among these components are transducers, amplifiers, filters, multiplexers, sample/holds and analog-to-digital converters. The system also includes all signal paths tying these functions together.

Several system architectures will be considered, followed by a general discussion aimed at the designer who must choose hardware for a given application.

Topics include:

- Data Acquisition System Architecture
- Signal Conditioning
- Transducers
- Single-Ended vs. Differential Signal Paths
- Low-Level Signals
- Filters
- Programmable Gain Amplifier
- Sampling Rate
- Computer Interface

Data Acquisition System Architecture

At present the most widely used DAS configuration is that shown in Figure 1. It handles a moderate number of analog channels, feeding into a common multiplexer, programmable gain amplifier (if required) track/hold amplifier and A-D converter.

A more specialized and expensive variation is to place a Track/Hold in each channel as shown in Figure 2. Switching all channels to HOLD simultaneously produces a "snapshot" view which preserves the phase relation of signals in all channels. This information is important in seismic studies and vibration analyses.

The DAS system of Figure 3 offers many advantages, but is not yet practical except for slowly changing channel data. Low frequency signals allow dedication of a slow but accurate integrating type A-D converter for each channel. The channel filters, often included to reduce aliasing errors and noise, are not necessary, since aliasing is not a problem with low bandwidth signals. The integrating converter suppresses wideband noise by averaging it about the instantaneous signal level. Also, the converter's integration period may be chosen to provide almost complete rejection of a specific interference frequency such as 60 Hz. Digital outputs from the converters are then digitally multiplexed.

The system shown in Figure 3 has an inherent advantage over the other two systems, having eliminated both the track/hold and the analog multiplexer with their many error contributions. The disadvantage, of course, is cost. Figure 3 would become the system of choice in many more applications, if a significant reduction should occur in the price of successive - approximation A-D converters.

A small RAM may be added at the converter's output in any of these systems, to buffer the computer and offload its involvement with individual conversions. Timing and control may be arranged to scan all channels repeatedly, and continuously update a RAM location for each channel. The computer is then free to look at a recent reading for any channel, at any time.

Further discussion will center on Figure 1, both in the single-ended version shown, and in the differential version.

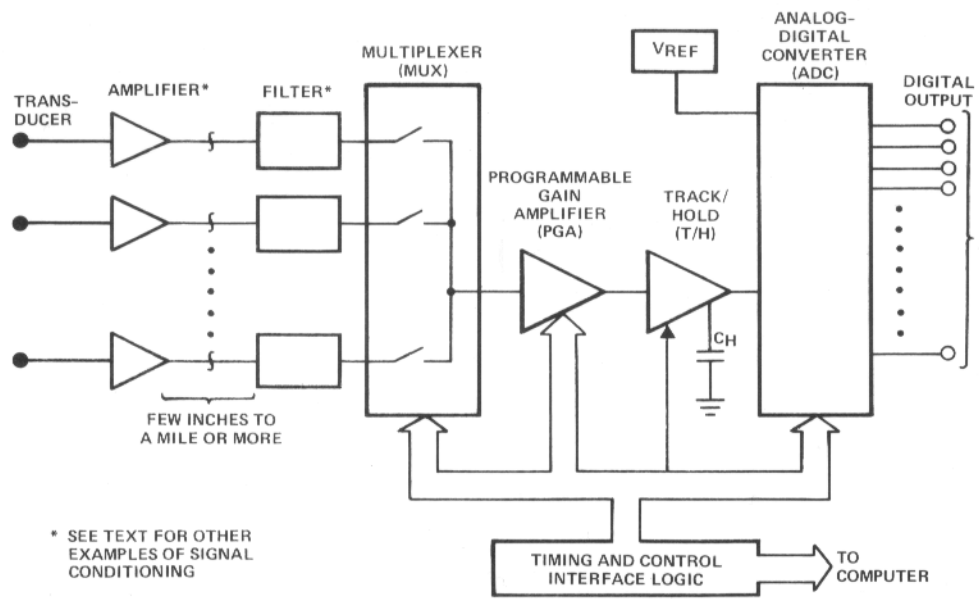


FIGURE 1. TYPICAL DATA ACQUISITION SYSTEM

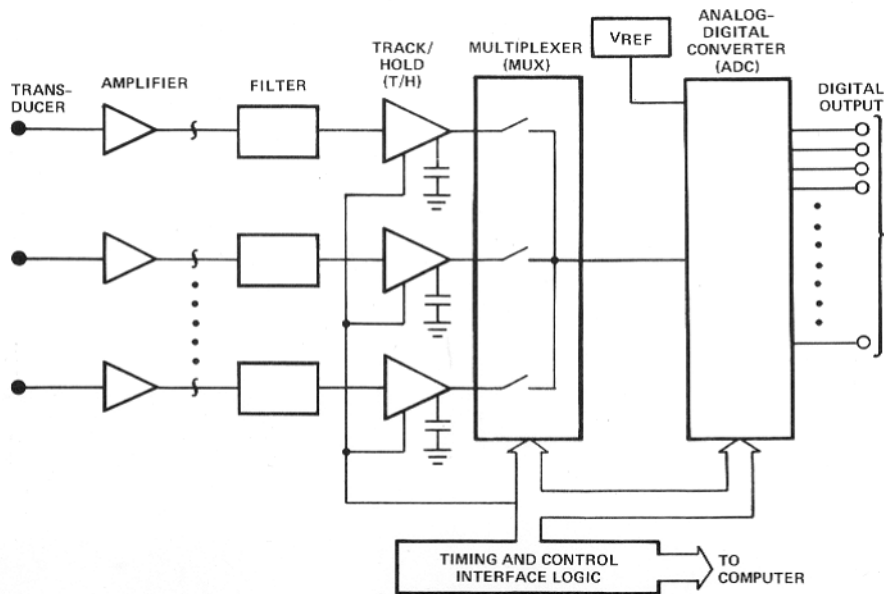


FIGURE 2. DAS SYSTEM FOR SIMULTANEOUS SAMPLING OF ALL CHANNELS

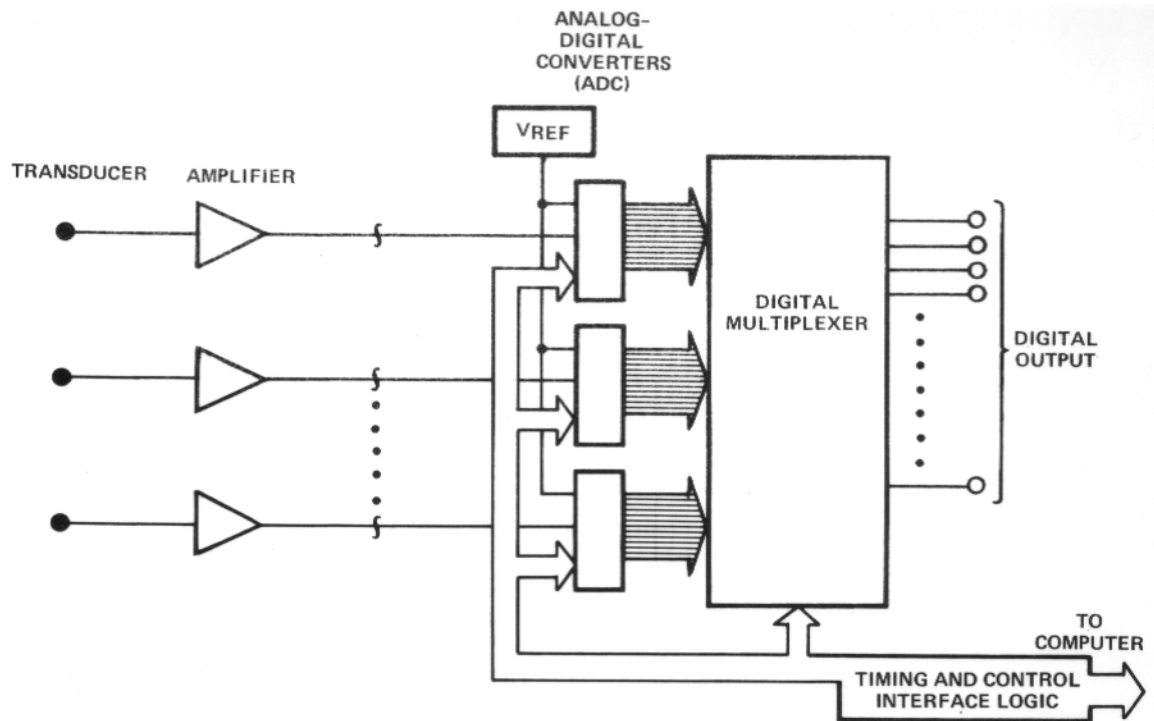


FIGURE 3. HIGH ACCURACY, MULTI-CONVERTER DAS SYSTEM

Signal Conditioning

Signal conditioning refers to all the operations performed on a transducer signal up to (and including) digitization by the A-D converter. Standard among these operations are multiplexing, programmable gain, and Track/Hold. Others may be added as required:

- Transducer excitation
- Amplification
- Filtering
- Calibration
- Linearization
- Voltage to Current Conversion (4 to 20mA; 10 to 50mA)
- RMS to DC Conversion
- Logarithmic Signal Compression
- Common Mode Rejection

For highest signal-to-noise ratio all signal conditioning should be performed near the transducer, with the exception of common mode rejection and filtering. Filters should be located near the multiplexer input. Besides minimizing alias errors originating in the high end of the transducer's output spectrum, filters suppress wideband noise picked up on signal lines to the transducer.

Transducers

The first item in the signal path of a DAS is the transducer. This device usually transforms energy from one form to another, producing an electrical analog of the physical variables to be monitored or measured. Transducers are based on a variety of physical principles but most produce a voltage as output. Some yield an intermediate variable such as resistance or capacitance, which is transformed to voltage by an applied electrical excitation (carrier frequency, DC voltage, current source).

Often, several types of transducers are available to sense a given quantity. When selecting a voltage output transducer, remember that a low source resistance is desirable, both to minimize noise and to reduce loading by the next "block" in the signal path. Provision on the transducer for a convenient method of signal calibration will be welcome, once a system is in operation. Also, a center tap on the transducer allows better interface to a balanced line if low level signals are to be transmitted.

Several questions arise at this point:

- Should the signal path be single-ended or differential?
- Should the signal be transmitted at low level (100mV) or high level?
- What type of conductor should be used for signal transmission?

Answers to these and other questions are covered in the following sections.

Single-Ended vs. Differential Signal Paths

Consider the transducer output. A high level signal (100mV to 10V) is easier to handle than low level. Is a common mode signal present? If not, is it likely to be acquired as “pickup” during transmission? This is likely if the cable is routed near fluorescent lights, motors or other electrical machinery. If common mode voltage is not expected, then an economical single-ended connection is possible, with a single wire per channel and a common return (see Figure 4). High level signals, short distance and controlled conditions will ensure good performance with this arrangement.

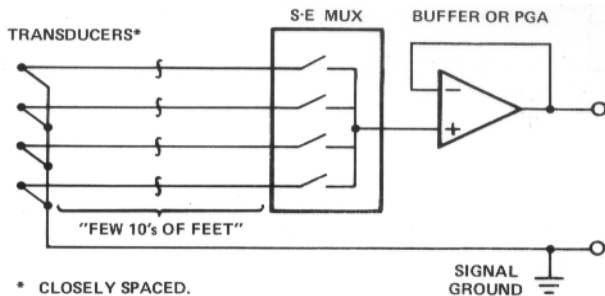


FIGURE 4. SINGLE-ENDED DATA PATHS

Low level signals require special treatment. Whether high or low level, the presence of common mode voltage calls for a differential signal path. The most widely used solution is an unshielded, twisted pair of wires, good for 1000 feet or so with a bandwidth of 100kHz. As a minimum then, two wires per channel feed into a differential amplifier or multiplexer, buffered by a full or pseudo-differential amplifier to reject the unwanted common mode voltage (see Figure 5).

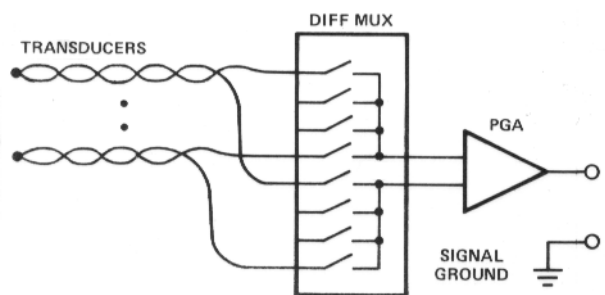


FIGURE 5. DIFFERENTIAL DATA PATHS

For the case in which the transducer output is a low level voltage, the choice is whether to transmit it as is, or to boost the level by adding an amplifier. The amplifier provides low source impedance as well as gain; two valuable forms of signal conditioning. However, providing power to a remote amplifier can be difficult. Even if a supply is available at the remote site, the voltage between two widely separated commons presents a problem. If the sum of signal plus common mode voltage does not exceed the input range of either the multiplexer or buffer amplifier, Figure 5 can be used.

A more expensive approach is required for higher common mode voltages. One reliable technique is the “flying capacitor” multiplexer of Figure 6, using reed relay switches. This works well for thermocouples bonded to machinery and riding on hundreds of volts relative to DAS ground, but in some applications the reed relay’s 1ms response time can be a limitation.

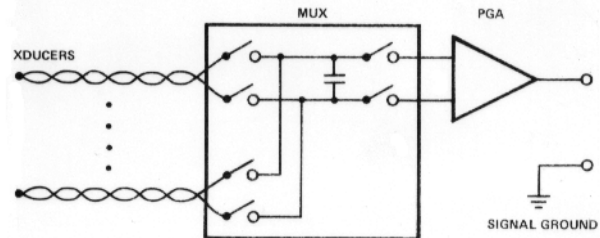


FIGURE 6. “FLYING CAPACITOR” MULTIPLEXER USING REED RELAY SWITCHES FOR HIGH CMV SIGNALS

Isolation amplifiers can handle higher voltages and higher bandwidths than the system of Figure 6. For example, magnetically isolated amplifiers are rated at 2kV and up, with a small signal bandwidth of approximately 2kHz. One of these per channel is expensive, but in addition to common mode rejection it can solve the problem of supplying power at the remote transducer. Isolation amplifier models are available which include $\pm 15V$ terminals, referenced to the floating front-end of the amplifier. This power can provide transducer excitation and supply an amplifier or other signal conditioning circuitry.

For higher bandwidth data, optically isolated amplifiers are available with $f_{-3dB} = 15kHz$ and 2kV isolation. These amplifiers do not provide the external supply terminals to power transducer circuitry.

Low Level Signals

The main concern with signals below 100mV is that noise, offset voltage, and other aberrations can represent a large percentage error. A shielded, differential signal path is essential for transmitting these signals, especially to maintain a noise level below $50\mu V_{RMS}$.

Most transducer outputs are low level and low bandwidth as well. Since shielding precautions to be described are intended to produce an acceptable signal to noise ratio, filters may not be necessary. Otherwise, active filters with their relatively large DC errors should not be used for low level signals. Passive filters on the other hand, are restricted to two- or three-poles as a practical limit, which in turn restricts the allowable signal bandwidth for a given accuracy (see the section titled *Filters*).

The transmission cable carrying the transducer signal is critical in a low level system. It should be as short as practical and rigidly supported. Signal conductors should be tightly twisted for minimum enclosed area, to guard against pickup of electromagnetic interference, and the twisted pair should be

shielded against capacitively coupled (electrostatic) interference. A braided wire shield may be satisfactory, but a lapped foil shield is better since it allows only one tenth as much leakage capacitance to ground per foot.

A key requirement for the transmission cable is that it present a balanced line to sources of noise interference. This means an equal series impedance in each conductor plus an equally distributed impedance from each conductor to ground. The result should be signals equal in magnitude but opposite in phase at any transverse plane. Noise will be coupled in-phase to both conductors and rejected as common mode voltage. Again, any such noise will be directly proportional to the source impedance driving the line. An isolation or instrumentation amplifier may be used to terminate the line, providing high input impedance, common-mode rejection, conversion from a differential to single-ended signal path, and a buffer for the ON resistance of the following multiplexer.

Coaxial cable is not suitable for low-level signals because the two conductors (center and shield) are unbalanced. Also, ground loops are produced if the shield is grounded at both ends by standard BNC connectors. If coax must be used, carry the signal on the center conductors of two equal-length cables whose shields are terminated only at the transducer end. As a general rule, terminate (ground) the shield at one end only, preferably at the end with greatest noise interference. This is usually the transducer end for both high and low level signals.

Printed circuit traces and short lengths of wire can add substantial error to a signal even after it has traveled hundreds of feet and arrived on a circuit board. Here, the small voltage drops due to current flow through connections of a few mΩ must be considered, especially to meet an accuracy requirement of 12-bits or more.

Table 1 shows a useful collection of data for calculating the effect of these short connections. Proximity to a ground plane will lower the values for inductance.

WIRE GAGE	EQUIVALENT WIDTH OF P.C. CONDUCTOR (2 OZ. Cu.)	DC RESISTANCE PER FOOT	INDUCTANCE PER FOOT	IMPEDANCE PER FOOT	
				AT 60Hz	AT 10kHz
18	0.47"	0.0064Ω	0.36μH	0.0064Ω	0.0235Ω
20	0.30"	0.0102Ω	0.37μH	0.0102Ω	0.0254Ω
22	0.19"	0.0161Ω	0.38μH	0.0161Ω	0.0288Ω
24	0.12"	0.0257Ω	0.40μH	0.0257Ω	0.0345Ω
26	0.075"	0.041Ω	0.42μH	0.041Ω	0.0488Ω
28	0.047"	0.066Ω	0.45μH	0.066Ω	0.0718Ω
30	0.029"	0.105Ω	0.49μH	0.105Ω	0.110Ω
32	0.018"	0.168Ω	0.53μH	0.168Ω	0.171Ω

TABLE 1. IMPEDANCE OF ELECTRICAL CONNECTIONS, +20°C

As an example, suppose the ADC in Figure 1 has 12-bit resolution, and the system accuracy is to be $\pm 1/2$ LSB ($\pm 1.2\text{mV}$). The interface logic might draw 100mA from the +5V supply. Flowing through six inches of #24 wire, this current

produces a drop of 1.28mV; more than the entire error budget. Obviously, this digital current must not be routed through any portion of the analog ground return network.

Filters

The presampling or anti-aliasing filters shown in Figure 1 are normally required with high-level signals of significant bandwidth, especially if the signal is to be reconstructed by a digital-to-analog converter after processing. If low level signals require a passive filter, the differential configuration of Figure 7 preserves some degree of impedance balance on the line.

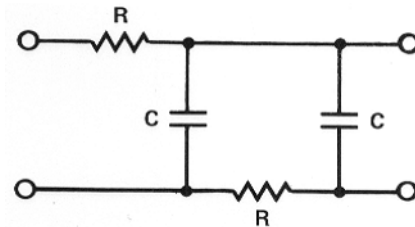


FIGURE 7. A PASSIVE, TWO-POLE, LOW PASS, DIFFERENTIAL INPUT FILTER

A low pass Butterworth response is best for the channel bandlimiting filter in most data acquisition systems. The Butterworth filter output decreases monotonically with frequency, though this attenuation is very slight within the passband. Other filter types produce ripple in the passband, whose amplitude degrades accuracy unless expensive, high tolerance components are used.

Butterworth is not the most linear phase response, and if signal group delay is critical an elliptic (Bessel) filter should be chosen. Again, however, Butterworth fits most applications. A given number of poles may be had by cascading the two- and three-pole sections shown in Figure 8. Either reference under "Filters" in the Bibliography gives a systematic procedure for calculating R and C values in terms of a given cutoff frequency. See the Section on "Sampling Rate" for the poles versus accuracy requirement.

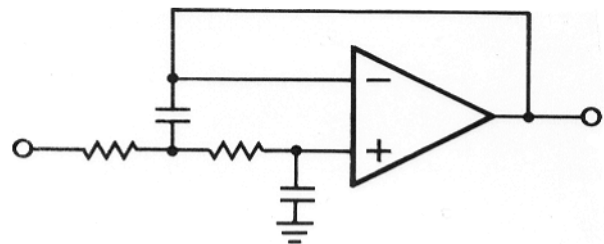


FIGURE 8A. TWO-POLE BUTTERWORTH LOW-PASS FILTER

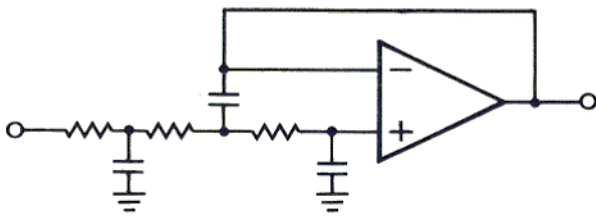


FIGURE 8B. THREE-POLE BUTTERWORTH LOW-PASS FILTER

Programmable Gain Amplifier (PGA)

Unless the ratio of highest to lowest signals anticipated on any channel is ≤ 2 , some form of programmable gain amplification is desirable between the multiplexer and A-D converter. Without this variable gain block, the MSB's are idled one after another as input level decreases. Although the resolution of an n-bit converter remains a constant $FS/2^n$ by definition, resolution referred to the input level is decreasing ($FS = \text{Full Scale}$).

Considering resolution as referred to the input level, a 12-bit converter digitizes an input of $.06FS$ to only 8 bits. The full 12-bit resolution applies only for $V_{IN} \geq FS/2$. Therefore, to fully utilize the converter, gain should be added as necessary before each conversion, to meet the condition $FS/2 \leq V_{IN} \leq FS$. Then the amount of gain introduced by the PGA is noted by the computer to keep track of the actual input value.

Three other services are performed by the PGA:

1. Buffering: Prevents a loading effect due to the multiplexer's ON resistance.
2. Differential to Single-Ended Conversion: Necessary for the majority of Track (or Sample)/Holds and A-D converters.
3. Common Mode Rejection (CMR): When connected to the output of a differential multiplexer, the PGA's differential input rejects the common mode voltage accumulated by a signal transmission cable. Figure 9 shows a subtractor or "pseudo-differential" PGA suitable for wideband signals with low common mode content. In this circuit, CMR is limited by precision of the "K" ratio and variations in the channel source impedance.

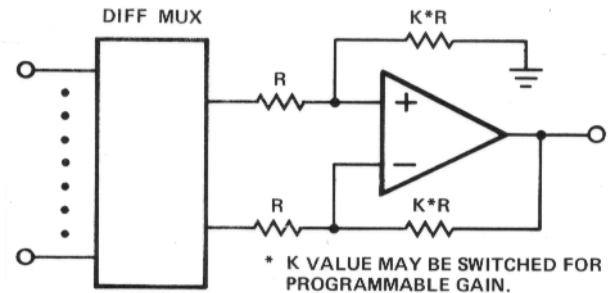


FIGURE 9. SUBTRACTOR OR PSEUDO-DIFFERENTIAL PGA

Figure 10 is the full differential PGA, necessary for low-level, high common mode signals. This version offers the highest gain accuracy and for high gain, the best CMR.

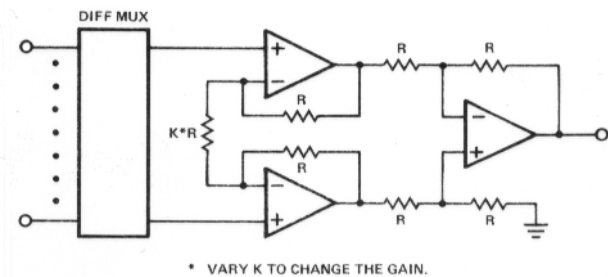


FIGURE 10. FULL DIFFERENTIAL PGA

The PGA normally precedes the Track/Hold, since the PGA would amplify any error introduced by that device. This order must be reversed to implement an auto-range capability, because the signal voltage must be held at the PGA input for the duration of an auto-range subroutine by the computer. Such an algorithm consists of:

- Set PGA gain
- Trigger a conversion
- Note Result
- Iterate until $(FS/2 \leq \text{Result} \leq FS)$

Sampling Rate

Throughput rate for a DAS may be defined as the maximum number of digital samples per second that it can produce without exceeding its specified limit for accuracy. The system may run at a lower speed to avoid generating redundant and useless data. If a waveform of significant bandwidth is to be reconstructed from the digital samples, then "the higher the better" is generally the rule for sampling rate.

The required rate is often higher than one would suppose. For example, using the criteria of data bandwidth alone, a very low sample rate is required for the slowly changing voltage outputs from a solar panel. Once per minute for each channel might be enough. With 60 channels though, the rate required is once per

second. In addition, one might require a maximum of one second for notice of failure on any channel, boosting the required sample rate to 60 samples per second. In this manner, low bandwidth channels may require a high speed DAS, according to the relationship:

$$\text{System Sample Rate} = (\text{Highest Channel Rate}) \times (\text{Number of Channels})$$

Also, a very high sample rate is required to preserve the high frequency content of a transient event on a single channel. The most commonly encountered requirement though, is a multichannel DAS (see Figure 1) with a modest bandwidth on each channel. For example, each data source might be an accelerometer with an output ranging through several hundred Hertz.

Notice that the low and high bandwidth signals just described cannot be handled efficiently with the same system. A sample rate high enough for the highest bandwidth channel will oversample the lower bandwidth channels, generating unnecessary data. High and low bandwidth data are best handled by separate multiplexer/ converter systems.

Presampling filters are essential to ensure accuracy in the sequence of digital samples representing a given channel. Since the multiplexer is a sampler (as is the Sample/Hold and A-D Converter) this means a separate filter dedicated to each channel preceding the multiplexer. A single filter following the multiplexer would do the job, but its modest response time would form a bottleneck restricting the sample rate. Guidelines are needed then, to relate a given level of accuracy to data bandwidth, filter cutoff frequency, and number of filter poles.

As mentioned earlier, a filter limits the error due to alias frequencies by restricting the bandwidth of both signal and noise. Either acting alone or in concert may cause error, since alias frequencies arise in several ways:

1. Overlap of the signal spectrum and the lower sideband associated with the sampling frequency f_s .
2. Overlap of the upper and lower sidebands associated with any two consecutive harmonics of f_s .
3. Overlap of any sideband with wideband noise from the data channel.

A band-reject filter would control case 1, but a low-pass type is needed to handle cases 2 and 3 as well. Again, the Butterworth response is preferred in most applications, but it does offer increasing phase shift and gain error for frequencies approaching the cutoff (-3dB) frequency. This cutoff should be set no higher than necessary for acceptable gain error in the highest signal components. A higher cutoff will only include unnecessary noise bandwidth.

Finally, for a given accuracy specification such as $\pm 1/2$ LSB, a tradeoff may be made between the sample rate and number of poles. These poles usually come from the filter, but the number may include any pole(s) inherent in the transducer, provided

they occur at an acceptable location relative to the cutoff frequency.

Figure 11 shows aliasing error, due to the signal spectrum alone, versus sampling rate for different numbers of poles. The horizontal axis is normalized to Sampling Frequency/Cutoff Frequency. Notice that a 2-pole filter requires a sampling frequency 30 times the filter cutoff frequency, just to obtain 1% accuracy. For $\pm 1/2$ LSB error in a 12-bit system ($\pm 0.01\%$), a 5-pole filter requires sampling at 11 times the cutoff frequency. Remember, Figure 11 applies only to the signal spectrum. Noise will cause some additional aliasing error.

Clearly, Nyquist's Sampling Theorem is not a practical guide for sampling rate in real applications. Actual (as opposed to hypothetical) filters cannot bandlimit a signal sufficiently to permit the theoretical minimum of two samples per cycle of highest signal frequency.

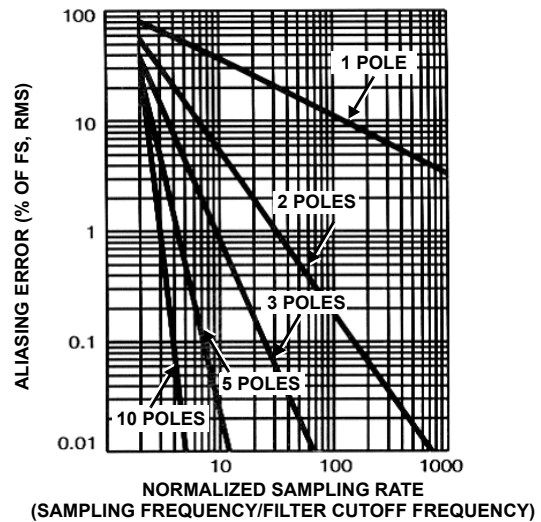


FIGURE 11. EFFECT OF FILTER POLES ON ALIASING ERROR

Computer Interface

The typical DAS we have described (Figure 1) requires several control signals:

- Multiplexer Channel Address
- PGA Gain Address
- Track/Hold Control
- A-D Converter
 - Start Convert
 - MSB Invert
 - Short Cycle
 - Unipolar/Bipolar
 - Output Byte Enable
 - Conversion Interrupt, etc.

This control can be provided directly by the computer, but some portion of these signals is usually supplied by an intermediate block of control logic. For monitoring predictable

channel data, the DAS can repeatedly scan through its channels, trigger the converter, and notify the computer when each data sample is ready. This independent operation can be accomplished by a clock and counter arrangement to supply channel and gain addresses, plus a dual "one shot" multivibrator (74123) to gate the Start Convert and Track/Hold functions.

To handle a sudden change in data level or other unexpected event, the computer must be able to randomly access any channel or PGA gain. Provision is made to write this information to the DAS via the computer's data or address bus, using appropriate address decoders and latches.

When processing higher bandwidth signals, one error source to be minimized is the Track/Hold's aperture delay uncertainty, or jitter. The logic which generates the T/H control signal needs close attention, since jitter in this waveform adds to that specified for the device itself.

Finally, the DAS output consists of a stream of digital words from the converter, synchronized with the converter's status signal indicating when the data is valid. Techniques for passing this data to the computer include direct memory access (DMA), memory mapping, and mapping via a dedicated I/O port, all with or without an external interrupt of the processor.

DMA is most efficient for the high speed transfer of large volumes of data. This can proceed by program request, resulting in the movement of a block of data to a designated sequence of memory locations, at a speed limited only by the memory cycle time. As an alternative, hardware can be configured to allow transfer of a data word during every non-memory machine cycle. This allows an almost continuous output of data from the DAS. The transfers are asynchronous and unsolicited by the program with only a slight increase in software execution time.

For less demanding data rates the choice is between an I/O or memory mapped interface. The former is best for small systems. For example, the 8085 microprocessor can control up to eight I/O devices without external address decoding. Addition of decoders expands the field from 8 to 256 peripherals.

There is a range of applications for which the choice of I/O or memory mapping is not clear, but memory mapping becomes attractive with increasing system complexity. The memory reference instructions available with this approach simplify programming and speed execution. A further increase in throughput is obtained by use of the processor's interrupt system, allowing the main program to proceed while an analog-to-digital conversion is in progress.

Memory mapping plus interrupt is very effective; however, the software overhead associated with service of an interrupt-driven I/O interface results in a diminishing advantage as the required throughput rate increases. Again, DMA offers the advantage of high data rates.

Bibliography

General

1. "Analog Data Book", Harris Corp. 1980
2. "Data Acquisition Handbook", Intersil, 1980
3. "Data Conversion Systems Digest", Analogic, 1978
4. "Integrated Circuit Converters, Data Acquisition Systems and Analog Signal Conditioning Components", Analog Devices, Inc. 1979
5. "Linear Applications Handbook", National Semiconductor, 1978

Grounds, Shielding and Power Distribution

6. "An IC Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change", Analog Devices Application Note, 1977
7. "Elimination of Noise in Low-Level Circuits", Gould Application Note
8. "Isolation and Instrumentation Amplifiers Designer's Guide", Analog Devices, 1978

Filters

9. "Electronic Filter Design Handbook", Arthur B. Williams, McGraw-Hill, 1981
10. "Need an Active Filter? Try These Design Aids", EDN, Nov. 5, 1978

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