Application Note

AN-501
Power-Up/Down Considerations in NOR Flash

Contents

1 Introduction

Flash memory devices are widely used components in microcontroller systems as regular companions to MCUs. Compared to MCUs, complex PMICs, and other SoCs, Flash memory is perceived to be a rather simple device. For example, a typical serial Flash device is commonly housed in an eight-pin package, contains two data pins (in and out), and communicates with the MCU over a simple four-wire SPI protocol. Such perceived simplicity, however, can be deceiving. Some important system design requirements specific to NOR Flash, such as proper power-up sequencing, can be overlooked. Under certain conditions, this can lead to unexpected and undesirable system operation.

The purpose of this document is to create awareness of the importance of proper system design with respect to an important element of correct NOR Flash memory operation: the correct power-up and power-down sequencing.

The importance of a correct power-up sequencing (often referred to as "VCC ramp") is described in more detail in Chapter 2.

Chapter 3 discusses hardware and software reset.

Even when a Flash device is powered up correctly, it can still be susceptible to varying voltage levels that can occur during device operation, such as a brown-out condition. The consequences of brown-out, recovering from it, and avoiding it are described in Chapter 4.

Power-down is discussed in Chapter 5.

Power cycling, as well as entering and exiting a variety of power saving modes represents its own challenges, which are discussed in Chapter 6.

The Appendix describes a variety of methods of executing a reset.

Additional information regarding VCC Power Off, Brownout, and Power-On with the DataFlash® Family can be found in Application Note ADAPP001A-DFLASH-5/13.

1.1 Target audience

This document provides both educational material on Flash memory principles of operations, as well as information on correct procedures and the correct interpretation of datasheet parameter values. The target audience for this document includes:

- Systems Engineers
- Applications Engineers
- FAEs
- Engineering Managers
- Marketing and Sales personnel

2 VCC Ramp and the Importance of Correct Power-up Sequencing

The internal operation of a Flash memory is complex. Storing and erasing cells in the memory array relies on quantum-mechanical principles, requiring analog and digital circuitry controlled by an integrated controller or complex state-machine that, like any other digital system, must start from a known state, which is predicated upon a clean reset and correct power-up sequence.

During the power-up sequence (also known as “VCC ramp”), the power supply voltage is ramping up, and numerous events take place in the device.

The power supply must rise in a monotonically, non-decreasing fashion. The VCC waveform should not have a dip or a prolonged steady value during the rising edge. It must reach the minimum operational voltage for the device within a period specified in the datasheet. It must have a specific minimum slew rate. A few examples of a good and bad VCC ramps are illustrated later in this document.

The VCC Ramp in Figure 1 shows the events that take place as the VCC is ramping

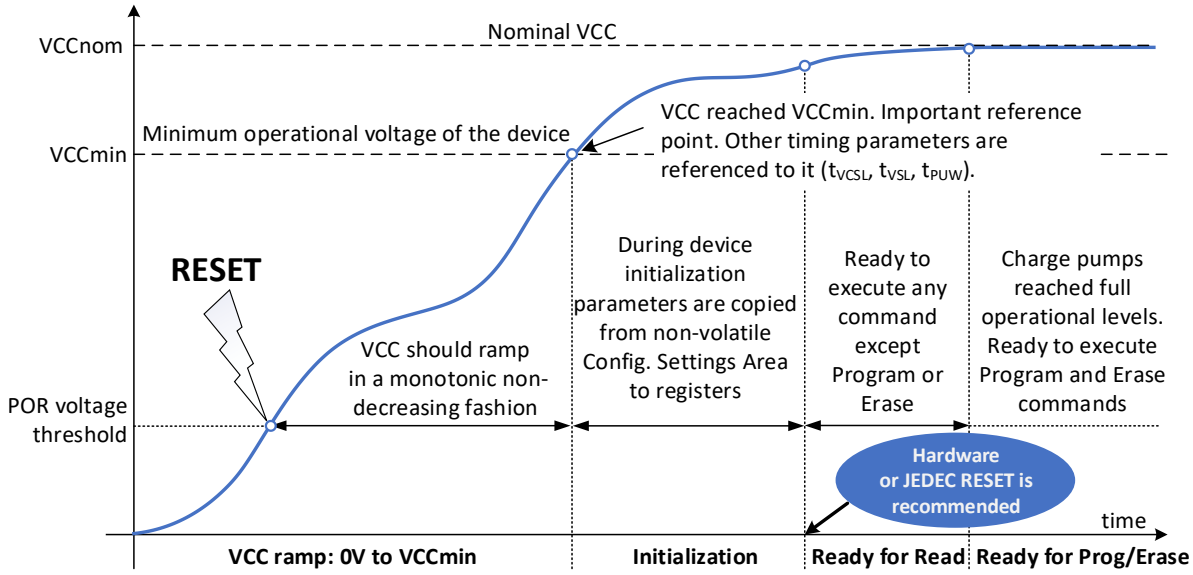


Figure 1: VCC Ramp

On power-up, the power supply voltage increases. Once it reaches the Power-On-Reset (POR) voltage threshold, it triggers the POR integrated circuitry whose function is to ensure the device starts up from a known, predefined state. The implementation of the POR circuitry varies from manufacturer to manufacturer and product to product.

The typical POR threshold voltage range is 1.4 V to 1.6 V. For actual values, see the datasheet. For some products, this voltage may not be published.

As VCC keeps ramping up, it eventually reaches a voltage level close to V_{CCmin}, at which the internal circuitry starts to come alive and the initialization sequence commences.

Part of the initialization is to copy system parameters stored in the device’s non-volatile memory, also known as *Configuration Settings Area*, into the working registers of the Flash.

It is very important that during the initialization the voltage does not drop below V_{CCmin}, otherwise the integrated state machine may not operate correctly, or register values may get corrupted, which can result in erroneous device operation.

Once the initialization is complete, the internal state-machine is ready to accept and execute commands from the host MCU (except Program and Erase operations for some devices).

In the datasheet, the time from V_{CCmin} until the CS# is allowed to go to Low is typically specified by timing parameters t_{VCSL} or t_{VSL} (check the datasheet for details).

The first command customers often issue is a query device ID, to verify if the Flash is responsive. If the device responds with the correct device ID, it indicates that it is operational.

Alternatively, to ensure a robust power-up sequencing, it is highly recommended that the first command to be a hardware reset, through a dedicated RESET pin, or a *JEDEC RESET*[1] for devices that support it.

The advantage of issuing a hardware or JEDEC reset when VCC is at, or above, V_{CCmin} is that the risk of incorrect initialization, due to marginally low VCC voltages (as it happens during a VCC ramp), is completely avoided.

Both approaches are valid, but the method where the first operation is a hardware reset is more robust.

Most Flash commands, including read commands, do not require high internal voltages; therefore, these commands are the first that can be executed after power-up.

Program and Erase operations rely on high internal voltages, and for some devices additional time is required for charge pumps to reach their operational levels and stabilize.

When CS# is driven to a Low logical level, the device is selected, and its internal state machine is enabled: it is now ready to accept and process commands from the host MCU. It is not desirable, nor a good design practice, to enable the state-machine prematurely (by letting CS# be in the active, logical Low state), before the correct initialization sequence is fully completed.

For that reason, it is important that during the power-up sequence the CS# (active low Chip Select signal) tracks the VCC. This ensures that during the power-on sequencing the state-machine is never in an active state, preventing accidental execution of internal algorithms before the device is fully initialized.

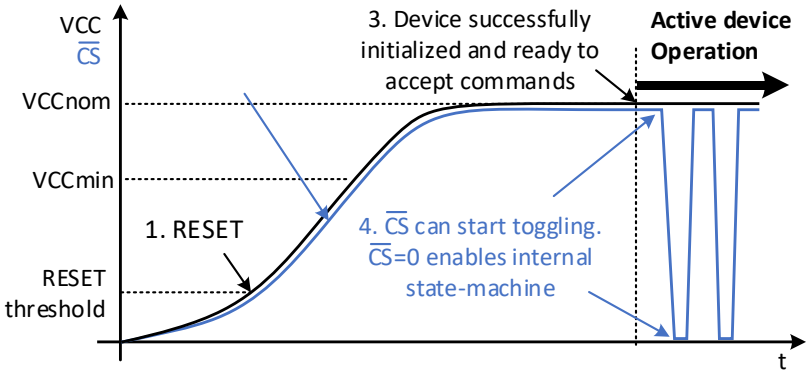


Figure 2: CS Tracks VCC During Power-Up

[1] JEDEC RESET is defined by standard #: JESD252

2.1 The importance of correctly loading configuration settings during power-up

There are batch-to-batch, wafer-to-wafer, and die-to-die differences that are sensitive to manufacturing process variations. Because of that, device-specific parameters are established during the testing phase of the manufacturing process and their values are stored in the *Configuration Settings Area*.

The *Memory Array* in a Flash is very analog in nature. The proper operating parameters are sensitive to process variations, and because of that they differ from device to device. Thus, during device characterization and also during the manufacturing process, tests are performed to establish parameters such as the bandgap voltage, reference currents, internal operating frequencies, charge pump reference voltages, sense-amplifier or current/voltage-comparator reference values, which are stored in Configurations Settings Area. Some parameters are specific to a device family; some of them are unique for each device.

The Configuration Settings Area is a small, non-volatile memory section inside the Flash, that stores important operating parameters for the device.

The configuration settings are read and copied into the internal registers of the device on each power-up or hardware reset.

Internal registers store parameters used by the controlling state-machine, and their programmed values affect the way the internal built-in algorithms are executed.

The Configuration Settings can be categorized as:

- Product-specific parameters, such as Product IDs, date-codes, wafer number, X-Y coordinates of the die on the wafer, etc. and other parameters important to back track the origin of the die once dispatched to the field.
- Parameters determining internal reference voltages, currents, timing parameters, and frequencies. Many parameters are unique to a device, and they are established during manufacturing and testing.
- Parameters required for the execution of internal algorithms are:
    - reference voltage values that are used to determine if the cell is sufficiently programmed or erased,
    - number of attempts the internal algorithm takes to program a cell before giving up and moving on to the next cell, and
    - number of attempts the internal algorithm takes to pre-program, erase, and recover cells or blocks of memory, while executing the variety of phases during the Erase operation.
- Mappings of redundant bit-lines.

  During the manufacturing process it is likely that some memory cells are not functional. To maximize yield, some level of redundancy is built into the device. During device manufacturing and testing, defective memory cells are detected; e.g. cells stuck high or low due to die contamination or process variations. When failed cells are detected, the entire bit-line is substituted and remapped to one of several built-in redundant bit-lines. The mapping of defective and correct bit-lines is stored in the Configuration Settings Area.

2.2 Consequences of Incorrect Power-up Sequencing

If any of the configuration registers are not initialized correctly during power-up, there can be wide-ranging consequences. Some failures can be quite obvious, e.g. device not starting up; to more subtle failures that occur only under extreme conditions (corner case VCC levels and/or extreme high or low temperatures). Some failures may be immediately observable, while some start to manifest themselves as performance degrades over time.

Here are a few examples of some potential issues:

- Unreliable programming and/or degradation in device endurance as a result of incorrect initialization of reference voltages and current sources.
- Incomplete erase or programming of the device as a result of incorrect initialization of internal voltage references or charge pump voltages.
- Timing issues because of the incorrect initialization of the internal timing generators.
- Potential marginal bit values that sometimes read a ‘1’ and sometimes a ‘0’ (perhaps at marginal power supply voltage or extreme temperatures) because some cells were insufficiently programmed or erased.
- A flipped cell value as a result of internal disturbances in the device. Sensitivity to internal disturbances can be made worse if the Configuration Settings values are incorrect or corrupt. There are failure mechanisms that flip a ‘1’ to a ‘0’, and other mechanisms that flip a ‘0’ to a ‘1’.

Diagnosing issues that are the consequence of incorrect power up sequencing can be quite complex and time consuming. For that reason, the effort required to properly design a power-up sequencing circuit becomes very important. It is better to ensure correct power-up sequencing than eventually having to deal with complicated and obscure symptoms that may show up intermittently or at corner cases only and are a debugging nightmare.

2.3 Power-up sequencing in the datasheet

A proper power-up sequencing is critical to correct operation of the Flash. The power supply must adhere to the parameters specified in the datasheet.

Unfortunately, due to historical reasons, the Power-up Timing in the datasheet is specified using different styles. Some manufacturers prefer one style over the other. It is not unusual to see the same manufacturer using different styles for different products. There are two prevalent styles and this document presents both. There are products that use a variation of the two, or something unique.

2.3.1 Power-Up Timing Example 1

Below is one example of parameters and timing diagram:

Table 1: Example 1 Parameters

Parameter	Range
Operating Temperature (Case)	-40 C to 85 C
VCC Power Supply*	1.65 V to 3.6 V

* In this example V_{CCmin} is 1.65 V as indicated by the minimum value of VCC Power Supply range.

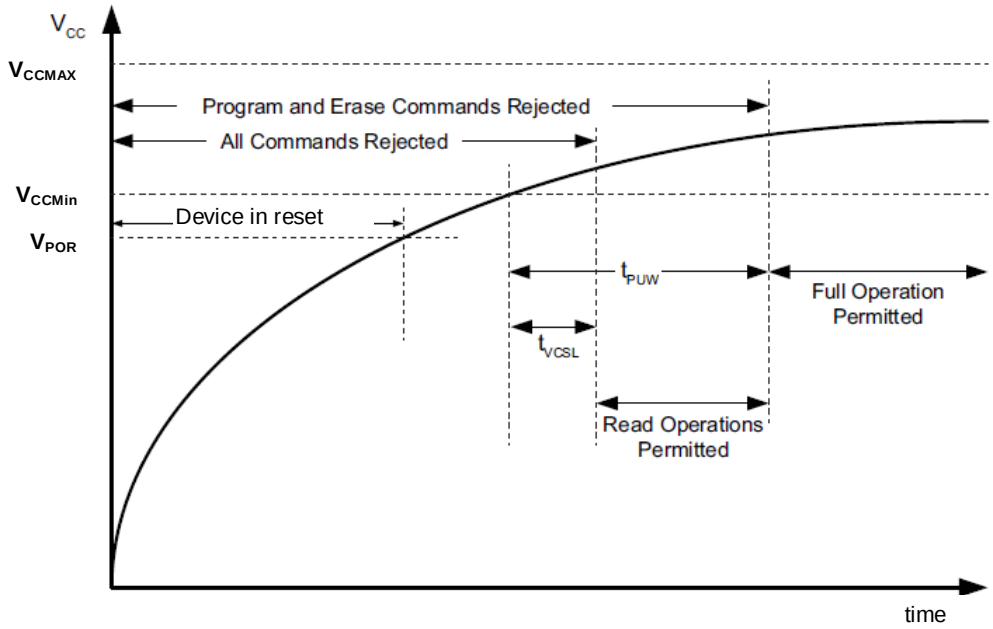


Figure 3: Power-Up Sequencing Timing Parameters (Example 1)

Table 2: Example 1 Timing Parameters

Symbol	Parameter	Min	Max	Units
t_{VCSL}	*VCC minimum* to *Chip Select Low* time for Read command		260	µs
t_{VR}	VCC rising edge from 0V to V_{CCmin}	1	500000	µs/V
V_{POR}	Power on reset voltage	1.45V	1.6	V
t_{PUW}	Power up delay time before Program or Erase is allowed		3	ms

When power is applied to the device, VCC must ramp at a specific rate (t_{VR}) for example not slower than 500 ms/V. This is a slow rising edge, and it is expected that any decent power supply can easily meet it. t_{VR} indicates the range of acceptable values.

The quality of the VCC ramp and the speed of its rising edge is completely under the systems designer control and is based on the type and topology of the power supply, component values, tolerances, etc.

The ramp must be clean, with minimum noise, and monotonically non-decreasing.

Calculating the time from power-up until the device is ready to accept commands consists of the following steps:

1. The *0V to V_{CCmin}* rate must be established by measurements or calculations. This part is completely determined by the power supply. The Flash device maker cannot know what kind of power supply is to be used, and the shape and speed of the VCC rising edge. When designing a system, the user must use the most conservative value (slowest rising edge) for calculations.
2. Look up t_{VCSL} in the datasheet, which represents the *"VCC minimum to chip select low"* time. It guarantees, that the device initialization and all other actions that make the Flash ready to accept Read commands, will be completed by the time specified. The beginning of t_{VCSL} is referenced to V_{CCmin}.

For devices where extra time is necessary to prepare the device for Erase and/or Program operation, the t_{PUW} *"Power up delay time before Program or Erase is allowed"* is also provided.

3. Add the two together: (time from 0 to V_{CCmin}) + t_{VCSL}
   For devices that require extra time for Program/Erase, use (time from 0 to V_{CCmin}) + t_{PUW}

2.3.2 Power-Up Timing Example 2

Figure 4 shows the second common style.

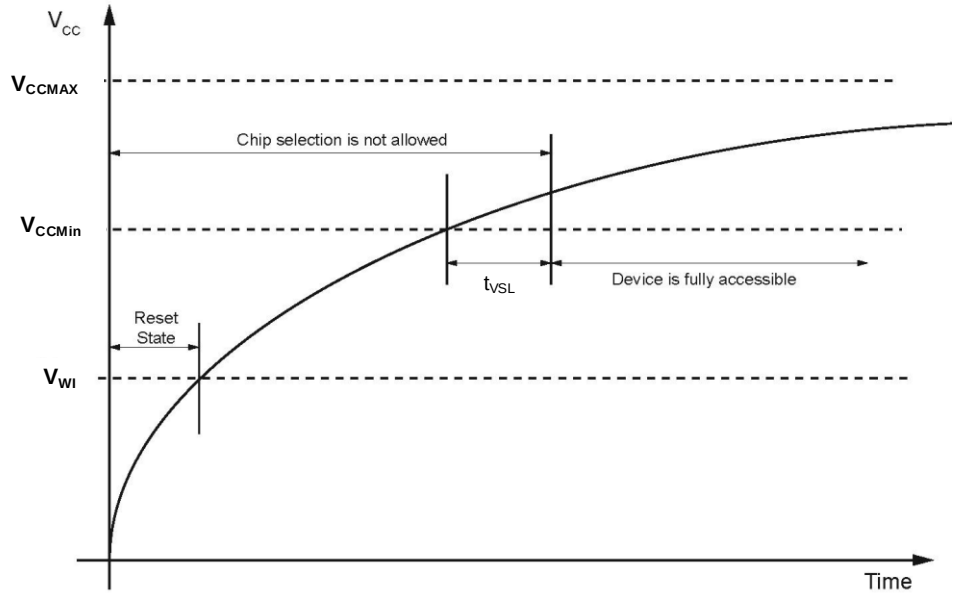


Figure 4: Power-Up Sequencing Timing Parameters (Example 2)

Table 3: Example 2 Timing Parameters

Symbol	Parameter	Min	Max	Units
t_{VSL}	VCCmin to CS Low	1.5		ms
V_{WI}	Write Inhibit Threshold Voltage	1.0	1.4	V

As it was the case with Example 1, calculating the time from power-up until the device is ready to accept commands consists of the following:

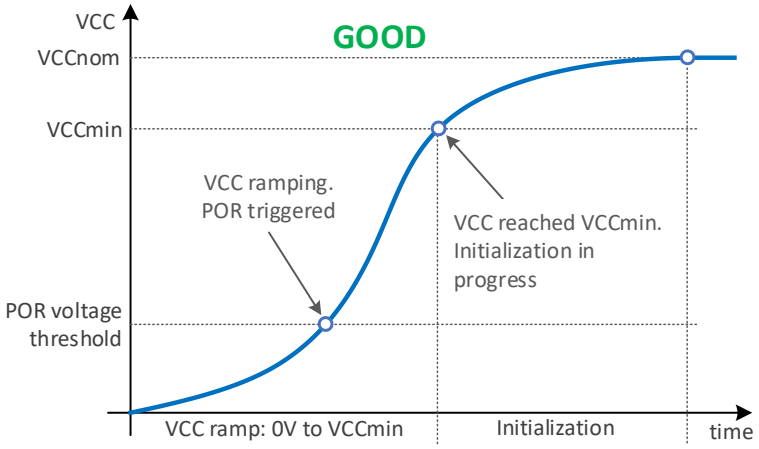
1. Establish *0V to V_{CCmin}* time, by measurements or calculations. Use the most conservative value.
2. Look up t_{VSL} in the datasheet which represents the *"VCCmin to chip select low"* as in Example 1. In this example the user must wait minimum 1.5ms before CS# is allowed to go Low.
3. Add the two together: (time from 0 to V_{CCmin}) + t_{VSL}

The POR voltage threshold is specified as *Write Inhibit Voltage* (V_{WI}). When VCC drops below this value, the device is reset.

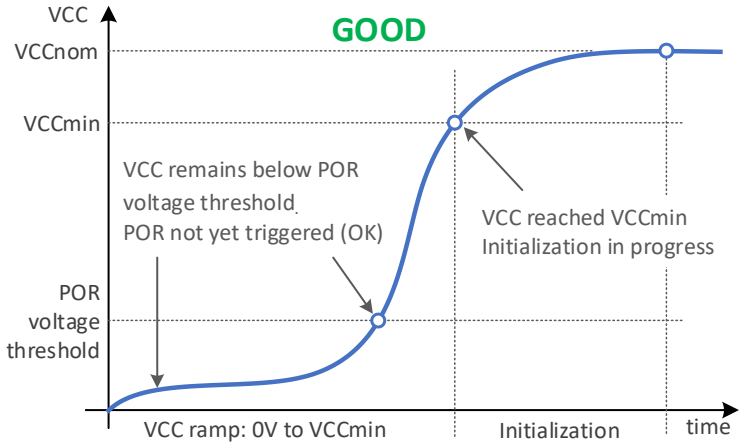
2.4 Examples of good and bad VCC ramps

To better illustrate the timing requirements of a correct power-up sequencing, four actual VCC ramp examples are provided, two good and two bad cases.

1. Curve 1 illustrates an excellent VCC ramp. After the initial rise of VCC, it reaches the POR voltage threshold that triggers the POR circuitry. The VCC keeps ramping up, eventually reaching V_{CCmin}. When reaching a voltage close to V_{CCmin}, the initialization process is initiated and since VCC is at or above V_{CCmin} the initialization will be successfully completed.



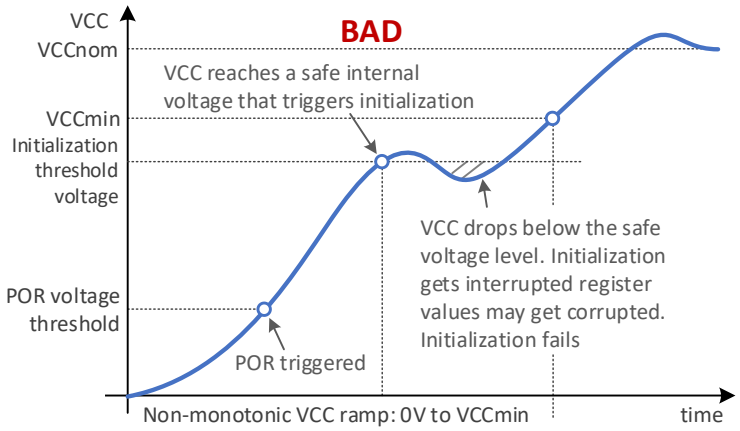
2. Curve 2 is also an acceptable VCC ramp. Initially, VCC starts rising, but not yet reaching the POR threshold. Since the POR circuitry was not triggered, no harm was done. When VCC finally reaches the voltage threshold that triggers the POR circuit, VCC reaches V_{CCmin} relatively quickly. By the time the initialization starts, VCC is close to, or above V_{CCmin} ensuring good initialization.



3. Curve 3 is like curve 2, except in this case the early part of the VCC ramp is large enough to trigger the POR reset circuitry. After that, VCC lingers close to the internal voltage that may trigger the initialization (initialization threshold voltage). If the initialization was triggered and the voltage drops below this threshold, the initialization is interrupted and may fail.

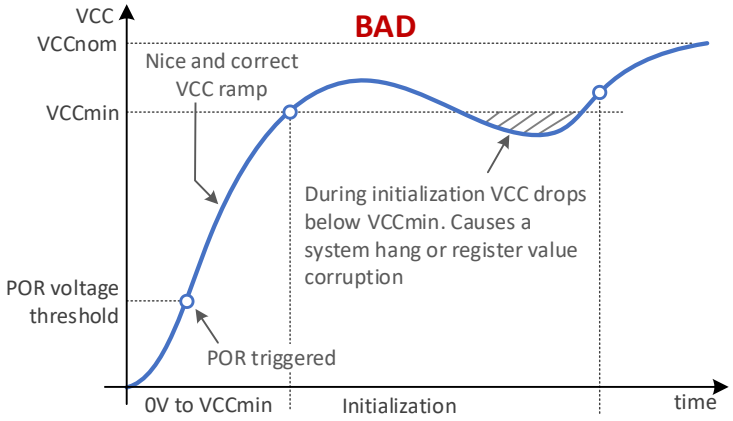
There is risk of incorrect initialization any time the VCC ramp does not have a monotonically non-decreasing shape. If the initialization was triggered and it was followed by a dip in the supply voltage, or there is a hump or oscillation around the threshold voltage, the device may fail for multiple reasons:

- Due to marginally low VCC voltage the internal state-machine may stop responding resulting in a system halt,
- It is possible that, despite the low supply voltage the internal state-machine is still functional, but during initialization some bits are not copied correctly from Configuration Settings Area to the internal working registers or some internal register values may get corrupted. The consequences of that can show up in later device operation, depending which bits were affected.



4. Curve 4 is similar to curve 1, except during the initialization at one-point VCC drops below V_{CCmin}. This is a condition is called a “brown-out”. The details of how to prevent such condition and how to recover from it, will be discussed in a chapter dedicated to brown-out condition.

   As in curve 3, the consequences can be a system halt, or some registers bits getting corrupted, which may manifest itself later as incorrect device operation.



3 Reset

Systems generally use a reset function at power-up to ensure that all parts of the system start in a known state. Reset can also be used to recover from serious faults that may be caused by hardware problems during runtime. These can include signal integrity and timing problems, electromagnetic interference, etc. Software bugs can also cause a program to crash and become unresponsive.

There are two major categories of reset: hardware and software.

3.1 Hardware Reset

Some Flash memory devices have a RESET# (active low) pin. When that pin is pulled low, an internal reset is performed.

Sometimes, the RESET# pin is combined with a hold functionality; it then becomes RESET#/HOLD#. Typically, the pin functionality can be programmatically configured in the *Status Register*.

Potential issues with the dedicated hardware pin are:

- Requires a dedicated pin on the Flash device.
- Requires a dedicated Reset control signal on the host MCU, which means another pin is used up on the MCU that could have been used for other purposes.
- Requires software to control when and how this signal is toggled.
- When the SPI operates in *Quad Mode*, instead of using two communication signals (SI and SO), four bidirectional signals are used: IO[3:0]. In such cases, the RESET# pin is re-configured into an input/output pin, and the reset functionality is lost.

The picture below shows two block diagrams: the first system (Figure 5a) is in SPI mode with a hardware reset pins on both, the MCU and the Flash. The second system (Figure 5b) is in Quad mode, where the RESET# signal on the flash was repurposed to an I/O pin.

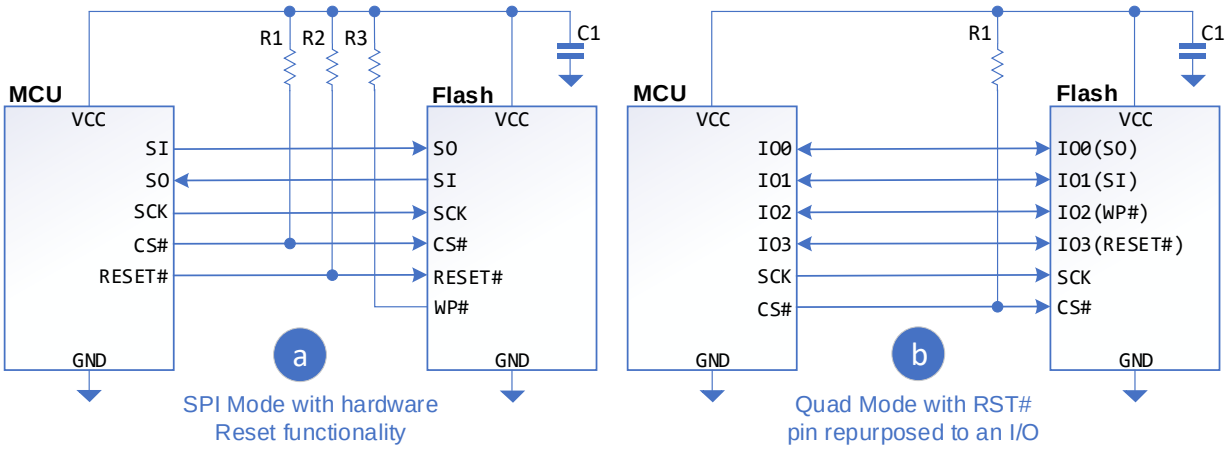


Figure 5: SPI and Quad Modes with and without a Hardware Reset Functionality

There is another method to reset the Flash (for the devices that support it): the so called JEDEC Reset described in the next section.

3.2 JEDEC Reset

JEDEC reset is an alternative way of performing hardware reset. It is a useful feature, because it does not require a dedicated reset pin on the flash and on the MCU. It uses the existing SPI signals (in-band hardware reset). Reset is performed with a short sequence which toggles CS# and SI, while SCK is kept inactive. The details of how JEDEC Reset works is described in the Appendix.

One useful application of the JEDEC Reset is when the MCU and the Flash communicate with each other using advanced quad-SPI or octal-SPI modes (for example QPI or Quad 0-4-4).

If for any reason the MCU is reset, the MCU's flash host controller reverts to standard SPI communication. The MCU is unaware of the state of the Flash and so they may get out of sync and unable to communicate. The MCU must reset the flash to get back in sync with it.

The solution to this issue is to perform a JEDEC Reset, an option which is available in many modern flash products and is quite simple. A dedicated reset pin option is not available in most cases. The only other option is a reset procedure performed in software, which can be long and complicated.

The JEDEC Reset is equivalent to the one that is performed during the VCC ramp. Everything gets reset, the device is re-initialized, and the internal registers are reloaded from the Configuration Setting Area.

NOTE:

The advantage of issuing a hardware or JEDEC reset when VCC is at or above V_{CCmin} is that the risk of incorrect initialization, due to marginally low power supply voltages (as can happen during VCC ramp) is completely avoided.

3.3 Software Reset

Software reset is performed by sending a sequence of two commands in sequence over the SPI interface: Reset Enable (66h) and Reset (99h). It is required that the Flash's communication interface is still operational and able to receive and process commands. If the Flash is in a mode where it no longer can accept commands through the SPI interface, the software reset cannot work.

Software reset is used when the state-machine hangs, but the communication interfaces are still working. In that case, the state-machine can be restarted.

Software reset is not as powerful as the hardware or JEDEC resets because in some cases (depending on the implementation), it does not fully re-initialize the chip. The internal registers are not reloaded from the Configuration Settings Area, and if there was a register corruption, that condition will not be rectified.

Refer to the datasheet to find out the exact effect of the software reset for a specific device.

If there is any doubt that the device may have been exposed to a brown-out or a voltage glitch, the safest thing to do is to execute a hardware or JEDEC reset.

4 Brown-out

If during normal operation, the operating VCC voltage drops below a specified minimum voltage (V_{CCmin}), it is possible that either the internal state-machine hangs or the content of the internal registers, containing the unique parameters for that particular Flash memory device, get corrupted. The consequences are similar to incorrect power-up sequencing.

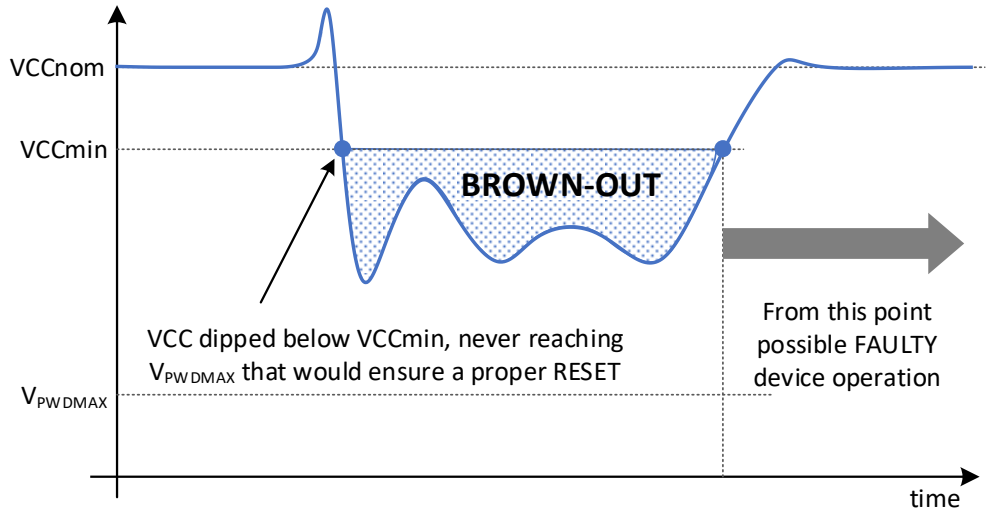


Figure 6: Brown-out Condition

Once the voltage of the device falls below the V_{CCmin} level (see Figure 6) proper operation cannot be guaranteed. In the area shown between V_{CCmin} and V_{PWDMAX}, the device is in an indeterminate state, where some of the internal circuits may be functioning, and others may not. Therefore, once the voltage falls below V_{CCmin}, it must continue to fall below V_{PWDMAX}, to ensure it dropped below the threshold of the POR circuitry.

Table 4: Brown-out Sequencing Timing Parameters

Symbol	Parameter	Min	Max	Units
V_{PWDmax}	Maximum VCC brown-out		0.2	V
t_{PWD}	VCC brown-out low time	300		µs

In this example V_{PWDMAX} is 0.2 V (Table 4). Once the V_{PWDMAX} voltage is reached, it must remain at this level for a minimum of t_{PWD} (in Table 2 this is 300µs) before another power-up is attempted.

4.1 Causes of brown-out conditions

Brown-out conditions can occur due to:

- Disruption of the main power in the system
- Incorrect voltage regulation of the power supply
- Glitches in the VCC
- Large noise in VCC
- Low battery condition in battery operated devices

4.2 Recovery from a brown-out condition

In case VCC has dropped below V_{CCmin}, effectively we have a brown-out condition.

The correct recovery procedure is to turn off VCC and let it decay toward 0V. As VCC is decreasing, it is required to wait until VCC drops below V_{PWDMAX}. Once VCC is below V_{PWDMAX} it is important to wait t_{PWD} to ensure the device is fully powered down and ready for the next power up sequence.

After t_{PWD} has elapsed VCC can be reapplied. The power-up sequence is identical to the sequence described in Section 2. The device requires a specific ramp-up time to reach V_{CCmin}, and then an initialization time as defined by the time t_{VCSL}.

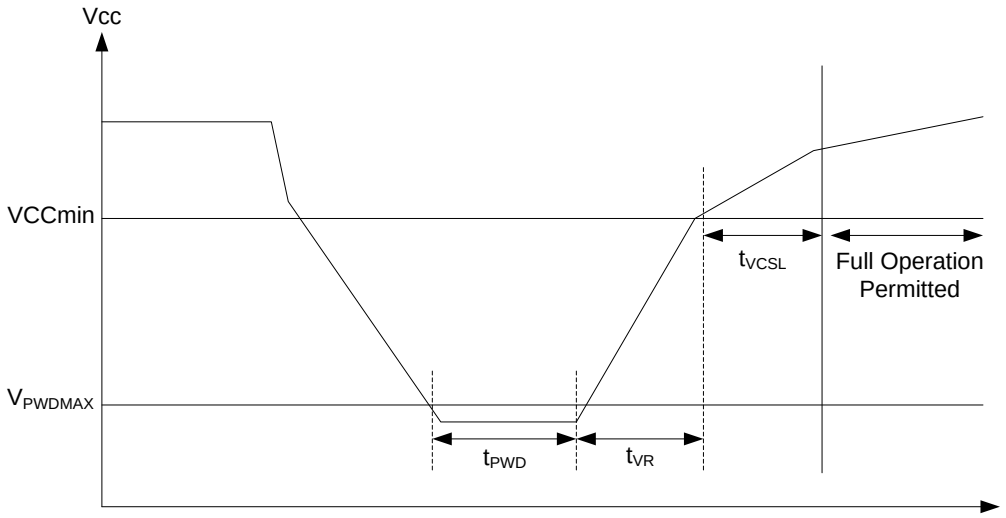


Figure 7: Recovery from Brown-Out Condition

4.3 Avoiding a brown-out condition

The best is to avoid brown-out conditions altogether:

- Follow correct power-up sequencing. The Chip Select pin (CS#) must track VCC during ramp-up, so the device does not wake up in active state prematurely (before critical parameters are initialized),
- Provide stable power supplies,
- Minimize power supply noise,
- Provide sufficient decoupling on VCC,
- Carefully lay-out the PCB, provide a low-impedance (ESR, ESL) path from decoupling capacitors to VCC pin. Refer to PCB layout guidelines for more information.

If there is a suspicion that a brown-out condition has occurred, it is best to decrease VCC to below the reset threshold voltage (V_{PWDMAX}) so that the POR circuitry is safely turned off and armed for the next power-up sequence. Once this occurs, VCC can be reapplied in orderly fashion, as described in Section 2. The POR sequence can be properly executed again, and the correct configuration settings reloaded.

When VCC has reached a level above V_{CCmin} and has stabilized, it is also recommended to execute a hardware or JEDEC reset.

5 Power-Down

As the device is powered down it must be ensured that the VCC drops below V_{PWDMAX} (the threshold voltage of the POR reset circuitry) before another power-up sequencing is initiated.

If required, an off-the-shelf load switch[2] can be used or a discharge circuit may be designed for quickly discharging the decoupling capacitors, to avoid any remnant, floating voltages on VCC that may interfere with the next power up.

The picture below depicts a conceptual discharge circuitry using discrete components.

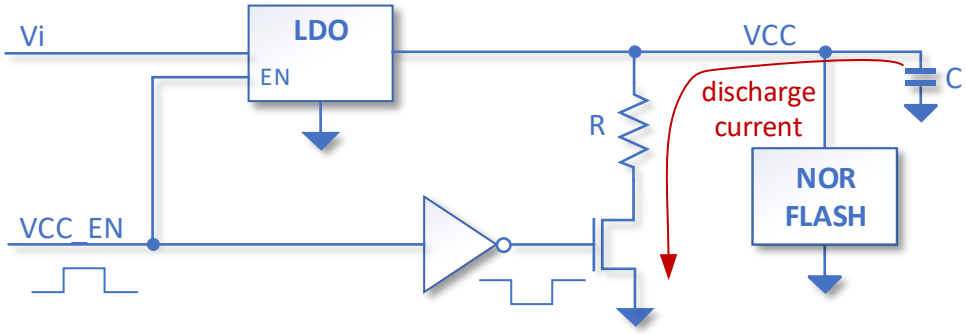


Figure 8: Discharge Circuitry with Discrete Components

[2] Example load switches: TI TPS20xxC or Dialog SLG46617

6 Power Cycling and Power Saving Modes

To save system power, system designers often chose to power-down the Flash device when not in use; or the device is put into one of a variety of power-saving modes (like the ultra-Deep Power Down) with a software command, for Flash devices that support this feature, like Dialog's Wide VCC devices. The device internally manages which parts of the device remain powered and which ones are turned off.

6.1 Power Cycling (Power-Off Followed by a Power-On)

In a full power-down mode, the VCC of the external power supply is powered down.

Immediately after power down, the VCC is decreasing toward 0V. In some device families there are internal nodes within the Flash that may remain energized. The electrical charge must be discharged before powering-up the device again, to ensure a clean and correct power-up sequence.

This discharge may take some time under extreme conditions, for instance when the temperature is very low.

To ensure a robust power-up sequencing after the device is powered down, it is important to allow sufficient time for these internal nodes to be fully discharged.

The time required is different for different device families. Below is an example list of device families that are affected with corresponding minimum required wait times. Note that this information may not be listed in the datasheet.

Table 5: Example of Minimum Wait Time After Power-Down or Ultra Deep Power Down Before Resuming Normal Operation (Per Device Family)

Device family	Minimum required wait time
AT25XE	550 ms
AT25FF	550 ms
AT25EU	750 ms *

* under extreme conditions it can go up to 1500ms

Immediately after power-up, once the VCC has reached its operational level and is stabilized, the first command should be a hardware or JEDEC reset, as already described in previous sections. This ensures that any potential issues during power-up sequencing are resolved.

6.2 Entering and Exiting Ultra-Deep Power-Down (uDPD)

Another common way of saving electrical power is to enter Ultra-Deep Power-Down (uDPD) for devices that support this feature. Refer to the datasheet for how to enter and exit uDPD.

A typical command to enter uDPD is 79h (or B9h in some devices).

The characteristic of this power mode is that large parts of the internal electrical circuitry is powered down, keeping only essential circuitry alive.

Similar issues as with power-cycling (described in the previous section) may occur. After some parts of the device are powered down, there are nodes in the device that still remain energized. The electrical charge must be discharged below a specific voltage level to ensure that on the next power-up this circuitry goes through its own, proper power-up sequence. Thus, it is important to allow sufficient time between entering uDPD modes and before resuming normal operation. This is critical especially when the device is operating under corner case conditions (marginal VCC values and extreme temperatures).

The time required is different for different device families. The minimum required wait time (time required to remain in power-saving mode, to allow the internal nodes to properly discharge) is listed in Table 5.

A typical command to resume normal operation from uDPD is ABh.

After exiting uDPD, make the first command a hardware or JEDEC reset, described in previous sections. This ensures that any potential issues during power-up sequencing are resolved. Read the manufacturer ID to confirm the device is operational.

Appendix A

a) JEDEC Reset (JEDEC Standard #: JESD252)

The JEDEC RESET command sequence can be used to wake up the device from Deep Power-Down (DPD) or ultra-Deep Power-Down (uDPD) modes. This sequence can also be used to reset the device to a state similar to the power-on state without cycling power.

The reset sequence does not use the SCK pin. The SCK pin has to be held low (mode 0) or high (mode 3) through the entire reset sequence. This prevents any confusion with commands, as no command bits are transferred (clocked).

A reset is commanded when the data on the SI pin is 0101 on four consecutive positive edges of the CS pin with no edge on the SCK pin throughout. This is a sequence where:

1. CS is driven active low to select the device.
2. Clock (SCK) remains stable in either a high or low state.
3. SI is driven low by the bus master, simultaneously with CS going active low. No SPI bus slave drives SI during CS low before a transition of SCK.
4. CS is driven inactive. The slave captures the state of SI on the rising edge of CS.

The above steps are repeated 4 times, each time alternating the state of SI.

After the fourth CS pulse, the slave triggers its internal reset. SI is low on the first CS, high on the second, low on the third, and high on the fourth. This provides a value of 5h, unlike random noise. Any activity on SCK during this time halts the sequence, and a Reset is not generated.

The device always reverts to standard SPI mode after a JEDEC hardware reset.

It is important to understand what parts of the device circuitry gets reset after a JEDEC reset is performed. This can vary from product to product, and it is described in detail in the datasheet.

Figure 9 illustrates the timing for the JEDEC hardware reset operation.

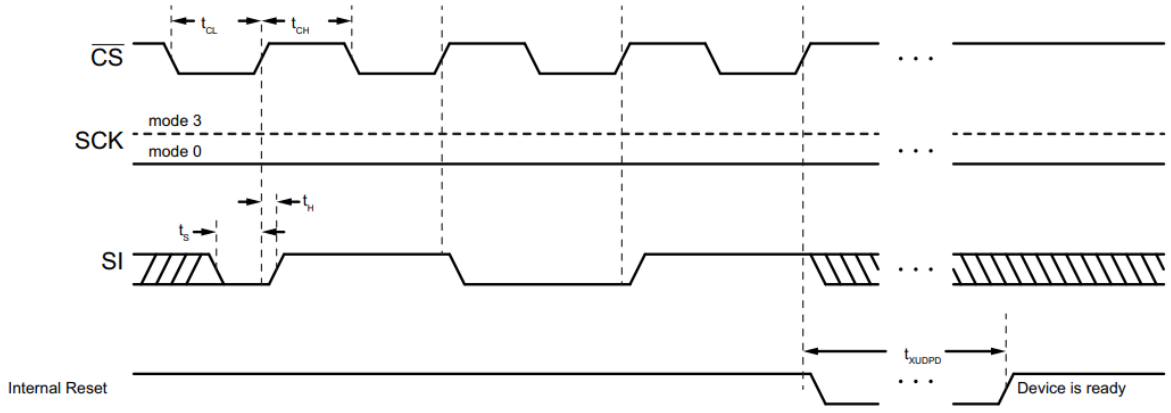


Figure 9: JEDEC Hardware Reset Timing

b) ABh Command

Executing an ABh command while in uDPD mode causes the device to exit uDPD and resume normal operation, returning to an idle state. This command causes the device to perform an internal reset. In this case, the SRAM contents are undefined.

c) Device Resets

In addition to the ABh command, performing a Power-On-Reset (POR), a JEDEC reset, or asserting the hardware reset pin (RESET#) also causes the device to exit uDPD. If the device is reset in any of these three ways, the SRAM contents are undefined.

d) Enable Reset (66h) and Reset (99h) Commands

Executing the Reset command (66h/99h) terminates all internal operations and causes the device to initialize. Once the software Reset instruction is accepted, any on-going internal operation are terminated, and the device returns to its default power-on state and loses all of the current volatile settings, such as Volatile Status Register bit, Write Enable Latch (WEL) status, Program/Erase Suspend status, Continuous Read Mode bit setting, etc.

To avoid accidental reset, both Enable Reset (66h) and Reset (99h) instructions must be issued in sequence. Any other command other than Reset (99h) after the Enable Reset (66h) command disable the Reset Enable state. A new sequence of Enable Reset and Reset is needed then to reset the device.

List of Figures

Revision History

Revision	Date	Description
A1	05-2021	Initial release.
A2	09-2021	Added a note to Table 5

