To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

4509 Group

Input/Output Port

1. Abstract

The following article provides application examples and setting examples of input/output ports of 4509 Group.

2. Introduction

The explanation of this issue is applied to the following condition:

• Microcomputer: 4509 Group

Due to the bit location for the control register, a bit with no function may be operated in some cases.
Values can be optionally set on those bits.

3. Input/Output Port

3.1 Port P0

Port P0, 4 bits supported, has input and output functions. Ports $P0_0$ through $P0_2$ share their pins with Serial interface ports SIN, SOUT, and SCK.

The key-on wakeup function can be switched On/Off by setting register K0 by setting register PU0, whereas the pull-up transistor function can be switched On/Off also by setting register PU0.

Further, the output format from the ports can be selected from two options by setting register FR0. The format options are N-channel open-drain ouput and CMOS output.

3.1.1 Port P0 Input/Output Procedure

・Input Procedure

Corresponding to the port to be used, set "0" to registers $FR0_0$ though $FR0_3$ and set "1" to the output latch of port P0i (i: 0 through 3) by OP0A instruction. "L" will be input, if "0" is set to the output latch.

By executing IAP0 instruction, the content of port P0 is transfered to register A.

・Output Procedure

The contents of register A is output to port P0 by OP0A instruction.

The output format for each pin can be selected from two options according to the condition of registers $FR0_0$ through $FR0_3$. One format option is N-cahnnel open-drain output, and the other is CMOS output.

Note1: Port $P0_0$ shares its pin with Serial interface SIN; therefore set "00_2" or "01_2" to registers $J11_1$ and $J10_0$ when using the pin as port $P0_0$.

Note2: Port $P0_1$ shares its pin with Serial interface SOUT; therefore set "00_2" or "10_2" to registers $J11_1$ and $J10_0$ when using the pin as port $P0_1$.

Note3: Port $P0_2$ shares its pin with Serial itnerface SCK; therefore set "00_2" to resgisters $J11_1$ and $J10_0$ to when using the pin as port $P0_2$.

3.2 Port P1

Port P1, 4 bits supported, has input and output functions.

The key-on wakeup function and the pull-up function can be switched On/Off by setting register K1 and register PU1 respectively.

The output format from the port can be selected from two options by setting register FR1. The one format is N- channel open-drain output, and the other is CMOS output.

Further, ports $P1_1$, $P1_2$, and $P1_3$ share their pins with terminals CNTR1 input/output, CNTR0 input/output, and INT input, respectively. INT performs switching On/Off of the key-on wakeup by setting register $L1_0$.

3.2.1 Port P1 Input/Output Procedure

・Input Procedure

Corresponding to the port to be used, set "0" to register $FR1_0$ though $FR1_3$ and set "1" to the output latch of port P0i (i: 0 through 3) by OP1A instruction. "L" will be input, if "0" is set to the output latch.

By executing IAP1 instruction, the content of port P1 is transfered to register A.

・Output Procedure

The contents of register A is output to port P1 by OP1A instruction.

The output format for each pin can be selected from two options depending on the setting of registers $FR1_0$ through $FR1_3$. One format option is N-channel open-drain output, and the other is CMOS output.

Note1: Port $P1_2$ shares its pin with Serial interface CNTR0; therefore set "0" to register $W5_3$ when using the pin as port $P1_2$.

Note2: Port $P1_1$ shares its pin with Serial interface CNTR1; therefore set "0" to register $W6_3$ when using the pin as port $P1_1$.

3.3 Port P2

Port 2, 2 bits supported, has input and output functions. Ports $P2_0$ and $P2_1$ sahre their pins with analogue input ports A_{IN0} and A_{IN1}.

The key-on-wakeup function can be switched On/Off by setting registers K21 and $K2_0$, whereas the pull-up function can be set to On/Off by setting registers $PU2_1$ and $PU2_0$.

Further, the output format from the port can be selected from two options by setting registers $FR2_1$ and $FR2_0$. The one format is N-channel open-drain output, and the other is CMOS output.

3.3.1 Port P2 Input/Output Procedure

・Input Procedure

Corresponding to the port to be used, set “0” to register $FR2_0$ and $FR2_1$ and set “1” to the output latch of port P2i (i: 0 and 1) by OP2A instruction. “L” is input, when “0” is set to the output latch.

By executing IAP2 instruction, the content of Port P2 is transfered to register A.

・Output Procedure

The contents of register A is output to port P2 by OP2A instruction.

The output format for each pin can be selected from two options according to the setting of registers $FR2_0$ and $FR2_1$. The format options are N-cahnnel open-drain output and CMOS output.

3.4 Port P3

Port 3, 2 bits supported, has input and output function. Ports $P3_0$ and $P3_1$ share the pins with analogue input ports A_{IN2} and A_{IN3}.

The output format from the port can be selected from two options by setting Registers $C1_1$ and $C1_0$. The one format is N-channel open-drain output, and the other is CMOS output.

3.4.1 Port P3 Input/Output Procedure

・Input Procedure

Corresponding to the port to be used, set “0” to register $C1_0$ and $C1_1$ and set “1” to the output latch of port P3i (i: 0 and 1) by OP3A instruction. “L” will be input, when “0” is set to the output latch.

By executing IAP3 instruction, the content of port P3 is transfered to register A.

・Output Procedure

The contents of register A is output to port P3 by OP3A instruction.

The output format for each pin can be selected from two options according to the setting of registers $C1_0$ and $C1_1$. The format options are N-cahnnel open-drain output and CMOS output.

3.5 Port D

Port 3, 6 bits supported, has input and output functions. Ports D_2 and D_3 share the pins with analogue input ports A_{IN4} and A_{IN5}.

For Ports D_2 and D_3, the key-on wakeup is switched On/Off by setting registers $K2_3$ and $K2_2$, whereas the pull-up function is switched On/Off by setting registers $PU2_3$ and $PU2_2$.

Further, the output format can be selected from two options by setting registers FR3, $C1_3$, and $C1_2$.
The available format are N-channel open-drain output and CMOS output.

3.5.1 Port D Input/Output Procedure

Port D performs input and output for each bit; therefore specify one pin out of six pins of port D by using register Y as a data pointer when performing input or output with ports D0 through D_5.

・Input Procedure

Corresponding to the port to be used, set “0” to registers FR3i (i= 0 through 3) and C1i (i= 2 and 3) and set “1” to the output latch of ports Di (i= 0 though 5) by SD instruction. When “0” is set to the output latch, “L” will be input.

If the content of the port, which has been designated by register Y, is “0” under SZD instruction, the next instruction will be skipped; contrarily the next instruction is executed, if it is “1”.

・Output Procedure

Set the output level by SD instruction and RD instruction.

The output format for each pin can be selected from two options according to the setting of registers FR3, $C1_3$ and $C1_2$. The output format options are N-cahnnel open-drain output and CMOS output.

The port will be “high impedance” or “H” level when executing SD instruction.

All ports of port D will be “high impedance” or “H” level when executing CLD instruction.

The prots will be “L” level when executing RD instruction.

Note1: Values higher than “0110_2” must not be set to register Y when executing SD instruction or RD instruction.

4. Relevant Register

4.1 Timer Control Register W5

Table 4.1 shows the bit configuration for Timer control register W5.

Writing to Register W5 can be performed by TW5A instruction after setting values to register A.

The contents of register W5 can be transfered to register A by TAW5 instruction.

Table 4.1 Bit Configuration for Timer Control Register W5

Timer control register W5		at reset: 0000_2	at RAM back-up: State retained	R/W TAW5/TW5A
$W5_3$	$P12$/CNTR0 pin function slection bit	0	$P12$ (I/O) / CNTR0 (input)	
		1	$P12$ (input) / CNTR0 (I/O)	
$W5_2$	Timer 1 count auto-stop circuit selection bit (Note 2)	0	Count auto-stop circuit not selected	
		1	Count auto-stop circuit selected	
$W5_1$	Timer 1 count start synchronous circuit selection bit (Note 3)	0	Count start synchronous circuit not selected	
		1	Count start synchronous circuit selected	
$W5_0$	CNTR0 pin input count edge selection bit	0	Falling edge	
		1	Rising edge	

Note 1: "R" represents read enabled, and "W" represents write enabled.

Note 2: It is valid only when both INT Timer 1 Control Enable bit ($I10$) and Timer 1 count start synchronous circuit selection bit ($W5_1$) are "1".

Note 3: It is valid only when INT Timer 1 control enable bit ($I10$) is "1".

Note 4: Unused bits while setting the port.

4.2 Timer Control Register W6

Table 4.2 shows the bit configuration for register W6.

Writing to register W6 can be achieved by TW6A instruction after setting values to register A.

The contents of register W6 can be transfered to register A by TAW6 instruction.

Table 4.2 Bit Configuration for Register W6

Timer control register W6		at reset: 0000_2	at RAM back-up: State retained	R/W TAW6/TW6A
$W6_3$	$P11$/CNTR1 pin function selection bit	0	$P11$ (I/O) / CNTR (input)	
		1	$P11$ (input) /CNTR1 (I/O)	
$W6_2$	CNTR1 pin output auto-control circuit selection bit	0	Output auto-control circuit not selected	
		1	Output auto-control circuit selected	
$W6_1$	Timer 2 INT input cycle count circuit selection bit	0	INT pin input period count circuit not selected	
		1	INT pin input period count circuit selected	
$W6_0$	CNTR1 pin input count edge selection bit	0	Falling edge	
		1	Rising edge	

Note 1: "R" represents read enabled. "W" represents write enabled.

Note 2: Unused bits while setting the port.

4.3 Serial Interface Control Register J1

Table 4.3 shows the bit configuration for Serial interface control register J1.

Writing to register J1 can be achieved by TJ1A instruction after setting values to register A.

The contents of register J1 can be transferd to register A by TAJ1 instruction.

Table 4.3 Bit Configuration for Serial Interface Control Register J1

Serial interface control register J1		at reset: 0000_2		at RAM back-up: state retained	R/W TAJ1/TJ1A
$J1_3$	Serial interface synchronous clock selection bits	$J1_3$	$J1_2$	Synchronous Clock	
		0	0	Instruction clock (INSTCK) divided by 8	
		0	1	Instruction clock (INSTCK) divided by 4	
$J1_2$		1	0	Instruction clock (INSTCK) divided by 2	
		1	1	External clock (S_{CK} input)	
$J1_1$	Serial interface port function selection bits	$J1_1$	$J1_0$	Port Function	
		0	0	$P0_0$, $P0_1$, $P0_2$ selected / S_{IN}, S_{OUT}, S_{CK} not selected	
		0	1	$P0_0$, S_{OUT}, S_{CK} selected / S_{IN}, $P0_1$, $P0_2$ not selected	
$J1_0$		1	0	S_{IN}, $P0_1$, S_{CK} selected / $P0_0$, S_{OUT}, $P0_2$ not selected	
		1	1	S_{IN}, S_{OUT}, S_{CK} selected / $P0_0$, $P0_1$, $P0_2$ not selected	

Note 1: "R" represents read enabled, and "W" represents write enabled.

Note 2: Unused bits while setting the port.

4.4 Pull-Up Control Register PU0

Table 4.4 shows the bit configuration for Pull-up register PU0.

Writing to PU0 can be achieved by TPU0A instruction after setting values to register A.

The contents of register PU0 can be transfered to register A by TAPU0 instruction.

Table 4.4 Bit Configuration for Pull-Up Register PU0

Pull-up control register PU0		at reset: 0000_2	at RAM back-up: state retained	R/W TAPU0/TPU0A
$PU0_3$	Port $P0_3$ pull-up transistor control bit	0	Pull-up transistor Off	
		1	Pull-up transistor On	
$PU0_2$	Port $P0_2$ pull-up transistor control bit	0	Pull-up transistor Off	
		1	Pull-up transistor On	
$PU0_1$	Port $P0_1$ pull-up transistor control bit	0	Pull-up transistor Off	
		1	Pull-up transistor On	
$PU0_0$	Port $P0_0$ pull-up transistor control bit	0	Pull-up transistor Off	
		1	Pull-up transistor On	

Note 1: "R" represents read enabled, and "W" represents write enabled.

4.5 Pull-Up Control Register PU1

Table 4.5 shows the bit configuration for Pull-up control register PU1.

Writing to register PU1 can be accomplished by TPU1A instruction after setting values to registere A.

The contents of register PU1 can be transfered to register A by TAPU1 instruction.

Table 4.5 Bit Configuration for Pull-Up Control Register PU1

Pull-up contorl register PU1		at reset: 0000_2		at RAM back-up: state retained	R/W TAPU1/TPU1A
$PU1_3$	Port $P1_3$ pull-up transistor control bit	0	Pull-up transistor Off		
		1	Pull-up transistor On		
$PU1_2$	Port $P1_2$ pull-up transistor control bit	0	Pull-up tansistor Off		
		1	Pull-up transistor On		
$PU1_1$	Port $P1_1$ pull-up transistor control bit	0	Pull-up transistor Off		
		1	Pull-up transistor On		
$PU1_0$	Port $P1_0$ pull-up transistor control bit	0	Pull-up transistor Off		
		1	Pull-up transistor On		

Note 1: “R” represents read enabled, and “W” represents write enabled.

4.6 Pull-Up Control Register PU2

Table 4.6 shows the bit configuration for Pull-up control register PU2.

Writing to register PU2 can be accomplished by TPU2A instruction after setting values to register A.

The contents of register PU2 can be transfered to register A by TAPU2 instruction.

Table 4.6 Bit Configuration for Pull-Up Control Register PU2

Pull-up control register PU2		at reset: 0000_2		at RAM back-up: state retained	R/W TAPU2/TPU2A
$PU2_3$	Port D_3 pull-up transistor control bit	0	Pull-up transistor Off		
		1	Pull-up transistor On		
$PU2_2$	Port D_2 pull-up transistor control bit	0	Pull-up transistor Off		
		1	Pull-up transistor On		
$PU2_1$	Port $P2_1$ pull-up transistor control bit	0	Pull-up transistor Off		
		1	pull-up transistor On		
$PU2_0$	Port $P2_0$ pull-up transistor control bit	0	Pull-up transistor Off		
		1	Pull-up transistor On		

Note 1: “R” represents read enabled, and “W” represents write enabled.

4.7 Port Output Structure Control Register FR0

Table 4.7 shows the bit configuration for Port output structure control register FR0.

Writing to register FR0 can be performed by TFR0A instruction after settting values to register A.

Table 4.7 Bit Configuration for Port Output Structure Control Register FR0

Port output structure control register FR0		at reset: 0000_2		at RAM bakc-up: state retained	W TFR0A
$FR0_3$	Port $P0_3$ output structure selection bit	0	N-channel open-drain output		
		1	CMOS output		
$FR0_2$	Port $P0_2$ output structure selection bit	0	N-channel open-drain output		
		1	CMOS output		
$FR0_1$	Port $P0_1$ output structure selection bit	0	N-channel open-drain output		
		1	CMOS output		
$FR0_0$	Port $P0_0$ output structure selection bit	0	N-channel open-drain output		
		1	CMOS output		

Note1: "W" represents write enabled.

4.8 Port Output Structure Control Register FR1

Table 4.8 shows the bit configuration for Port output structure control register FR1.

Writing to register FR1 can be performed by TFR1A instruction after setting values to register A.

Table 4.8 Bit Configuration for Port Output Structure Control Reigster FR1

Port ouptut structure control reigster FR1		at reset: 0000_2		at RAM back-up: state retained	W TFR1A
$FR1_3$	Port $P1_3$ output structure selection bit	0	N-channel open-drain output		
		1	CMOS output		
$FR1_2$	Port $P1_2$ output structure selection bit	0	N-channel open-drain output		
		1	CMOS output		
$FR1_1$	Port $P1_1$ output structure selection bit	0	N-channel open-drain output		
		1	CMOS output		
$FR1_0$	Port $P1_0$ output structure selection bit	0	N-channel open-drain output		
		1	CMOS output		

Note: "W" represents write enabled.

4.9 Port Output Structure Control Register FR2

Table 4.9 shows the bit configuration for Port Output structure control register FR2.

Writing to register FR2 can be accomplished by TFR2A instruction after setting values to register A.

Table 4.9 Bit Configuration for Port Output Structure Control Register FR2

Port ouput structure control register FR2		at reset: 0000_2	at RAM back-up: state retained	W TFR2A
$FR2_3$	Not used	0 1	This bit has no function, but read/write is enabled.	
$FR2_2$	Not used	0 1	This bit has no function, but read/write is enabled.	
$FR2_1$	Port $P2_1$ output structure selection bit	0	N-channel open-drain output	
		1	CMOS output	
$FR2_0$	Port $P2_0$ output structure selection bit	0	N-channel open-drain output	
		1	CMOS output	

Note 1: ”W” repserents write enabled.

Note 2: Unused bit while setting the port.

4.10 Port Output Structure Control Register FR3

Table 4.10 shows the bit configuration for Port ouptut format control register FR3.

Writing to register FR3 can be accomplished by TFR3A instruction after setting values to register A.

Table 4.10 Bit Configuration for Port Output Structure Control Register FR3

Port output structure control register FR3		at reset: 0000_2	at RAM back-up: state retained	W TFR3A
$FR3_3$	Port D_3 output structure selection bit	0	N-channel open-drain output	
		1	CMOS output	
$FR3_2$	Port D_2 output structure selection bit	0	N-channel open-drain output	
		1	CMOS output	
$FR3_1$	Port D_1 output structure selection bit	0	N-channel open-drain output	
		1	CMOS output	
$FR3_0$	Port D_0 output structure selection bit	0	N-channel open-drain output	
		1	CMOS output	

Note 1: “W” represents write enabled.

4.11 Port Output Structure Control Register C1

Table 4.11 shows the bit configuration for Port output structure control register C1.

Writing to register C1 can be accomplished by TC1A instruction after setting values to register A.

Table 4.11 Bit Configuration for Port Output Structure Control Register C1

Port output structure control register C1		at reset: 0000_2		at RAM back-up: state retained	W TC1A
$C1_3$	Port D_5 output structure selection bit	0	N-channel open-drain output		
		1	CMOS output		
$C1_2$	Port D_4 output structure selection bit	0	N-channel open-drain output		
		1	CMOS output		
$C1_1$	Port $P3_1$ output structure selection bit	0	N-channel open-drain output		
		1	CMOS output		
$C1_0$	Port $P3_0$ output structure selection bit	0	N-channel open-drain output		
		1	CMOS output		

Note 1: "W" represents write enabled.

4.12 Key-On Wakeup Control Register K0

Table 4.12 shows the bit configuration for Key-on wakeup contorl register K0.

Writing to register K0 can be accomplished by TK0A instruction after setting values to register A.

The contents of register K0 can be transfered to register A by TAK0 instruction.

Table 4.12 Bit Configuration for Key-On Wakeup Control Register K0

Key-on wakeup control register K0		at reset: 0000_2		at RAM back-up: state retained	R/W TAK0/TK0A
$K0_3$	Port $P0_3$ key-on wakeup control bit	0	Key-on wakeup not used		
		1	Key-on wakeup used		
$K0_2$	Port $P0_2$ key-on wakeup control bit	0	Key-on wakeup not used		
		1	Key-on wakeup used		
$K0_1$	Port $P0_1$ key-on wakeup control bit	0	Key-on wakeup not used		
		1	Key-on wakeup used		
$K0_0$	Port $P0_0$ key-on wakeup control bit	0	Key-on wakeup not used		
		1	Key-on wakeup used		

Note 1: "R" represents read enabled, and "W" represents write enabled.

4.13 Key-On Wakeup Control Register K1

Table 4.13 shows the bit configuration for Key-on wakeup control register K1.

Writing to reigster K1 can be accomplished by TK1A instruction after setting values to register A.

The contents of register K1 can be transfered to register A by TAK1 instruction.

Table 4.13 Bit Configuration for Key-On-Wakeup Control Reigster K1

Key-On-Wakeup Control Register K1		Reset: 0000_2		RAM Backup: Hold	R/W TAK1/TK1A
$K1_3$	Port $P1_3$ key-on wakeup control bit	0	Key-on wakeup not used		
		1	Key-on wakeup used		
$K1_2$	Port $P1_2$ key-on wakeup control bit	0	Key-on wakeup not used		
		1	Key-on wakeup used		
$K1_1$	Port $P1_1$ key-on wakeup control bit	0	Key-on wakeup not used		
		1	Key-on wakeup used		
$K1_0$	ポート $P1_0$ key-on wakeup control bit	0	Key-on wakeup not used		
		1	Key-on wakeup used		

Note 1: "R" represents read enabled, and "W" represents write enabled.

4.14 Key-On Wakeup Control Register K2

Table 4.14 shows the bit configuration for Key-on wakeup control register K2.

Writing to register K2 can be accomplished by TK2A instruction after setting values to register A.

The contents of register K2 can be transfered to register A by TAK2 instruction.

Table 4.14 Bit Configuration for Key-On Wakeup Control Register K2

Key-on wakeup control register K2		at reset: 0000_2		at RAM back-up: state retained	R/W TAK2/TK2A
$K2_3$	Port D_3 key-on wakeup control bit	0	Key-on wakeup not used		
		1	Key-on wakeup used		
$K2_2$	Port D_2 key-on wakeup control bit	0	Key-on wakeup not used		
		1	Key-on wakeup used		
$K2_1$	Port $P2_1$ key-on wakeup control bit	0	Key-on wakeup not used		
		1	Key-on wakeup used		
$K2_0$	Port $P2_0$ key-on wakeup control bit	0	Key-on wakeup not used		
		1	Key-on wakeup used		

Note 1: "R" represents read enabled, and "W" represents write enabled.

4.15 Key-On Wakeup Control Register L1

Table 4.15 shows the bit configuration for Key-on wakeup control register L1.

Writing to register L1 can be accomplished by TL1A instruction after setting values to register A.

The contents of register L1 can be transfered to register A by TAL1 instruction.

Table 4.15 Bit Configuration for Key-On Wakeup Control Register L1

Key-on wakeup control register L1		at reset: 0000_2		at RAM back-up: state retained	R/W TAL1/TL1A
$L1_3$	Ports $P1_0$-$P1_3$ return condition selection bit	0	Return by level		
		1	Return by edge		
$L1_2$	Ports $P1_0$-$P1_3$ valid waveform/ level selection bit	0	Falling waveform / “L” level		
		1	Rising waveform / “H” level		
$L1_1$	INT return condition selection bit	0	Return by level		
		1	Return by edge		
$L1_0$	INTpin key-on wakeup control bit	0	Key-on wakeup not used		
		1	Key-on wakeup used		

Note 1: “R” represents read enabled, and “W” represents write enabled.

5. Application Example of Port

5.1 Key Input by Key Scanning

After setting the N-channel open-drain output for the output format of port D, it is possible to build a key-matrix with an external circuit of keys by employing the pull-up transistor of port P0.

Overview: Keys for the external component

Specification: Outputs “L” level with port D, and performs input of 16 keys with port P0.

Figure 5.1 illustrates an example of the key-matrix circuit while Figure 5.2 depicts the key scan input timing.

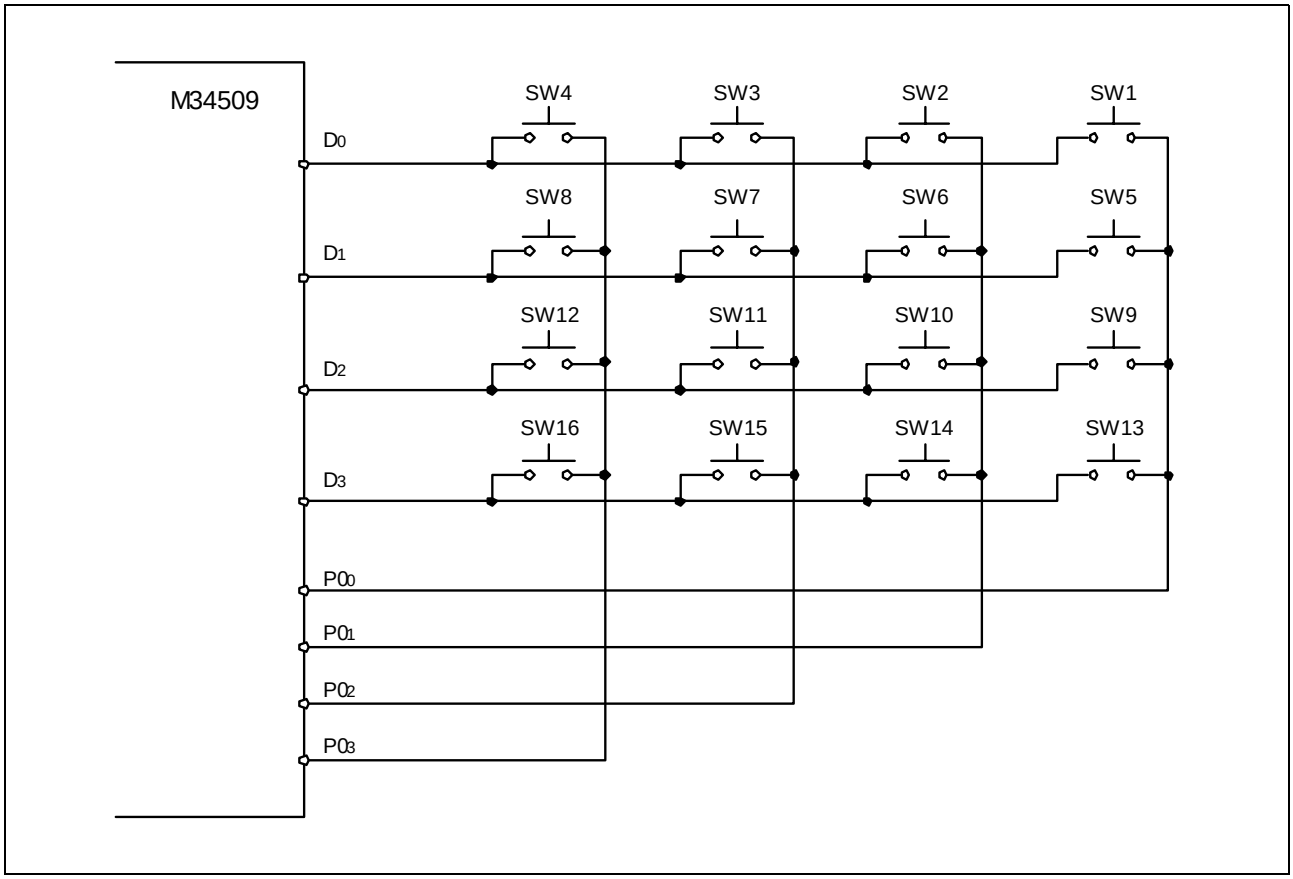
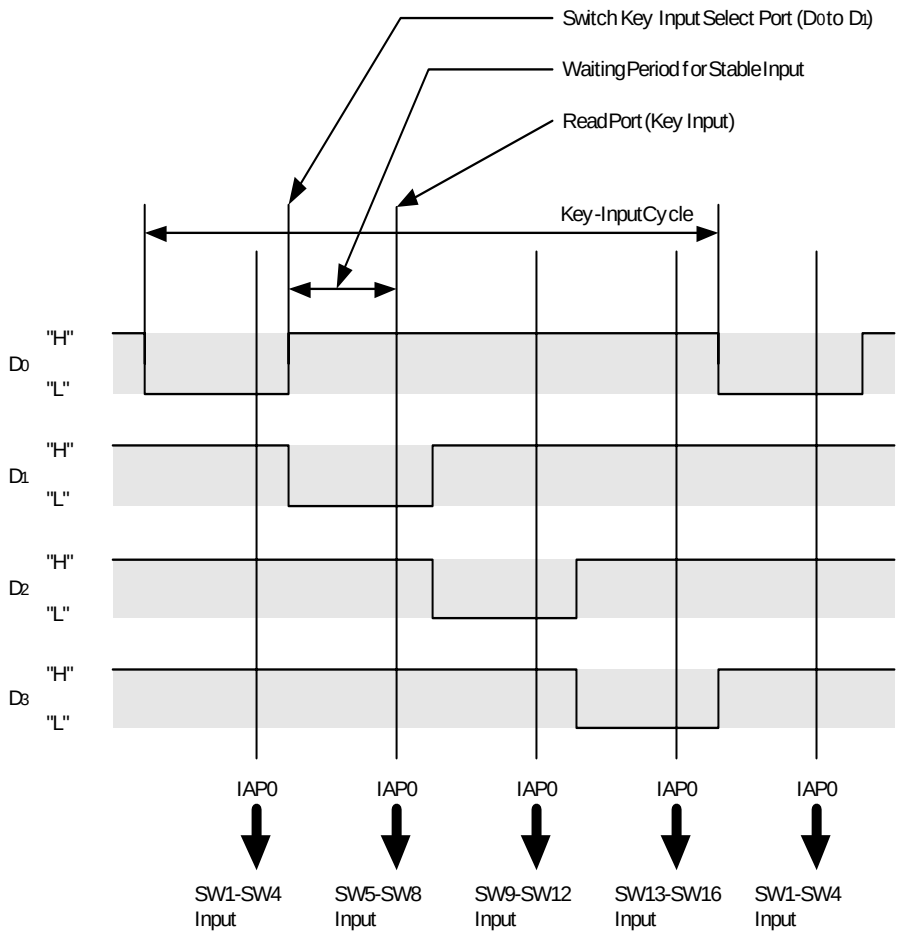


Figure 5.1 Key Matrix Circuit Example



Note: "H" output of Port D is "High Impedance".

Figure 5.2 Key Scan Input Timing

6. Reference Documents

Datasheet
4509 Group Datasheet

Before using this material, please visit our website to verify that this is the most updated document avaiable.

7. Our Official Website and Inquiry Contact

Renesas Technology Corporation Website
http://www.renesas.com/

Inquiry Contact
http://www.renesas.com/inquiry
csc@renesas.com

Revision History	4509 GroupInput/Output Port Application Note

Rev.	Date	Description	
		Page	Summary
1.00	July 01, 2006	—	First Edition Issued

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corporation product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corporation or a third party.
2. Renesas Technology Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corporation assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corporation by various means, including the Renesas Technology Corporation Semiconductor home page (http://www.renesas.com).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corporation is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corporation for further details on these materials or the products contained therein.