WHAT IS A ZERO DELAY BUFFER?

A zero delay buffer is a device that can fan out one clock signal into multiple clock signals, with zero delay and very low skew between the outputs. This device is well-suited for a variety of clock distribution applications requiring tight input-output and output-output skews. A simplified diagram of a zero delay buffer is shown in figure 1. A zero delay buffer is built with a PLL that uses a reference input and a feedback input. The feedback input is driven by one of the outputs. The phase detector adjusts the output frequency of the VCO so that its two inputs have no phase or frequency difference. The PLL control loop zero delay is achieved by aligning phase between input clock and output clock.
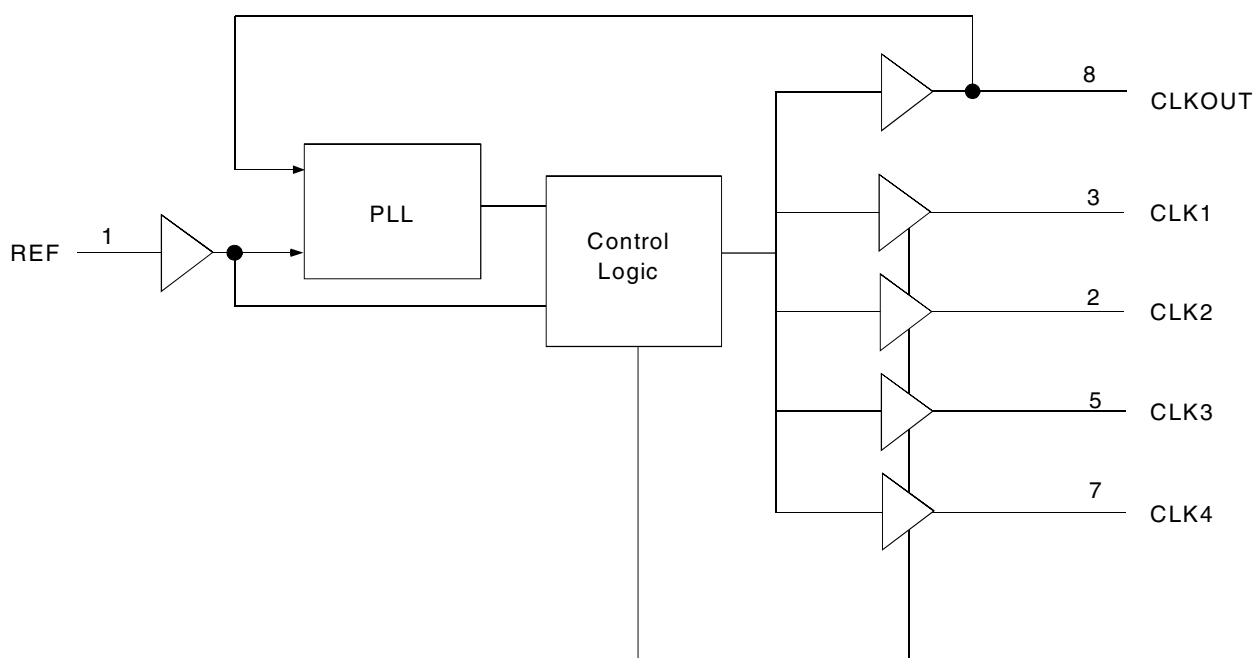
WHAT IS THE IDT2305, IDT2308 AND IDT2309?

The IDT2305 is high speed phase lock loop (PLL) clock buffer. IDT2305 accepts one reference input and drives out five low skew clocks.
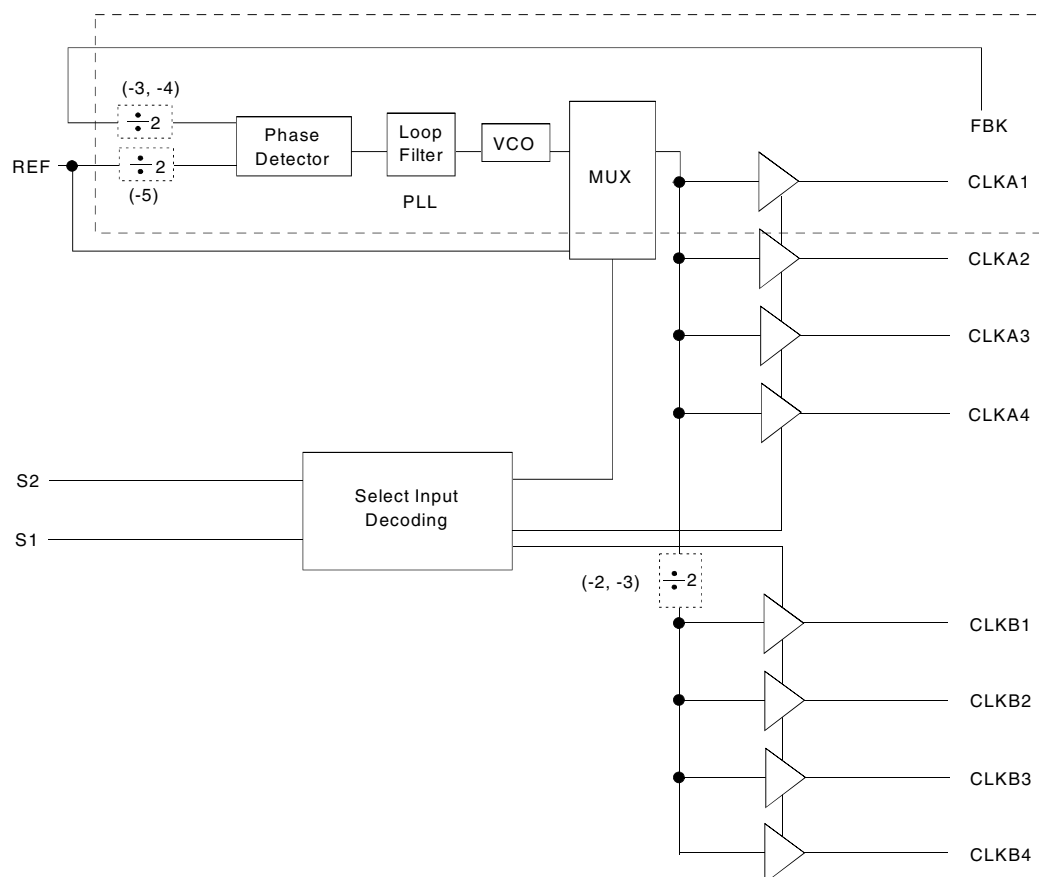
The IDT2308 is a high-speed phase-lock loop (PLL) clock multiplier. It is designed to address high speed clock distribution and multiplication applications. IDT2308 has two banks of four outputs, each controlled by two select addresses. By proper selection of input addresses, one or both banks can be put in tri-state mode. IDT2308 is available in six unique configurations for both prescaling and multiplication of the input REF Clock. The PLL is closed externally to provide flexibility by allowing the user to control the delay between the input and output clocks.

The IDT2309 is a 16-pin version of the IDT2305. IDT2309 accepts one reference input and drives two banks of four low skew clocks. All parts have on-chip PLLs which lock to an input clock on the REF pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad.
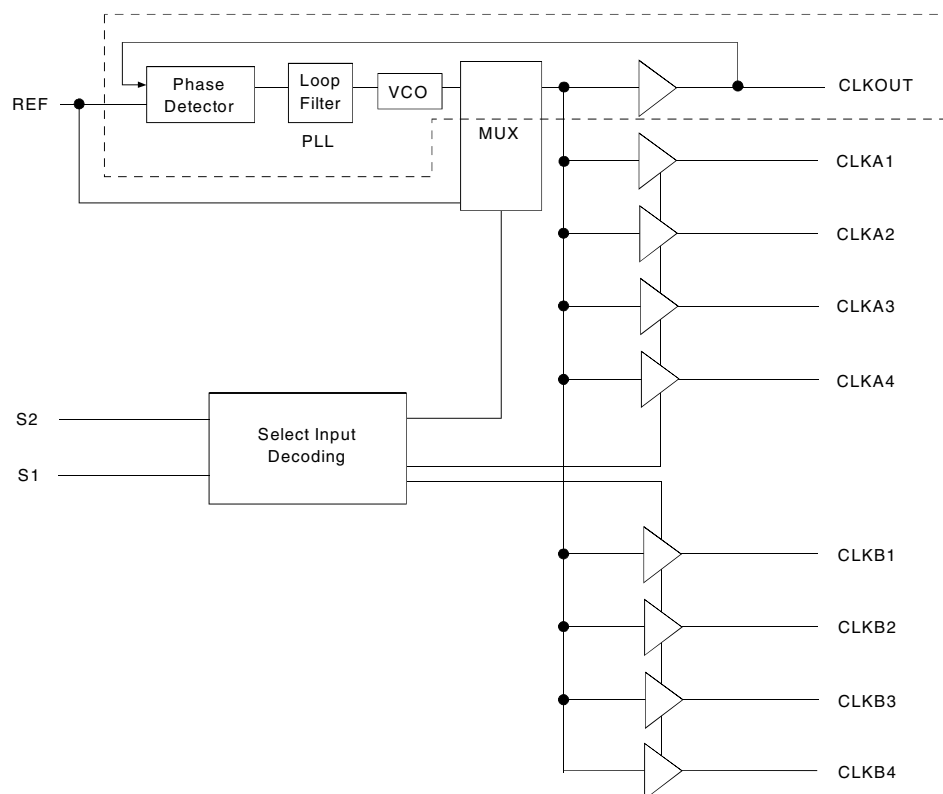
BLOCK DIAGRAM FOR 2305

DSC-5951/10

BLOCK DIAGRAM FOR 2308

BLOCK DIAGRAM FOR 2309

FUNCTION TABLE - 2308 [1]

S2	S1	CLKA	CLKB	Output Source	PLL Shut Down
L	L	Tri-State	Tri-State	PLL	Y
L	H	Driven	Tri-State	PLL	N
H	L	Driven	Driven	REF	Y
H	H	Driven	Driven	PLL	N

NOTE:
1. H = HIGH Voltage Level
    L = LOW Voltage Level

AVAILABLE OPTIONS - 2308

Device	Feedback From	Bank A Frequency	Bank B Frequency
IDT2308-1	Bank A or Bank B	Reference	Reference
IDT2308-1H	Bank A or Bank B	Reference	Reference
IDT2308-2	Bank A	Reference	Reference/2
IDT2308-2	Bank B	2 x Reference	Reference
IDT2308-3	Bank A	2 x Reference	Reference or $\overline{\text{Reference}}$[1]
IDT2308-3	Bank B	4 x Reference	2 x Reference
IDT2308-4	Bank A or Bank B	2 x Reference	2 x Reference
IDT2308-5H	Bank A or Bank B	Reference/2	Reference/2

NOTE:
1. Output phase is indeterminant (0° or 180° from input clock).

REF to CLKA/CLKB Delay vs. Output Load Difference Between CLKA/CLKB Pins

Output Load Difference Between CLKA/CLKB Pins (pF)

ZERO DELAY AND SKEW CONTROL - 2308

To close the feedback loop of the 2308, the FBK pin can be driven from any of the eight available output pins. The output driving the FBK pin will be driving a total load of 5pF plus any additional load that it drives. The relative loading of this output (with repect to the remaining outputs) can adjust the input-output delay.

For applications requiring the zero input-output delay, all outputs including the one providing feedback should be equally loaded. If input-output delay adjustments are required, use the Output Load Difference chart above to calculate loading differences between the feedback output and remaining outputs. Ensure the outputs are loaded equally for zero output-output skew.

FUNCTION TABLE - 2309[1]

S2	S1	CLKA	CLKB	CLKOUT[1]	Output Source	PLL Shut Down
L	L	Tri-State	Tri-State	Driven	PLL	Y
L	H	Driven	Tri-State	Driven	PLL	N
H	L	Driven	Driven	Driven	REF	Y
H	H	Driven	Driven	Driven	PLL	N

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
2. This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between REF and the output.

ZERO DELAY AND SKEW CONTROL - 2305 AND 2309

For zero output-to-output skew, all outputs must be equally loaded. The feedback loop doesn't dynamically adjust the skew between CLKOUT and the other outputs. All must have the same load on them to achieve zero output-to-output skew. ZERO DELAY BUFFER TIMING DIRAGRAMS shows how output loading affects output-to-output skew. Feedback is assumed to be driven by CLKOUT. If the outputs are less loaded than CLKOUT, they will lead. If other outputs are more loaded than CLKOUT, they will lag CLKOUT. CLKOUT and rest of the outputs all start at the rising edge at the same time.

All outputs should be uniformly loaded in order to achieve zero I/O delay. Since the CLKOUT pin is the internal feedback for the PLL, its relative loading can affect and adjust the input/output delay. For designs utilizing zero I/O delay, all outputs, including CLKOUT, must be equally loaded. Even if the output is not used, it must have a capacitive load equal to that on the other outputs in order to obtain true zero I/O delay.

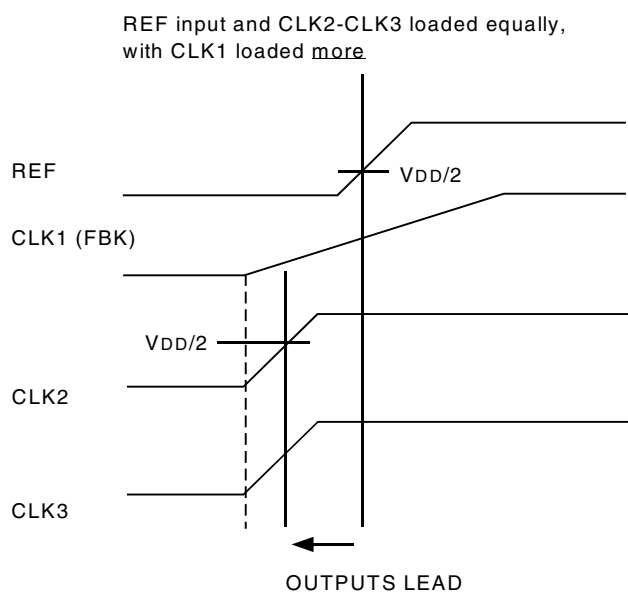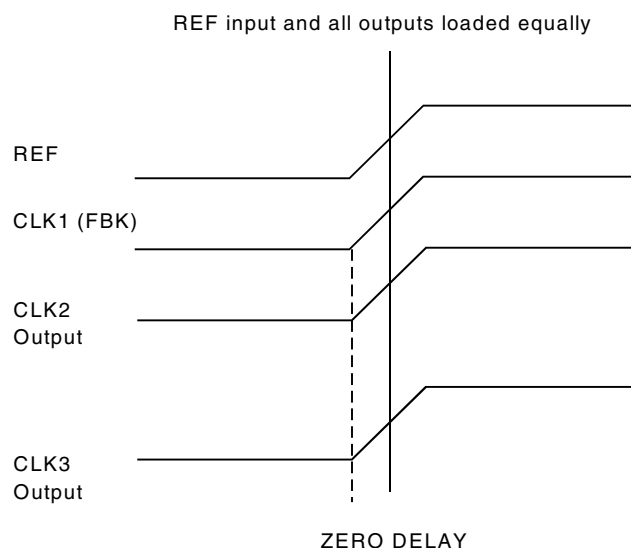## ZERO DELAY BUFFER TIMING DIAGRAMS - 2308

REF input and all outputs loaded equally

REF

CLK1 (FBK)

CLK2
Output

CLK3
Output

ZERO DELAY

REF input and CLK2-CLK3 loaded equally,
with CLK1 loaded _more_

REF

CLK1 (FBK)

$V_{DD}/2$

$V_{DD}/2$

CLK2

CLK3

OUTPUTS LEAD

FIGURE 1

REF input and CLK2-CLK3 loaded equally,
with CLK1 loaded _less_

REF

CLK1 (FBK)

$V_{DD}/2$

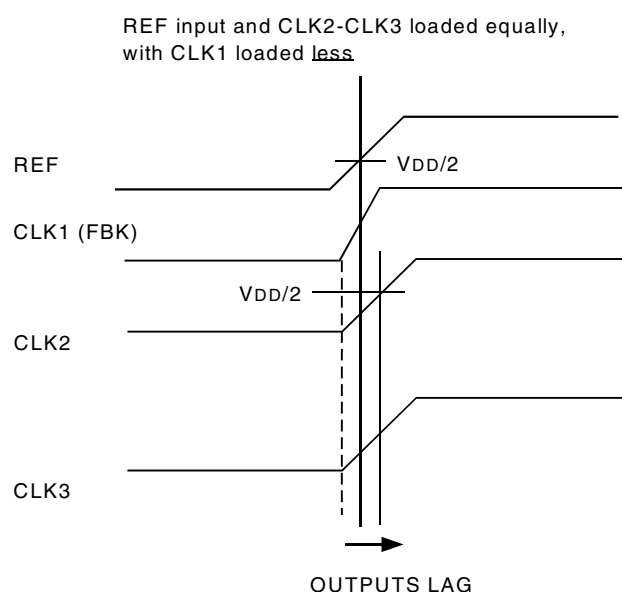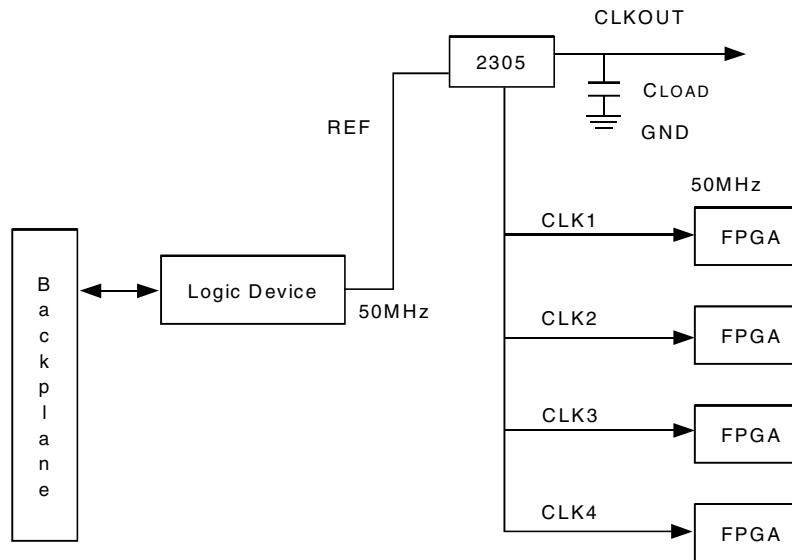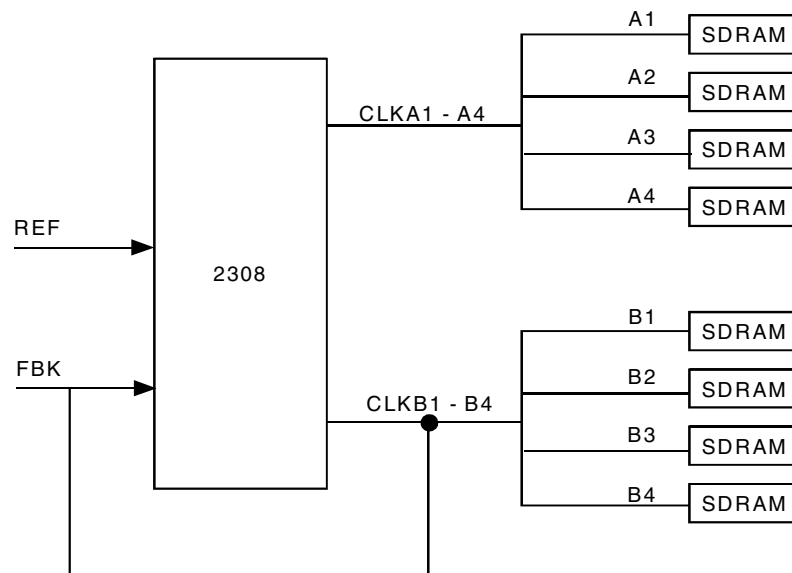$V_{DD}/2$

CLK2

CLK3

OUTPUTS LAG

FIGURE 2

In figure 1, CLK1 has a larger load. The PLL adjusts itself to position the zero skew between REF and the feedback pin. REF and CLK1 both cut across $V_{DD}/2$ at the same time. However, since the other output clocks are less loaded, their rise time is faster than CLK1. Consequently, they advance the REF by a certain amount that is controlled by the loads.

In figure 2, CLK1 has less load than other outputs. The PLL adjusts itself so that both REF and the feedback clock cross $V_{DD}/2$ at the same time. However, since the rest of the clocks have heavier loads, they are delayed by a certain amount that is controlled by the loads.

APPLICATIONS

Example for 2305 Zero Delay Buffer

Example for 2308 Zero Delay Buffer

POWER DOWN

The 2305, 2308, and 2309 provide auto power down features that shut off the PLL, tri-state outputs, and place the device into a low current state if the reference clock stops. The power down mode can also be entered by tristating the input reference driver and allowing the internal pull down resistor to pull the input low.

LEAD OR LAG ADJUSTMENTS

Lead or lag adjustment can be achieved by the property of PLLs. The PLL senses the phase of the CLKOUT pin at a threshold of $V_{DD}/2$ and compares it to the REF pin at the same $V_{DD}/2$ threshold. All outputs start their transition at the same time (including CLKOUT). Changing the load on an output changes its rise time, therefore also changing how long it takes the output to get to $V_{DD}/2$ threshold. With the help of these properties, we can try to adjust the time when the output reaches $V_{DD}/2$ threshold relative to when the REF input reaches $V_{DD}/2$ threshold. The CLKOUT output cannot be adjusted. The outputs can lead by loading the CLKOUT more heavily than the other outputs and vice versa.

SUGGESTED LAYOUT RECOMMENDATIONS FOR 2305, 2308, AND 2309

For best performance, good supply decoupling is essential. Place decoupling capacitors as close to the V_{DD} and GND pins of the zero delay buffer as possible. In a noisy environment, adding a ferrite bead in series with the V_{DD} supply line to the zero delay buffer will help. Decoupling capacitors should be low inductance surface mount ceramic types. Their electrical value is not critical; any value within the range 0.01uF to 0.1uF is suitable. To use two paralleled capacitors, use different electrical values for each in order to minimize the effects of any parasitic resonance between the trace inductance and the decoupling capacitors.

Dedicate one layer of the PCB to be ground plane, and connect all GND pins directly to this ground plane with vias placed as close as possible to the package pins. Ensure that the device which generates the REF input to the zero delay buffer is also connected to the ground plane with a via close to its GND pin, and that the devices driven by the zero delay buffer are connected to the ground plane with a via close to their GND pins.

Keep all I/O traces as short as possible. These are actually transmission lines, and unless the user has the luxury of being able to add a terminating resistor at the load end, the waveform will be progressively degraded by reflections from the end of the trace as the trace length is increased. If timing skew between outputs is more important than waveform integrity, equalize the trace lengths from each zero delay buffer output to its load, even if that means increasing the length of some traces. If the phase error between the REF input and the output is important, ensure that all outputs are loaded equally. Note that the FBK input capacitance will be added to whichever output is used for feedback.

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