ESD CONSIDERATIONS IN HIGH SPEED CIRCUITS

APPLICATION NOTE AN-123

By Stanley Hronik

INTRODUCTION

The primary cause of component failure in high speed logic circuits is electrostatic discharge (ESD)[1]. ESD can be encountered during improper device or board handling, through improperly designed interfaces, or if lightning or other phenomena causes a large voltage spike on a device interface. The industry has adopted standards and methods for component handling, system design, and component design which avoid many of the potential problems with ESD.

When devices are damaged by static electricity, the affected devices may cease to function, exhibit parameter degradation, or demonstrate high failure rates. In all situations the only repair is the replacement of the damaged component.

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ESD MODELS

In order to establish industry standards and provide uniformity between manufacturers on ESD ratings, models have been developed for testing devices under closely controlled conditions in ESD simulated environments. The first model is the Human Body Model which is designed to simulate the high impedance contact made when touching components with the hand or in similar situations. The second model is the Machine Model which simulates a much lower contact impedance as may be experienced in a component handler or similar situation where the device contacts are touching other metal. The third model is the Charged Device Model that simulates passing components between charge levels as may happen when a component is dropped from a statically charged storage tube to a grounded surface.

Human Body Model

The human body model, the model most often referred to in component data sheets when an ESD rating is given, is shown in Figure 1. The model consists of a voltage source that charges a 100pF capacitor. When the capacitor is at full charge, the capacitor is then discharged through a 1500Ω current limiting resistor into the device under test. The test is conducted with the device under test connected in the following configurations:

- ***All pins with respect to ground.*** Terminal B is connected to all device ground pins. Terminal A is connected to each non ground pin individually and the test is run for each pin. All other pins are open.
- ***All pins with respect to power.*** The test is repeated except terminal B is connected to all power (Vcc) pins. If there is more than one type of power supply (e.g. two voltage levels), each group of power pins is connected to terminal B independently. All other pins are open.
- ***Pins with respect to others on the same interface.*** The test is repeated except terminal B is connected to all other pins with a name similar to the one under test. e.g. If a pin on an output port is being tested, all other pins in the same port are connected to terminal B. All other pins are open.

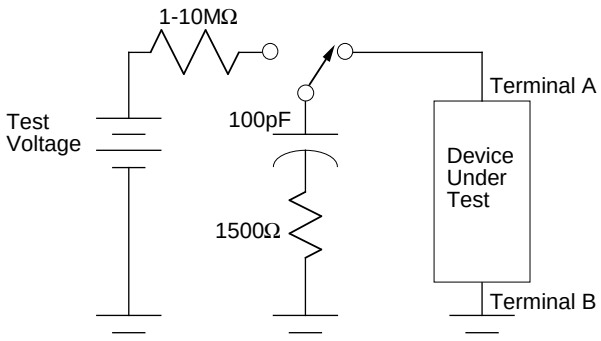

Figure 1. Human Body Model for ESD testing.

The tests are conducted with the device receiving three positive voltage pulses and three negative voltage pulses in each configuration. All component configurations must be able to withstand the test voltage for the component to be rated at the test voltage. Component damage can determined by the failure to pass any component test, but is usually exhibited by excessive leakage currents.

Machine Model

The Machine Model as shown in Figure 2 is similar to the Human Body Model except the Machine Model contains a larger capacitor and there is no series resistor to limit the current levels. With the higher current levels in the Machine Model, most components will break down at much lower test voltages than with the Human Body Model.

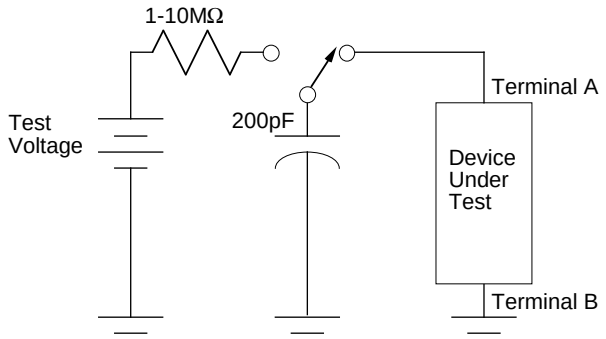

Figure 2. Machine Model for ESD testing.

Charged Device Model

The Charged Device Model, as shown in Figure 3, statically charges the component with a high voltage power supply through the 500MΩ resistor to the test voltage with the connection to the 1 Ω resistor open. When fully charged, the connection to the voltage source is broken and the connection to ground is made through the 1 Ω resistor. The test can be conducted between any two device pins or using the same pin for both the charge and discharge path. The 1Ω resistor allows the connection of a 50Ω scope probe to view the output waveform and measure the current levels. The current levels are determined by the capacitance levels of the device under test.

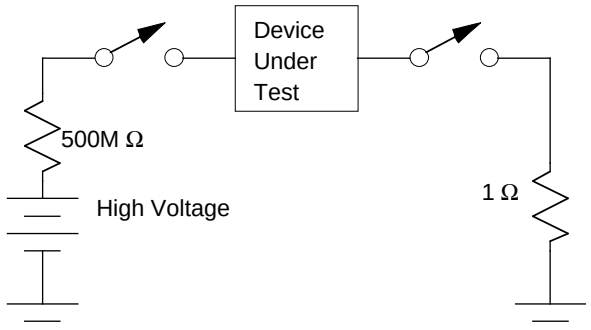

Figure 3. Charged Device Model for ESD testing.

ESD Rating Classes

The ESD rating classes are defined in Mil-Std-883C, Method 3015.7 and are as follows using the human body model:

ESD Failure Thresholds
Class 1 -- 0 volt to 1999 volts
Class 2 -- 2000 volts to 3999 volts
Class 3 -- 4000 volts and above

ESD RATING OF IDT LOGIC COMPONENTS

The ESD rating levels of IDT Logic Components are achieved through the integrity of the array on which the parts are built. All of IDT's newer arrays have class 2 ESD protection (>2000V human body model, >200V machine model). To achieve and guarantee class 2 levels, the ESD breakdown level on newer logic components is typically 3500 - 4000 volts human body model. IDT Logic Components which are guaranteed to have class 2 ESD ratings typically have a note listed in the FEATURES section of the data sheet as follows:

- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0).

The "Absolute Maximum Ratings" table in IDT data sheets lists the maximum voltages IDT Logic Components can withstand for extended periods. Since ESD voltages exceed those, exposure to ESD will cause damage to the device if the voltages are extreme, if the charge density is too high, or if the component is repeatedly exposed to high voltage levels. Exposure to ESD can have cumulative effects and eventually cause breakdowns, even if the component is rated for the exposure voltage.

ESD Structure in IDT Logic Components

The ESD rating level on IDT Logic Components is achieved through the device technology. Various models show what may happen under several ESD situations. Since ESD is unpredictable in its intensity, source, polarity, and discharge path, the models represent idealized situations and may or may not represent the effects of selected situations.

IDT Logic Components contain various pin and device dependent ESD structures. A partial model of these ESD structures is shown in Figure 4. The clamp diodes on the component inputs and outputs serve as the primary bypass paths for ESD charge currents. If an ESD charge forward biases one of the clamp diodes, the clamp diode drains off the excess charge and relieves the charge voltage. Ideally this is done without damaging the component. The source impedance, lead inductance, input capacitance and silicon structure all serve to protect the component from ESD damage.

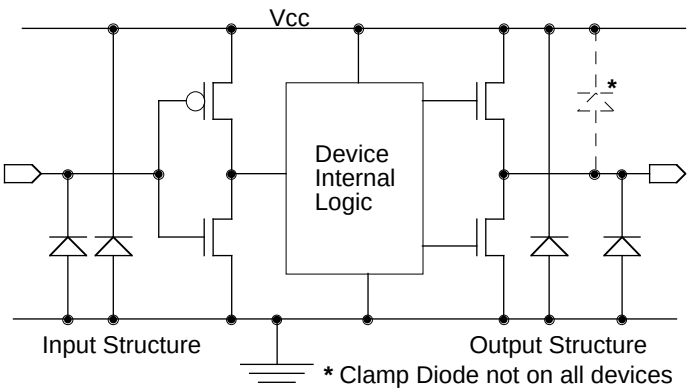

Figure 4. Clamp diode arrangement on IDT Logic Components.

There are many arrangements where a static charge would reverse bias the clamp diodes in the model and have no apparent conductive path for release of the charge. When this happens the component will start to avalanche, providing a low impedance path for the discharge of the static buildup. The avalanche condition of an IDT Logic Component is modeled in Figure 5 as a zener diode along with the models of other circuit elements. In this figure the static charge is represented by a charged capacitor with the amount of charge strictly dependent upon the charge source and conditions. The resistor represents the source/contact resistance or impedance between the charge and the component.

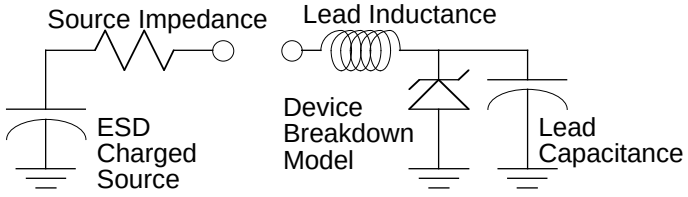

Figure 5. Partial model of the discharge of ESD through a component

The voltage at which the component will avalanche can be any voltage over the absolute maximum rating of the component (typically 7 volts), but will usually occur between 10 volts and 20 volts. Figure 6 shows the effects of the clamp diodes on the V/I curves of a typical IDT Logic Component. If a component enters an avalanche condition (shown as breakdown) or forward biases a clamp diode, this is potentially a very damaging situation that the component can withstand for very short periods only. Causing the component to avalanche for extended periods (beyond a few ns) or subjecting the component to repeated avalanche conditions will cause the component to fail.

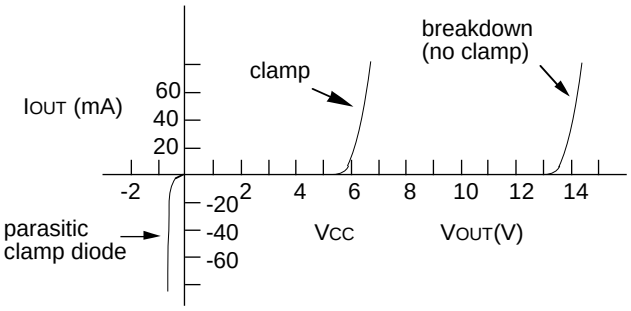

Figure 6. Typical input and output (when 3-state) impedance of IDT Logic Components.

COMPONENT ESD VULNERABILITY

During the expected life of a component, the device will pass through various stages of component handling, manufacturing processes and usage. At these stages differing levels of ESD exposure will be seen.

Loose Components

Loose components which have not been installed on circuit boards are in their most vulnerable condition relative to ESD damage. An ESD strike on a loose component is likely to strike an isolated pin and use a second isolated pin as a return path, making a direct hit with no bypass, isolation, parallel routing or other surge mitigating conditions. Under this situation it is very easy to develop a surge level that will damage even well designed components with excellent ESD protection.

Board and System Assemblies

Once assembled into circuit boards, the devices usually will be connected with other components on a substrate making multiple contacts between pins. In a circuit board the component Vcc and GND pins have been firmly attached to the power and ground planes of the board which will directly tie them to the decoupling capacitors and other board components. This configuration will mitigate the effects of static to a large extent on the Vcc and GND pins.

The input and output pins of a component on a circuit board are not as protected as the Vcc and GND pins, but will have the loading of the circuit card itself including other components, board capacitance, connector capacitance and trace inductance. The loading of multiple pins tied together will increase the capacitance when ESD strikes, dampening the pulse. Multiple contacts tied together also allow the pulse to distribute itself, reducing the impact on any single device.

Devices are most prone to ESD damage when they are in their loose state, unassembled to a board.

DESIGNING FOR ESD ENVIRONMENTS

In situations where there are extended cable lengths, cables running outdoors, cables running long distances underground, or cables in any situation on or near an antenna where it is possible for lightning to strike and damage any device directly connected to the cable, special precautions must be taken against component ESD damage. Many other situations can produce lightning like conditions, among which are any high voltage systems, X-Rays, and nuclear weapons. Lightning voltage levels and charge currents are extreme and unpredictable, making it very difficult to design for general purpose lightning protection.

External Cable Connections

Many bus driver components are used in external system interfaces as peripheral drivers/receivers. In applications where logic components are directly connected to external devices, especially through cables, care should be taken to protect against ESD from interface handling. External cable interfaces should all be shielded with a grounded metal connector shroud which connects directly to the cable shield. The metal connector shroud will provide a first contact point for anyone or anything that happens to physically touch the interface. This is especially true when connecting two systems where the two grounds must be equalized. Through this contact, the static buildup can be discharged directly to the system ground through the connector shield without passing directly through a logic component.

Line Termination

By providing line termination on system interfaces, some ESD protection will be achieved. The presence of the additional termination components increases the input capacitance and provides alternate paths for ESD currents. A shunt termination with a 50 Ω resistor from every input to ground is beneficial, or the Thevenin configuration of Figure 7 will also help. One of the primary benefits of line termination is that device inputs or outputs which are floating will have a low impedance path to ground, draining off any ESD buildup that occurs.

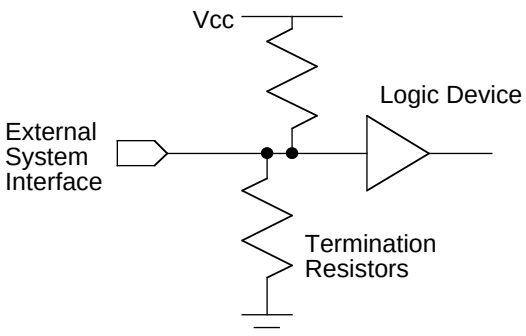

Figure 7. Adding termination resistors to external inputs or outputs helps protect against ESD damage.

Figure 8 shows a receiver circuit that protects against ESD in severe situations. This circuit withstands voltage levels far exceeding the class 3 specifications. During circuit layout it may be necessary to provide spark gaps and sufficient isolation to avoid arcing into sensitive circuitry. The diodes shown in Figure 8 will add capacitance which slows the incoming static pulse slightly, allowing it to drain off before damaging the comparator. It may be necessary to add additional capacitors to the input of the comparator if the ESD voltage levels are extreme.

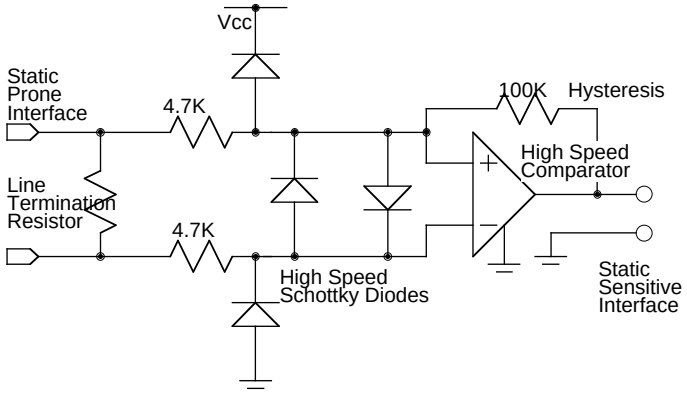

Figure 8. A receiver circuit for use in highly static prone situations.

Transmitter circuits which have continuously active, low impedance outputs are less sensitive than receiver circuits to ESD. Low impedance drivers allow current to pass, draining the static charge, without dissipating high levels of energy within the device. Transmitter circuits can be further protected by adding clamping diodes and resistances to the interface; however, good protection against static is difficult in transmitter circuits without increasing the drive impedance and severely limiting the transmitting capability of the circuit.

Transient Suppression Devices

In environments where cables may be running significant distances through static prone areas, another method of protecting device inputs and outputs from ESD damage is to use bypass components on all external interface pins. Several companies make bypass diodes which will shunt the charge around the logic component on the bus and protect the input/output. When designing an interface with one of these components, the designer must keep in mind that the path for the ESD may be from input signal to return path, from signal to ground (or Vcc), from signal to a different signal input, or any other combination. Figure 9 shows how a simple, single transient suppression device could be used to protect against damage from a signal to ground ESD pulse.

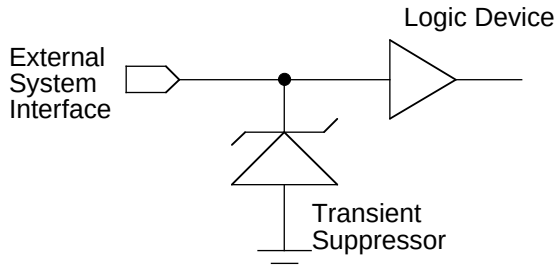

Figure 9. Using a transient suppresser on a device input.

Optocouplers

Optocouplers are excellent for protecting against ESD problems in situations where two systems are being linked in electrically hostile environments. Optocouplers allow ground isolation making it possible for systems to remain electrically neutral within themselves, even though they may be floating in a noisy electrical environment. In applications where the ground levels are uncertain, where strong electric fields exist, or where lightning, nuclear systems, X-ray machines or other pulse generators exist, optocouplers may be a solution.

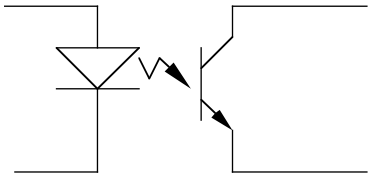

Figure 10. Optocouplers solve many ESD and grounding problems between systems.

Common Mistakes

Input and output impedances cannot be used to calculate current levels for ESD protection. The ESD calculations are for transient conditions and can not be accurately modeled as an input or output resistor on a component. A closer approximation of impedance is to assume the component is in an avalanche condition and is modeled like a zener diode. Lead inductance, device capacitance and alternative paths significantly complicate any model.

Adding series resistors without a bypass does not necessarily help protect against ESD damage. Any series resistor that could be added would be small relative to the impedances associated with a static charge and any effect it did have would simply slow the RC time constant and deliver a lower voltage for a longer time. The charge from an ESD hit is a quantity of charge that must be dissipated. For good ESD protection, the charge must bypass the device rather than pass through at a slightly slower rate.

Damaging levels of static are usually present, even when visible sparks are not seen. ESD problems are exacerbated by dry climate, heavy clothing, carpeting, lightning, large electric fields, long cables, poor grounds, untreated Styrofoam and innumerable other situations. No visible sparks does not mean that an ESD problem does not exist. Seeing sparks guarantees that a serious problem does exist.

CONCLUSIONS

ESD damage remains one of the primary causes of component failure. Recently great strides have been made in protecting components against damage; however, even the most robust of parts will not survive the huge current surge of an unmitigated static pulse. Most IDT Logic Components are ESD class 2, making IDT an industry leader in ESD protection. IDT Logic Components will survive the static levels found in most handling and interfacing situations if standard ESD procedures are followed. When used in a high level ESD environment, precautions must be made to protect the component from the current surges.

[1] ESD is also sometimes used as an acronym for Electro Sensitive Devices.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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