GreenPAK Macro Cell Example: Constructing additional DFF types

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Date: February 02, 2015

Introduction

D-type flip flops are used in many GreenPAK designs. Sometimes a user may need more of them than the available pre-configured DFF blocks in the GreenPAK IC.

Reference books can give a variety of solutions on how to construct DFF's. However, some are not efficient designs. The following is a collection of solutions with working examples using GreenPAK. Emphasis is on simplicity, and minimizing circuit resource usage.

From concept to simple examples

Using LUT's in the latch configuration. The first LATCH passes the logic level from the D input to the first LUT output if the C input is LOW. If the C input is HIGH, then the state of the first output doesn't change. (This corresponds to the LATCH cell function in a GPAK chip). The second LATCH operates just as the first LATCH does, but its C input is inverted. The first LATCH output is connected to the input of the second LATCH and their C inputs are connected to the same clock signal source (See Fig.1).

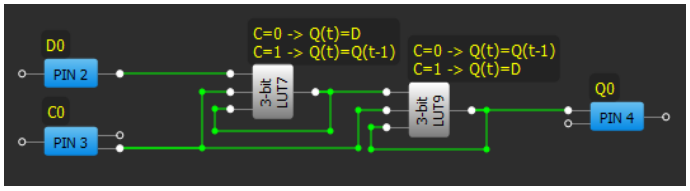

Figure 1. DFF based on LUT cells (DFF0)

This circuit does not use an edge detector or one-shot, which avoids those potential issues. Using only two 3-bit LUTs, this DFF is also simpler than what is typically offered in reference books. A variant of this simple DFF with the inverted output is shown in Fig.2.

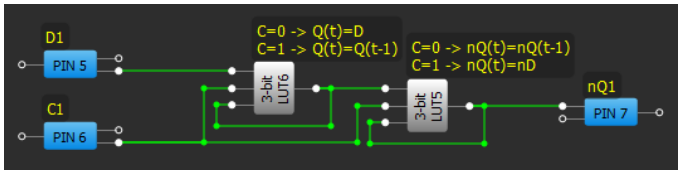

Figure 2. DFF with inverted output (DFF1)

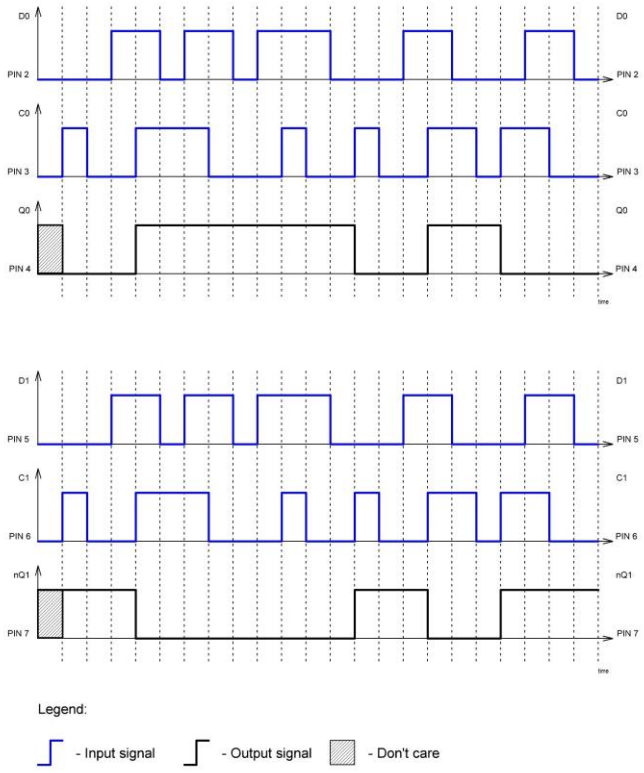

Figure 3. DFF0 and DFF1 timing diagram

The timing diagrams and functional waveforms for these DFF's are shown in Fig.3, 4.

Fig. 4. Waveform definition:

D0 – PIN#2 (D0)
D1 – PIN#3 (C0)
D2 – PIN#4 (Q0)
D3 – PIN#5 (D1)
D4 – PIN#6 (C1)
D5 – PIN#7 (nQ1)

DFF0 and DFF1 macro cells configuration can be found in Appendix 1.

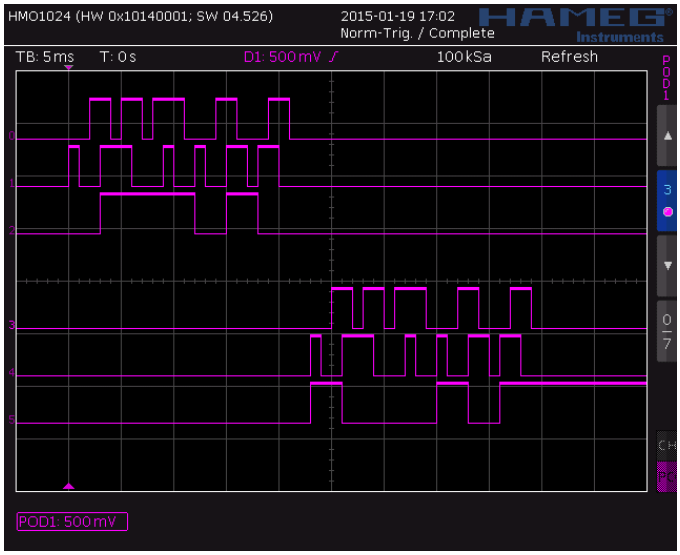

Figure 4. DFF0 and DFF1 functional waveforms

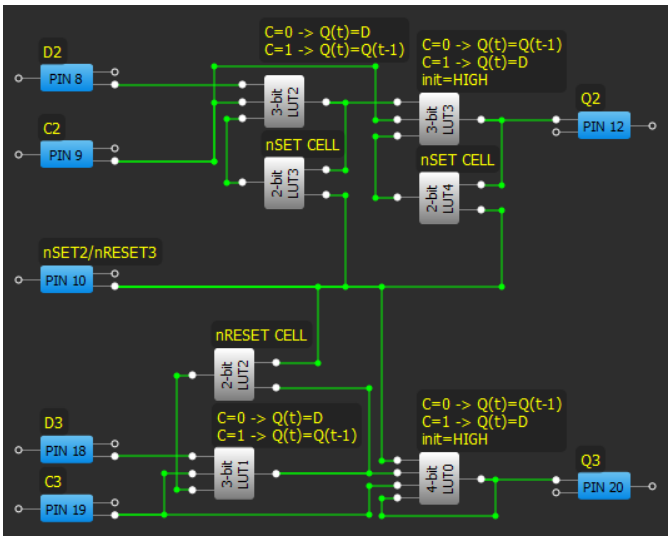

Figure 5. DFFs with nSET and nRESET input

DFF with nRESET or nSET input. MODE input in the DFF.

DFFs with nRESET or nSET are the type most commonly used in designs. We will look at how to construct them using LUT cells.

The schematic of the flip flop with nSET input (DFF2), and also with the nRESET input (DFF3) is shown In Fig. 5. There are small differences from the previous DFF0,1 versions. 2-bit LUTs are added to the feedback circuits of the first LATCH and the second LATCH.

DFF3 also utilizes a 4-bit LUT in making the second latch. Operation of these DFF's is as follows. A LOW level on the nSET input will set output of each LATCH HIGH and then the DFF2 output will be set HIGH. Similarly, a LOW on the nRESET input will set output of each LATCH LOW that will reset the DFF3 output. Timing diagrams for DFFs with nSET and nRESET inputs can be found in Fig. 6. Waveforms for these flip flops operation are shown in Fig. 7.

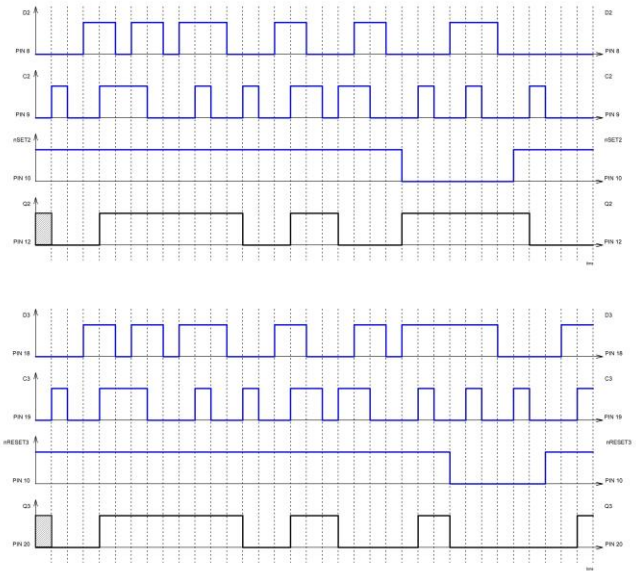

Figure 6. DFF2 and DFF3 timing diagram

Fig. 7. Waveform definition:

D0 – PIN#8 (D2)
D1 – PIN#9 (C2)
D2 – PIN#12 (Q2)
D3 – PIN#10 (nSET2/nRESET3)
D4 – PIN#18 (D3)
D5 – PIN#19 (C3)
D6 – PIN#20 (Q3)

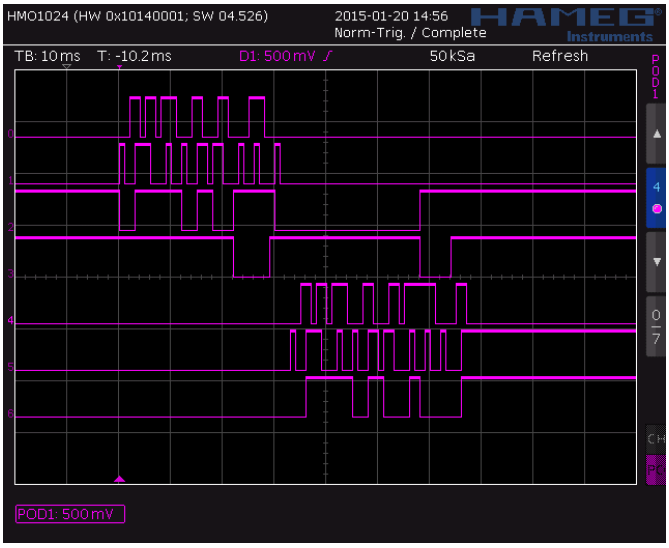

Figure 7. DFF2 and DFF3 functionality waveform

The previously described DFF0,1,2,3 examples are functional equivalents of preconfigured GreenPAK DFF cells. The following example will extend DFF functionality within GreenPAK (See Fig. 8). In this macro cell one additional input is added, a MODE input. MODE makes it possible to select whether DFF4 will be nSET or nRESET type input.

The nSET/nRESET input functions as nSET if the MODE input is HIGH, and nRESET if MODE input is LOW. Assignment of the nSET/nRESET PIN can be changed dynamically.

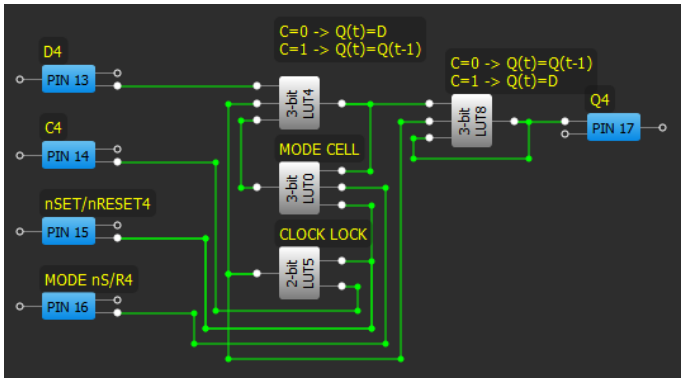

Figure 8. DFF4 with nSET/nRESET and MODE inputs

Also, the initial state of DFF4 depends on MODE input. The initial state will be HIGH if the MODE input is HIGH, and vice versa.

DFF4 functions a little differently, therefore we will review it in more detail. While the two latches (3-bit LUT4 and 3-bit LUT8) are familiar, the distinctions are in the feedback loop. MODE CELL (3-bit LUT0) controls the feedback.

When the nSET/nRESET PIN is HIGH, this cell shorts the feedback of the 3-bit LUT4 cell, and DFF4 functions in normal mode. If nSET/nRESET input is LOW, then the output of MODE CELL is set the same as the logic level on MODE nS/R4 input. Respective with MODE nS/R4 PIN, this action sets or resets the first latch. For the second latch this function is realized differently. When nSET/nRESET input is LOW, the signal from C4 input isn't passed to a CLOCK LOCK cell output, and a HIGH level is set on this output. As a result, on the output of the second latch the same logical level will be set, which is present on the output of the first latch. Such implementation option requires the minimum quantity of circuit resources. The timing diagram (Fig. 9) helps to understand the functionality of DFF4. Functional waveforms for DFF4 are shown in Fig. 10.

DFF2, DFF3 and DFF4 macro cells configuration can be found in Appendix 1.

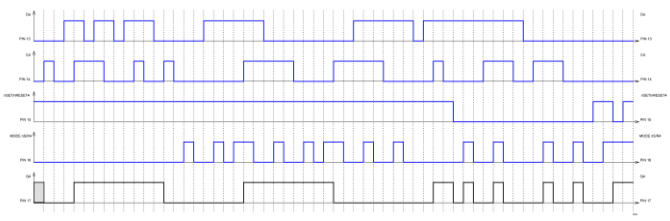

Figure 9. DFF4 timing diagram

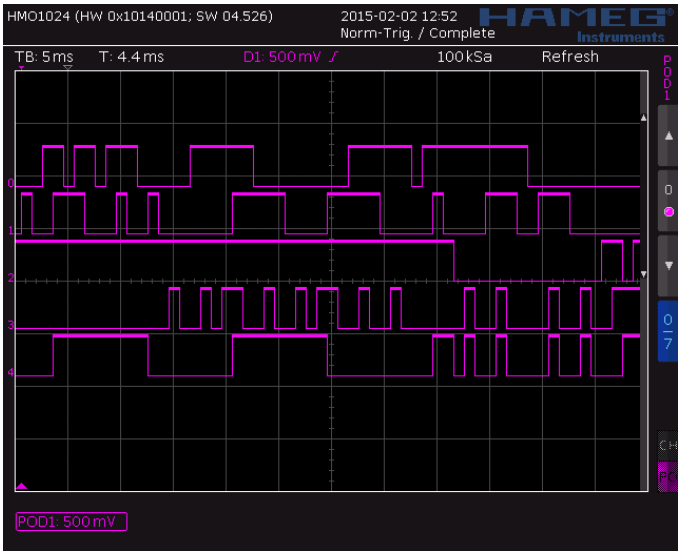

Figure 10. DFF4 functionality waveforms

Fig. 10. Waveform definition:

D0 – PIN#13 (D4)
D1 – PIN#14 (C4)
D2 – PIN#15 (nSET/nRESET4)
D3 – PIN#16 (MODE nS/R4)
D4 – PIN#17 (Q4)

Conclusion

The DFFs presented can be used in designs where additional flip flop cells are required. Flexibility and simplicity of the proposed circuits allow efficient adaptation to specific designs. Also, introduction of a dynamic nRESET/nSET mode circuit provides additional flexibility when using GreenPAK.

Appendix 1

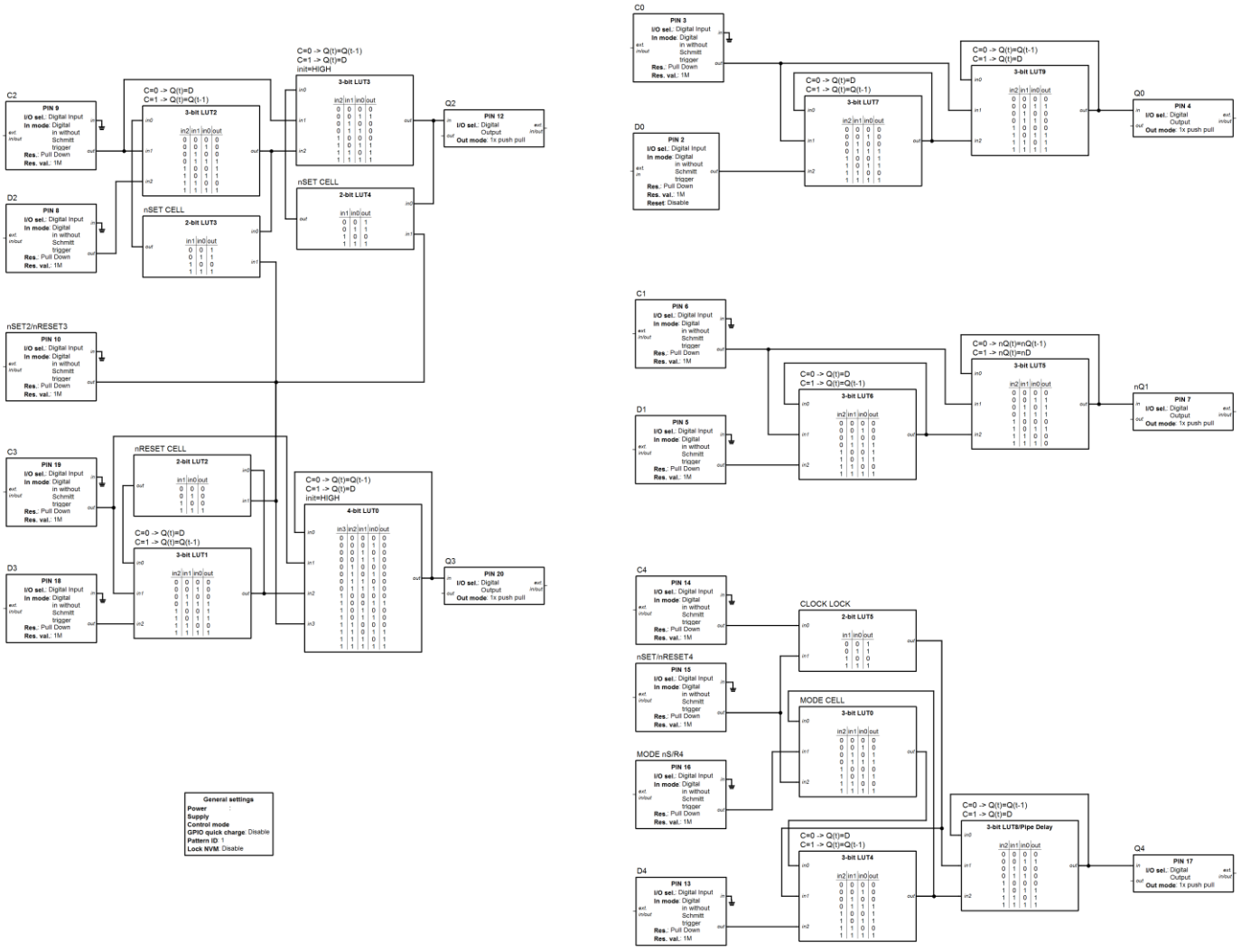

Figure 1.1. Block Diagram for Design

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