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Introduction

GreenPAK is a limited resource device that requires an efficient use of components in order to maximize the capability of the chip. One valuable way of maximizing efficiency is having the knowledge to flexibly use different components to perform the same function. This application note will cover a variety of ways to realize an edge detector circuit using a variety of blocks.

Edge Detectors

An edge detector circuit is a simple circuit with one input and one output. The circuit creates a short pulse when a defined edge, rising, falling, or both depending on the configuration, is detected. This application note will cover seven ways to create edge detectors.

2 LUTs

LUTs are the most common block on GreenPAK devices, so it is very useful to be able to create an edge detector with them. Figure 1 shows the proper circuit wiring create an edge detector.

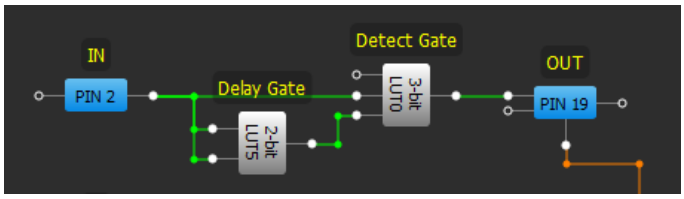

Figure 1. LUT Circuit

2-bit LUT4 creates a small delay because there is a delay created by the signal propagation through the gate. This delay is compared in 3-bit LUT7 against the input directly wired, which has essentially zero propagation time.

The short delay through 2-bit LUT4 causes a difference in logic on the input of the Detect Gate for a short period, which allows the Detect Gate to generate a short pulse. Figures 2 and 3 show the configuration of the LUTs.

2-bit LUT4 is configured as an AND gate with the gate's input going to both inputs IN0 and IN1. This configuration will generate the longest propagation delay. The Detect Gate (3-bit LUT7) determines if the edge detector detects rising, falling, or both edges. In this case it is a rising edge detector. See AN_1014 for a detailed analysis of using LUTs as edge detectors and their various configurations.

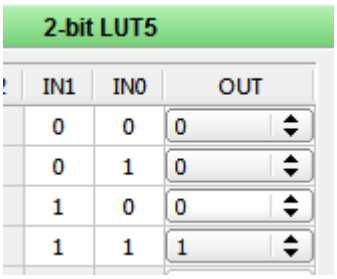

Figure 2. 2-Bit LUT5 Configuration

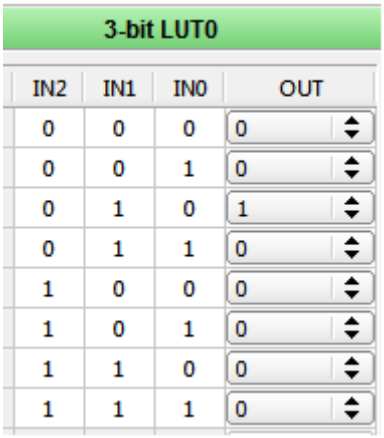

Figure 3. 3-Bit LUT0 Configuration

INV and LUT

The INV-LUT edge detector uses the exact same principle as the 2 LUTs edge detector configuration, except it uses an inverter as the delay. Figure 4 shows the circuit layout of the INV-LUT edge detector.

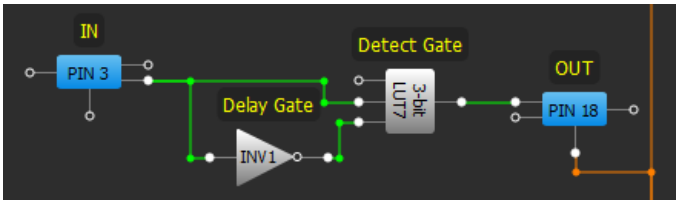

Figure 4. INV-LUT Circuit

The Detect Gate is the same as the Detect Gate of the LUT circuit, however the input is inverted due to the inversion from the Delay Gate. Figure 5 shows the configuration of the Detect Gate.

3-bit LUT7

IN2	IN1	IN0	OUT
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Figure 5. INV-LUT Configuration

DFF

The DFF edge detector circuit relies on the nRESET input on the DFFs. Some DFF's do not have the nRESET capability, so it is necessary to use a DFF with the nRESET input. Figure 6 shows the wiring off the DFF edge detector.

When the input has a rising edge, the high level from VDD is clocked into the D pin. Once the Q appears as a 1, nQ will become a 0, activating the nRESET and forcing the DFF back to zero. The propagation through nRESET causes a quick pulse on Q and prepares the DFF for the next edge. This is limited by the capability of the DFF as it can only detect rising edges.

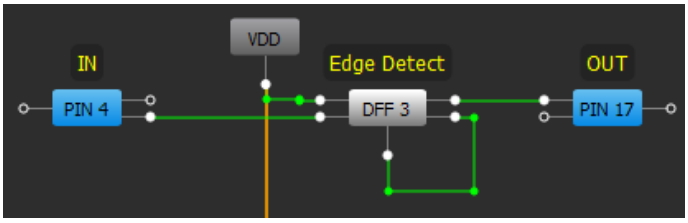

Figure 6. DFF Circuit

P DLY

The Programmable Delay (P DLY) has a built in Edge Detection feature. The P DLY can be used as a rising, falling or both edge detector, or simply as a short delay function. Its circuit is shown in Figure 7.

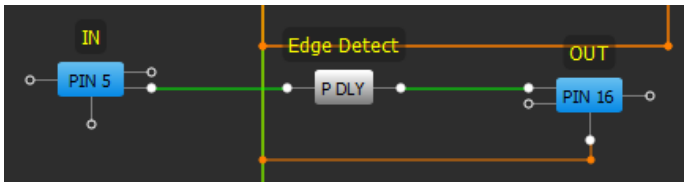

Figure 7. P DLY Circuit

The P DLY is configured through the properties section in GreenPAK designer. Figure 8 shows the interface to choose your settings.

There are three different drop down menu options: Mode, Delay, and Output mode.

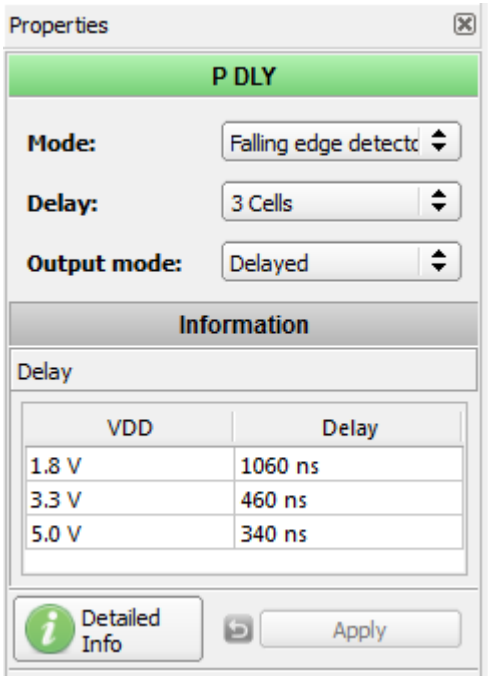

Figure 8. P DLY Properties Window

- Mode: selects which edge will generate an output pulse or if the P DLY will act as a simple delay block.
- Delay: selects either the length of the edge detector output pulse or the length of delay if in delay mode. The Information Table computes the relevant values in real time.
- Output mode: selects if the output is delayed. This delay is in the hundreds of ns varied by the VDD voltage and is independent from the Mode and Delay options.

DLY

On the GreenPAK3, there is one counter with an edge detector output: CNT6/DLY6. In the properties window, the CNT can be configured to output a pulse on rising, falling, or both edges.

Figure 9 shows the EDGE DETECT pin is the bottom right pin of CNT6/DLY6. The block must be configured as a Delay in the properties tab to access the Edge Detect pin.

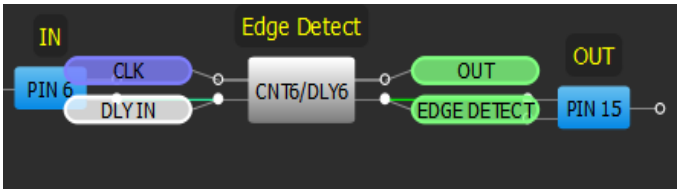

Figure 9. CNT6/DLY6 Circuit

Filter

The Filter design works on the same principle that the LUT edge detectors work, but generates a delay by using the filter block instead of the propagation time through a gate. Figure 10 shows the circuit configuration.

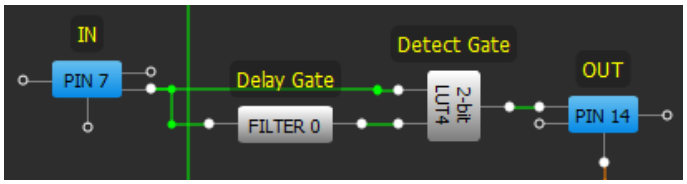

Figure 10. Filter Circuit

The filter's delay time is essentially the edge detector's output pulse width; the properties tab displays the length of the FILTER delay for common VDD voltages.

Pipe Delay

The Pipe Delay edge detector works essentially the same way as the DFF edge detector circuit. The nRESET is controlled by an inverter and the delay time is based on the propagation time through the inverter. Figure 11 shows the wiring of the circuit.

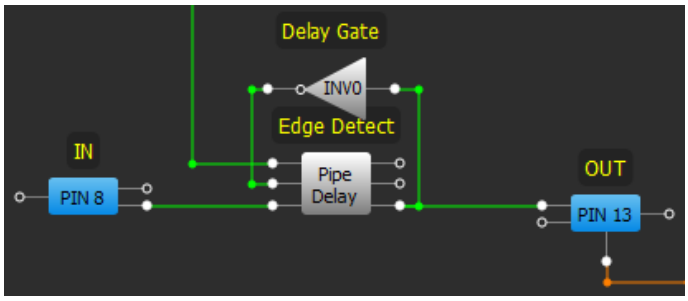

Figure 11. Pipe Delay Circuit

Edge Detector Differences

Since there are a variety of ways to make edge detectors, there are slight differences in the outputs of each edge detector. Two of the edge detector configurations can only detect rising edges, while the others can detect rising, falling or both. Figure 12 and 13 show the relative differences between the edge detectors. PDLY is set to 1 cell of delay. Table 1 shows the various edge detectors and some information about each configuration.

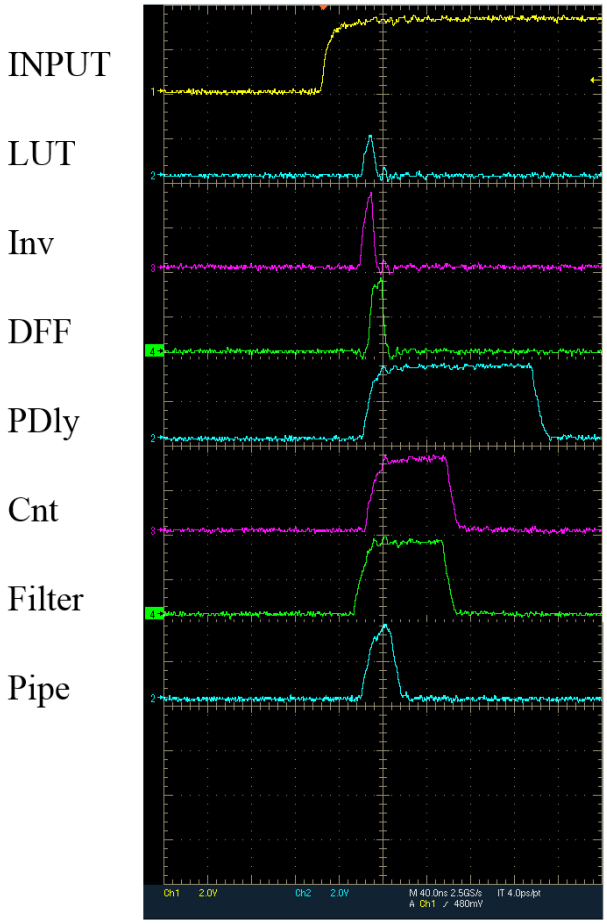

Figure 12. Rising Edge Response Waveforms

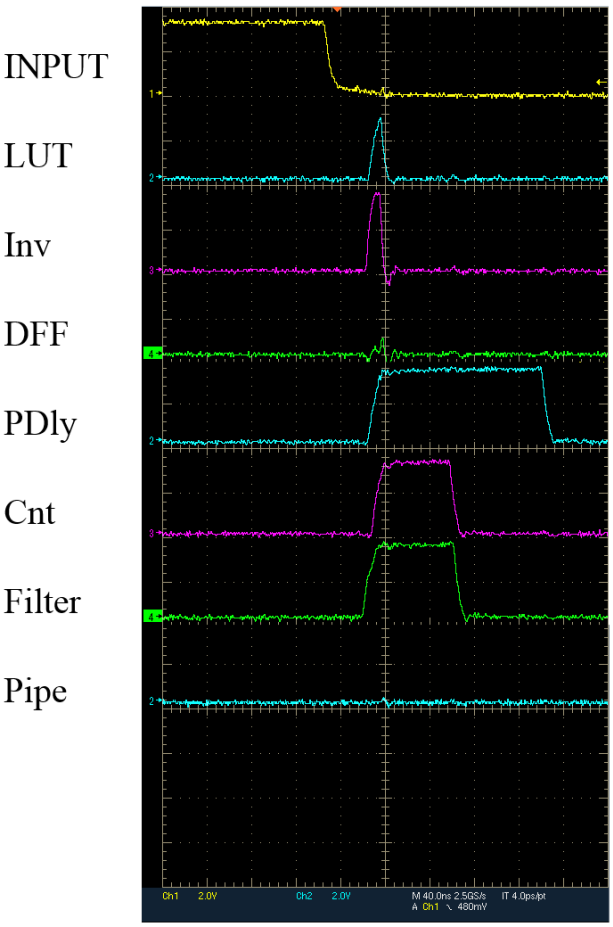

Figure 13. Falling Edge Response Waveforms

Edge Detector	Average Pulse Width (ns) at 3.3V	Rising Edge Only	Falling Edge Only	Both Edges	Max Number: SLG46721	Max Number: SLG46722
LUTS	15	X	X	X	9	8
Inverter	15	X	X	X	2	0
DFF	14	X			2	4
P DLY	155	X	X	X	1	1
CNT	70	X	X	X	1	1
Filter	75	X	X	X	2	2
PIPE	25	X			1	1

Table 1. Edge Detector Variations

Conclusion

It has been shown that by using components in various ways, numerous edge detector designs are successfully implemented and more fully utilizing the resources available.

Related Files

Programming code for **GreenPAK Designer**.

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