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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SY*-A011A/E	Rev.	1.00
Title	Revised information of S124 User's Manual from Rev.1.10		Information Category	Technical Notification		
Applicable Product	Renesas Synergy™ S1 Series S124	Lot No. All lots	Reference Document	S124 User's Manual: Microcontrollers, Rev.1.10		

1. 30.8.8 ADHSC Bit Rewriting Procedure

   [Before]

   Before changing the A/D Conversion Select bit (ADCSR.ADHSC) from 0 to 1 or from 1 to 0, the ADC14 must be in the standby state. Use the following procedure to modify the ADCSR.ADHSC bit. After the Sleep bit (ADHVREFCNT.ADSLP) is set to 0, wait for at least 1 ms then start the A/D conversion.

   [After]

   Before changing the A/D Conversion Select bit (ADCSR.ADHSC) from 0 to 1 or from 1 to 0, the ADC14 must be in the standby state. Use the following procedure to modify the ADCSR.ADHSC bit. After the Sleep bit (ADHVREFCNT.ADSLP) is set to 0, wait for at least 1 µs then start the A/D conversion.

2. Table 41.48 A/D internal reference voltage characteristics

   [Before]

   Conditions: VCC = AVCC0 = VREFH0 = 2.0 to 5.5 V*1

Item	Min	Typ	Max	Unit	Test conditions
Internal reference voltage input channel*2	1.36	1.43	1.50	V	-

   [After]

   Conditions: VCC = AVCC0 = VREFH0 = 2.0 to 5.5 V*1

Item	Min	Typ	Max	Unit	Test conditions
Internal reference voltage input channel*2	1.36	1.43	1.50	V	-
Sampling time	5.0	-	-	µs	-

3. 7.2.7 Voltage Monitor 1 Circuit Control Register 0 (LVD1CR0)

   [Before]

   RN bit (Voltage Monitor 1 Reset Negate Select)

   If the RN bit is to be set to 1 (negation follows a stabilization time after assertion of the LVD1 reset signal), set the LOCOCR.LCSTP bit to 0 (the LOCO operates). Additionally, if a transition to software standby is to be made, the only possible value for the RN bit is 0 (negation follows a stabilization time after VCC > Vdet1 is detected). Do not set the RN bit to 1 (negation follows a stabilization time after assertion of the LVD1 reset signal) in this case.

[After]

RN bit (Voltage Monitor 1 Reset Negate Select)

If the RN bit is to be set to 1 (negation follows a stabilization time after assertion of the LVD1 reset signal), set the MOCOCR.MCSTP bit to 0 (the MOCO operates). Additionally, if a transition to software standby is to be made, the only possible value for the RN bit is 0 (negation follows a stabilization time after VCC > Vdet1 is detected). Do not set the RN bit to 1 (negation follows a stabilization time after assertion of the LVD1 reset signal) in this case.

4. 7.2.8 Voltage Monitor 2 Circuit Control Register 0 (LVD2CR0)

[Before]

RN bit (Voltage Monitor 2 Reset Negate Select)

If the RN bit is to be set to 1 (negation follows a stabilization time after assertion of the LVD2 reset signal), set the LOCOCR.LCSTP bit to 0 (the LOCO operates). Additionally, if a transition to software standby is to be made, the only possible value for the RN bit is 0 (negation follows a stabilization time after VCC > Vdet2 is detected). Do not set the RN bit to 1 (negation follows a stabilization time after assertion of the LVD2 reset signal) in this case.

[After]

RN bit (Voltage Monitor 2 Reset Negate Select)

If the RN bit is to be set to 1 (negation follows a stabilization time after assertion of the LVD2 reset signal), set the MOCOCR.MCSTP bit to 0 (the MOCO operates). Additionally, if a transition to software standby is to be made, the only possible value for the RN bit is 0 (negation follows a stabilization time after VCC > Vdet2 is detected). Do not set the RN bit to 1 (negation follows a stabilization time after assertion of the LVD2 reset signal) in this case.

5. Table 41.33 SCI timing (2)

[Before]

Item				Symbol	Min	Max	Unit	Test conditions
Simple SPI	Data rise and fall time	Master		t_{Dr}, t_{Df}	-	20	ns	Figure 41.37 to Figure 41.40
		Slave	1.8 V or above		-	20		
			1.6 V or above		-	30		

[After]

Item				Symbol	Min	Max	Unit	Test conditions
Simple SPI	Data rise and fall time	Master	1.8 V or above	t_{Dr}, t_{Df}	-	20	ns	Figure 41.37 to Figure 41.40
			1.6 V or above		-	30		
		Slave	1.8 V or above		-	20		
			1.6 V or above		-	30		

6. Table 41.35 SPI timing (2 of 2)

[Before]

Item			Symbol	Min	Max	Unit	Test conditions
SPI	Slave access time	2.7 V or above	t_{SA}	-	2 x t_{Pcyc} + 50	ns	Figure 41.47 and Figure 41.48 C = 30pF
		2.4 V or above		-	2 x t_{Pcyc} + 60		
		1.8 V or above		-	2 x t_{Pcyc} + 85		
		1.6 V or above		-	2 x t_{Pcyc} + 110		
	Slave output release time	2.7 V or above	t_{REL}	-	2 x t_{Pcyc} + 50		
		2.4 V or above		-	2 x t_{Pcyc} + 60		
		1.8 V or above		-	2 x t_{Pcyc} + 85		
		1.6 V or above		-	2 x t_{Pcyc} + 110		

[After]

Item			Symbol	Min	Max	Unit	Test conditions
SPI	Slave access time	2.4 V or above	t_{SA}	-	2 x t_{Pcyc} + 100	ns	Figure 41.46 and Figure 41.47 C = 30pF
		1.8 V or above		-	2 x t_{Pcyc} + 140		
		1.6 V or above		-	2 x t_{Pcyc} + 180		
	Slave output release time	2.4 V or above	t_{REL}	-	2 x t_{Pcyc} + 100		
		1.8 V or above		-	2 x t_{Pcyc} + 140		
		1.6 V or above		-	2 x t_{Pcyc} + 180		