Date: Jul. 26, 2016

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-SY*-A008A/E	Rev.	1.00
Title	Revised information of S124 User's Manual from Rev.1.00		Information Category	Technical Notification		
Applicable Product	Renesas Synergy™ S1 Series S124	Lot No. All lots	Reference Document	S124 User's Manual: Microcontrollers, Rev.1.00		

1. 28. Serial Peripheral Interface (SPI)

• Max transfer bit length is changed from 16 bits to 32 bits (data buffer size is changed from 16 bits to 32 bits)

[Before]

Item	Description	place
Data format	Transfer bit length selectable as 8, 9, 10, 11, 12, 13, 14, 15, or 16 bits.	Table 28.1
SPI Data Register	SPDR_HA	28.2.5 etc.
SPI Data Control Register	Bit 5 : Reserved	28.2.7
SPI Command Registers 0	SPB[3:0] bit select SPI Data Length from 8, 9, 10, 11, 12, 13, 14, 15, or 16 bits	28.2.12
Transfer data length	8 to 16 bits	Table 28.4
Operation/data format	The explanation about 16-bit and 8-bit data transfer	28.3.4.1, 28.3.4.2

[After]

Item	Description	place
Data format	Transfer bit length selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits.	Table 28.1
SPI Data Register	SPDR/SPDR_HA	28.2.5 etc.
SPI Data Control Register	Bit 5 : SPLW (SPI Word Access/Halfword Access specification)	28.2.7
SPI Command Registers 0	SPB[3:0] bit select SPI Data Length from 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits	28.2.12
Transfer data length	8 to 16, 20, 24, or 32 bits	Table 28.4
Operation/data format	The explanation about 32-bit and 24-bit data transfer	28.3.4.1, 28.3.4.2

2. 41.9 POR and LVD Characteristics

• Modified LVD Hysteresis width (Electrical Characteristics).

[Before]

Table 41.53 Power-on reset circuit and voltage detection circuit characteristics (2)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Hysteresis width (LVD1 and LVD2)	V_{LVH}	-	70	-	mV	V_{det1_0} to V_{det1_4} selected.
		-	60	-		V_{det1_5} to V_{det1_9} selected.
		-	50	-		V_{det1_A} to V_{det1_B} selected.
		-	40	-		V_{det1_C} to V_{det1_D} selected.
		-	60	-		LVD2 selected.

(c) 2016. Renesas Electronics Corporation. All rights reserved.

[After]

Table 41.53 Power-on reset circuit and voltage detection circuit characteristics (2)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Hysteresis width (LVD0, LVD1, and LVD2)	V_{LVH}	-	60	-	mV	LVD0 selected
		-	100	-		V_{det1_0} to V_{det1_2} selected.
		-	60	-		V_{det1_3} to V_{det1_9} selected.
		-	50	-		V_{det1_A} to V_{det1_B} selected.
		-	40	-		V_{det1_C} to V_{det1_F} selected.
		-	60	-		LVD2 selected.

3. 19.9.2 Settings of GTCCRn during Compare Match Operation (n = A to F)

[Before]

(3) When automatic dead time setting is made in saw-wave one-shot pulse mode

The GTCCRC and GTCCRD registers must be set to satisfy the following restrictions. If the restrictions are not satisfied, the correct output waveforms with secured dead time may not be obtained.

• In up-counting: GTCCRC < GTCCRD, GTCCRC > GTDVU, GTCCRD < GTPR – GTDVU

• In down-counting: GTCCRC > GTCCRD, GTCCRC < GTPR – GTDVU, GTCCRD > GTDVU

Similarly, the GTCCRE and GTCCRF registers must be set to satisfy the following restrictions. If the restrictions are not satisfied, the correct output waveforms with secured dead time may not be obtained.

• In up-counting: GTCCRE < GTCCRF, GTCCRE > GTDVU, GTCCRF < GTPR – GTDVU

• In down-counting: GTCCRE > GTCCRF, GTCCRE < GTPR – GTDVU, GTCCRF > GTDVU

[After]

(3) When automatic dead time setting is made in saw-wave one-shot pulse mode

The GTCCRC and GTCCRD registers must be set to satisfy the following restrictions. If the restrictions are not satisfied, the correct output waveforms with secured dead time may not be obtained.

• In up-counting: GTCCRC < GTCCRD, GTCCRC > GTDVU, GTCCRD < GTPR – GTDVU

• In down-counting: GTCCRC > GTCCRD, GTCCRC < GTPR – GTDVU, GTCCRD > GTDVU

4. 16.2.1 Port Control Register 1

[Before]

16.2.1 Port Control Register 1 (PCNTR1)

PDR is a bit that selects the input or output direction for individual pins of the corresponding port when the pins are configured as general I/O pins. Each bit of PORTm.PDR corresponds to each pin of port m. I/O direction can be specified in 1-bit unit.

[After]

16.2.1 Port Control Register 1 (PCNTR1/PODR/PDR)

The Port Control Register 1 (PCNTR1) is a 32-bit and 16-bit read/write register that controls port direction and port output data. PODR bits [31:16] in PCNTR1 and PDR bits [15:0] in PCNTR1 are accessed in 16-bit units.

The PDR bit selects the input or output direction for individual pins of the associated port when the pins are configured as general I/O pins. Each bit of PORTm.PDR corresponds to each pin of port m. I/O direction can

be specified in 1-bit unit.

5. 16.2.2 Port Control Register 2

[Before]

16.2.2 Port Control Register 2 (PCNTR2)

PIDR is a bit that reflects the individual pin states of the port. The pin states of port m can be read with PORTm.PIDR regardless of the values of PORTm.PIDR and PORTm.PDR. When PORTm.PMR = 1 or PORTm.PDR = 1, the read data is a “don’t care”.

[After]

16.2.2 Port Control Register 2 (PCNTR2/EIDR/PIDR)

The Port Control Register 2 (PCNTR2) allows read access to the port input data and the port event input data by 32-bit and 16-bit access. EIDR bits [31:16] in PCNTR2 and PIDR bits [15:0] in PCNTR2 are accessed in 16-bit units.

The PIDR bit reflects the individual pin states of the port. The pin states of port m can be read with PORTm.PIDR regardless of the values of PORTm.PIDR and PORTm.PDR. When PORTm.PMR = 1 or PORTm.PDR = 1, the read data is a “don’t care”.

6. 16.2.3 Port Control Register 3

[Before]

16.2.3 Port Control Register 3 (PCNTR3)

POSR is a bit that changes the PODR based on POSR being set when a software write occurs. For example, for P100, when PORT1.POSR00 = 1, PORT1.PODR00 outputs 1. The bits of non-existent port m are reserved.

[After]

16.2.3 Port Control Register 3 (PCNTR3/PORR/POSR)

The Port Control Register 3 (PCNTR3) is a 32-bit and 16-bit write register that controls the setting or resetting of the port output data. PORR bits [31:16] in PCNTR3 and POSR bits [15:0] in PCNTR3 are accessed in 16-bit units.

The POSR bit changes the PODR based on POSR being set when a software write occurs. For example, for P100, when PORT1.POSR00 = 1, PORT1.PODR00 outputs 1. The bits of non-existent port m are reserved.

7. 16.2.4 Port Control Register 4

[Before]

16.2.4 Port Control Register 4 (PCNTR4)

EOSR is a bit that changes the PODR based on EOSR being set when an ELC_PORTx occurs. For example, for P100 if PORT1.EOSR00 is set to 1 when the ELC_PORTx occurs, PORT1.PODR00 outputs 1. The bits of non-existent port m are reserved.

[After]

16.2.4 Port Control Register 4 (PCNTR4/EORR/EOSR)

The Port Control Register 4 (PCNTR4) is a 32-bit and 16-bit read/write register that controls the setting or resetting of the port output data by event input from the ELC. EORR bits [31:16] in PCNTR4 and EOSR bits [15:0] in PCNTR4 are accessed in 16-bit units.

The EOSR bit changes the PODR based on EOSR being set when an ELC_PORTx occurs. For example, for P100 if PORT1.EOSR00 is set to 1 when the ELC_PORTx occurs, PORT1.PODR00 outputs 1. The bits of non-existent port m are reserved.

8. 16.2.5 Port mn Pin Function Select Register (PmnPFS) (m = 0 to 5; n = 00 to 15)

[Before]

16.2.5 Port mn Pin Function Select Register (PmnPFS) (m = 0 to 5; n = 00 to 15)

The Port mn Pin Function Control Register (PmnPFS) selects the pin function.

The PDR/PIDR/PODR bits serve the same function as the PCNTR. When these bits are read, the PCNTR value is read.

[After]

16.2.5 Port mn Pin Function Select Register (PmnPFS/PmnPFS_HA/PmnPFS_BY) (m = 0 to 5; n = 00 to 15)

The Port mn Pin Function Select Register (PmnPFS) is a 32-bit, 16-bit, and 8-bit read/write register that controls the selection of the port mn function which is set by 32-bit units. PmnPFS_HA bits [15:0] in PmnPFS are accessed in 16-bit units and PmnPFS_BY bits [7:0] are accessed in 8-bit units.

The PDR/PIDR/PODR bits serve the same function as the PCNTR. When these bits are read, the PCNTR value is read.

9. 2.8.2.4 Connecting sequence and SWD authentication

[Before]

Because the OCD emulator is protected by the SWD authentication mechanism, OCD might be required to input the ID code to the authentication registers. The value of the OSIS in the Option Setting Memory determines whether the code is required.

(1) When OSIS is all 1s (default)

OCD authentication is not required and OCD can use the AHB-AP without authentication.

(omitted)

(2) When OSIS is not all 1s

OCD authentication is required and OCD must write the unlock code to the IAUTH registers 0 to 3 in the OCDREG before using the AHB-AP.

[After]

Because the OCD emulator is protected by the SWD authentication mechanism, OCD might be required to input the ID code to the authentication registers. The value of the OSIS in the Option Setting Memory determines whether the code is required. After the negation of the reset, it must wait for 36 µs to compare the value of OSIS at the time of the cold start.

(1) When MSB of OSIS is 0 (bit 127 = 0)

The ID code is always non-matching and connection to the on-chip debugger is prohibited.

(2) When OSIS is all 1s (default)

OCD authentication is not required and OCD can use the AHB-AP without authentication.

(omitted)

(3) When OSIS is ALeRASE in ASCII code

The content of the user flash area is erased at once. For details, see section 37, Flash Memory.

(4) When OSIS is not all 1s

OCD authentication is required and OCD must write the unlock code to the IAUTH registers 0 to 3 in OCDREG before using the AHB-AP.

10. 8.2.8 Oscillation Stabilization Flag Register (OSCSF)

[Before]

8.2.8 Oscillation Stabilization Flag Register (OSCSF)

[Setting condition]

After the high-speed clock oscillator stops and the HOCOCR.HCSTP bit is set to 0, supply of the high-speed clock in the MCU starts after 287 cycles of the middle-speed clock are counted.

[After]

8.2.8 Oscillation Stabilization Flag Register (OSCSF)

[Setting condition]

After the high-speed clock oscillator stops and the HOCOCR.HCSTP bit is set to 0, supply of the high-speed clock in the MCU starts after 287 cycles of the middle-speed clock cycles associated with the setting of the HOCOWTCR register are counted.

11. 8.2.15 Clock Out Control Register (CKOCR)

[Before]

8.2.15 Clock Out Control Register (CKOCR)

Set this bit to enable output from the CLKOUT pin.

When this bit is set to 1, the selected clock is output. When this bit is set to 0, low is output. A glitch might be generated in the output if the CKOSTP bit is rewritten while the clock is still oscillating.

[After]

8.2.15 Clock Out Control Register (CKOCR)

Set this bit to enable output from the CLKOUT pin.

When this bit is set to 1, the selected clock is output. When this bit is set to 0, low is output. When changing this bit, confirm that the clock out source clock selected in the CKOSEL[3:0] bits is stable. Otherwise, a glitch might be generated in the output.

This bit must be cleared before entering Software Standby mode if the selecting clock out source clock is stopped in that mode.

12. 36.3.2 SRAM Error Source

[Before]

The SRAM error source is a parity error. Parity errors can be specified as either non-maskable interrupts or a reset, in the OAD bit of PARIOAD. TDC activation is not supported for SRAM parity errors.

Note: Reset and non-maskable interrupts are not generated when a debugger is connected.

[After]

The SRAM error source is a parity error. Parity errors can be specified as either non-maskable interrupts or a reset, in the OAD bit of PARIOAD. TDC activation is not supported for SRAM parity errors.

13. 25.13.6 Restrictions on Clock Synchronous Transmission (Clock Synchronous mode and Simple SPI mode)

[Before]

When the external clock source is used as a synchronization clock, the following restrictions apply.

(1) Start of transmission

Update TDR by the CPU or DTC and wait for at least five PCLKB cycles before allowing the transmit clock to be input, see Figure 25.77.

(2) Continuous transmission

Write the next transmit data to TDR or TDRHL before the falling edge of the transmit clock, bit [7], see Figure 25.77.

When updating TDR after bit [7] has started to transmit, update TDR while the synchronization clock is in the low-level period, and set the high-level width of the transmit clock, bit [7] to four PCLKB cycles or longer, see Figure 25.77.

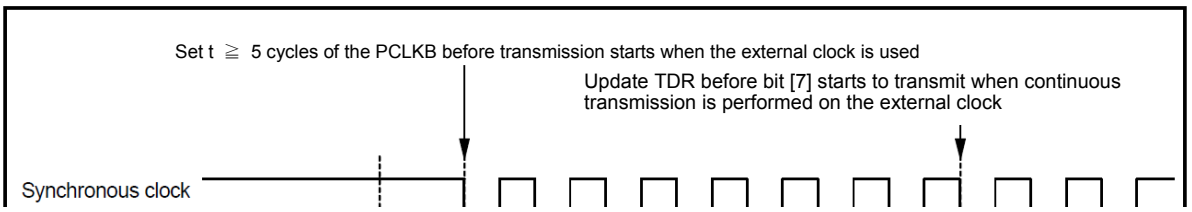

Figure 25.77 Restrictions on the use of external clock in clock synchronous transmission

[After]

When the external clock source is used as a synchronization clock, the following constraints apply.

(1) Start of transmission

Wait at least the following time from writing transmit data to TDR to the start of the external clock input:

• 1 PCLKB cycle + data output delay time for the slave (tDO) + setup time for the master (tSU).

See Figure 25.77

(2) Continuous transmission

Write the next transmit data to TDR or TDRHL before the falling edge of the transmit clock, bit [7], see Figure 25.77.

When updating TDR after bit [7] starts to transmit, update TDR while the synchronization clock is in the low-level period, and set the high-level width of the transmit clock, bit [7] to 4 PCLKB cycles or longer, see Figure 25.77.

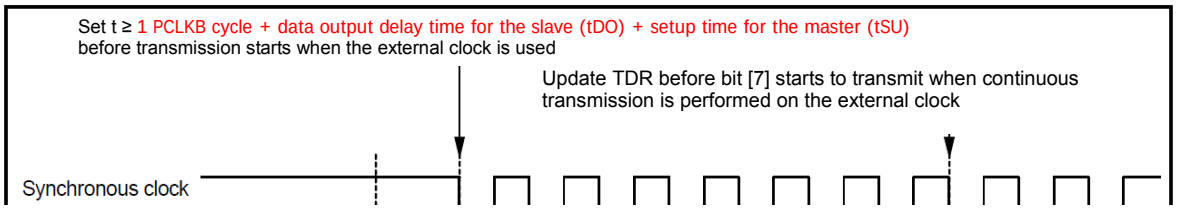

Figure 25.77 Restrictions on the use of external clock in clock synchronous transmission

14. 41.9 POR and LVD Characteristics

[Before]

tPOR specification is not defined.

[After]

Table 41.53 Power-on reset circuit and voltage detection circuit characteristics (2)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Wait time after Power-on reset cancellation	LVD0: enable	t_{POR}	-	1.7	-	ms	-
	LVD0: disable	t_{POR}	-	1.3	-	ms	-

15. 10.8.4 Snooze Operation Example

[Before]

Table 10.9 and Table 10.10 are max transfer rate of SCI0 in Snooze mode.

High-speed mode, Middle-speed mode, Low-speed mode

Table 10.9 HOCO: ± 1.0% (Ta = -20 to 85°C) (Unit: bps)

Maximum division ratio of ICLK, PCLKB, and PCLKD	HOCO frequency			
	24 MHz	32 MHz	48 MHz	64 MHz
1	9600	9600	-	
2			4800	2400
4				
8	4800	4800		
16				
32				
64				

High-speed mode, Middle-speed mode, Low-speed mode

Table 10.10 HOCO: ± 1.5% (Ta = -40 to -20°C, 85 to 105°C) (Unit: bps)

Maximum division ratio of ICLK, PCLKB, and PCLKD	HOCO frequency			
	24 MHz	32 MHz	48 MHz	64 MHz
1	2400		-	
2			2400	
4				
8				
16				
32				
64				

[After]

Table 10.9 and Table 10.10 are maximum transfer rate of SCI0 in Snooze mode. When SCI0 is used in Snooze mode, the following settings must be used:

• BGDM = 0

• ABCS = 0

• ABCSE = 0

See section 25, Serial Communications Interface (SCI) for information of these bits.

High-speed mode, Middle-speed mode, Low-speed mode

Table 10.9 HOCO: ± 1.0% (Ta = -20 to 85°C) (Unit: bps)

Maximum division ratio of ICLK, PCLKB, and PCLKD	HOCO frequency			
	24 MHz	32 MHz	48 MHz	64 MHz
1	9600*1	9600*4	-	-
2	9600*2	9600*5	4800	2400
4	9600*3	9600*6	4800	2400
8	4800	4800	4800	2400
16	4800	4800	4800	2400
32	2400	2400	2400	2400
64	2400	2400	2400	2400

Note 1. SCI0.SMR.CKS[1:0]=00b, SCI0.SEMR.BRME=1, SCI0.BRR=3Dh, SCI0.MDDR = CEh must be used for 9600bps.
Note 2. SCI0.SMR.CKS[1:0]=00b, SCI0.SEMR.BRME=1, SCI0.BRR=1Eh, SCI0.MDDR = CEh must be used for 9600bps.
Note 3. SCI0.SMR.CKS[1:0]=00b, SCI0.SEMR.BRME=1, SCI0.BRR=0Dh, SCI0.MDDR = BAh must be used for 9600bps.
Note 4. SCI0.SMR.CKS[1:0]=00b, SCI0.SEMR.BRME=1, SCI0.BRR=3Eh, SCI0.MDDR = 9Dh must be used for 9600bps.
Note 5. SCI0.SMR.CKS[1:0]=00b, SCI0.SEMR.BRME=1, SCI0.BRR=32h, SCI0.MDDR = FEh must be used for 9600bps.
Note 6. SCI0.SMR.CKS[1:0]=00b, SCI0.SEMR.BRME=1, SCI0.BRR=18h, SCI0.MDDR = F9h must be used for 9600bps.

High-speed mode, Middle-speed mode, Low-speed mode

Table 10.10 HOCO: ± 2.0% (Ta = -40 to -20°C, 85 to 105°C) (Unit: bps)

Maximum division ratio of ICLK, PCLKB, and PCLKD	HOCO frequency			
	24 MHz	32 MHz	48 MHz	64 MHz
1	2400	-	-	-
2	2400	2400	2400	1200
4	2400	2400	2400	1200
8	2400	2400	2400	1200
16	2400	2400	2400	1200
32	1200	1200	1200	1200
64	1200	1200	1200	1200

16. Modified SCI register explanation (SSR_FIFO.RDF, SIMR3.IICSTIF, FCR.FM)

[Before]

SIMR3.IICSTIF bit description

Writing 0 to the bit (confirm that the IICSTIF flag is 0 before doing so).

[After]

SIMR3.IICSTIF bit description

Writing 0 to the bit (after that, confirm that the IICSTIF flag is 0).

17. Simultaneous Serial Data Transmission and Reception (Clock Synchronous Mode)

[Before]

(2) FIFO selected

Figure 25.44 shows a sample flowchart for simultaneous serial transmit and receive operations in Clock synchronous mode at FIFO selected.

(omitted)

To switch from receive mode to simultaneous transmit and receive mode, check that the SCI completes the reception. Set the RIE and RE bits to 0. Check that the receive error flags ORER, FER, and PER in SSR_FIFO are 0, then set the TIE, RIE, TE, and RE bits in SCR to 1 simultaneously by a single instruction.

[After]

(2) FIFO selected

Figure 25.44 shows an example flow of simultaneous serial transmit and receive operations in clock synchronous mode with FIFO selected.

(omitted)

To switch from receive mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the reception.
2. Set the RIE and RE bits to 0.
3. Check that the receive error flags ORER in SSR_FIFO are 0, then set the TIE, RIE, TE, and RE bits in SCR to 1 simultaneously by a single instruction.