Renesas Synergy™ Platform

S3A7 to S3A3 MCU Group Migration Guide

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Introduction

This Application Note compares hardware peripherals, port select features, and functional differences between the Renesas Synergy™ Microcontrollers S3A7 MCU Group and the S3A3 MCU Group.

Target Device

Synergy S3A3 MCU Group

Contents

1. About this Document

This document is designed to provide the user with an overview of the functional, hardware, and electrical characteristic differences when migrating from the Synergy S3A7 MCU Group to the S3A3 MCU Group.

2. Audience

This document is intended for users who are designing application systems using the Synergy S3A3 MCU Group devices. Users are expected to have a technical understanding of the peripherals provided in the S3A7 MCU Group. This application note should be used in conjunction with the *S3A3 MCU Group User's Manual: Microcontrollers*.

The application note presents two major sections. The first section specifies functional and specification differences between the Synergy S3A7 MCU Group and the S3A3 MCU Group, respectively. The second section details the differences in port functionality between the two MCU's.

3. References

Renesas provides the following documents for the Synergy S3 Series MCUs. Before using any of these documents, visit our web site to obtain the latest versions in the Website and Support section of this application note.

Table 1 Synergy S3 Series MCU Group Documents

Document Type	Description	Description Title	Description No.
Datasheet S3A3 MCU Group	Overview and electrical characteristics of MCU.	S3A3 MCU Group Datasheet	R01DS0307EU0100
S3A3 MCU Group User's Manual: Microcontrollers	MCU specifications (pin assignments, memory maps, peripheral functions, electrical characteristics, and timing charts) and operation descriptions.	S3A3 MCU Group User's Manual: Microcontrollers	R01UM0006EU0100
Datasheet S3A7 MCU Group	Overview and electrical characteristics of MCU.	S3A7 MCU Group Datasheet	R01DS0263EU0100
S3A7 User's Manual: Microcontrollers	MCU specifications (pin assignments, memory maps, peripheral functions, electrical characteristics, and timing charts) and operation descriptions.	S3A7 MCU Group User's Manual: Microcontrollers	R01UM0002EU0120
Renesas Synergy Software Package	API reference and introduction to SSP architecture and programming.	Renesas Synergy Software Package (SSP) User's Manual	R01US0171EU100

4. Numbering Notation

The following numbering notation is used throughout this manual:

Table 2 Example of number notation

Example	Description
011b	Binary number. For example, the binary equivalent of the number 3 is 011b
1Fh	Hexadecimal number. For example, the hexadecimal equivalent of the number 31 is described 1Fh. In some cases, a hexadecimal number is shown with the prefix 0x.
1234	Decimal number. A decimal number is followed by this symbol only when the possibility of confusion exists. Decimal numbers are generally shown without a suffix.
Bit 4	Specifies the bit position in field or register.

5. Specification and Hardware Differences

Table 1 compares hardware compatibility and differences between the S3A3 MCU Group and S3A7 MCU Group. The table is ordered with increasing specifics from left to right. The left most column corresponds to a system as noted in the user's manual for the Synergy S3A3 MCU Group or S3A7 MCU Group. Values in the S3A7 column represent a system, subsystem, or field in register exists and has a certain value. Values in the S3A3 column show the change in hardware, new feature addition, or notes a main feature. The Reference column specifies the section in the *S3A3 MCU Group User's Manua*l that can be referred to for more information.

Note: The following table describes the terms and functionality of the peripherals.

Table 3 Terms and functionality of peripherals

Terms	Description
Exists or Available	The peripheral or function is implemented for a MCU Group
Does Not Exist or Not Available	The peripheral specified has been removed (when compared to the other MCU Group) or does not exist in the MCU Group
Not Applicable	The criteria for comparison is invalid for the MCU Group

Table 1. 1 Specification Difference (1 of 20)

Specification			S3A7	S3A3	S3A3 HWM Reference
CPU	CoreSight Register	PID0	Initial Value is 00000002h	Initial Value is 00000013h	Table 2.8
Resets	Register initialized by Reset Sources	LOCOCR	All reset sources	Only VBATT_POR	Table 6.3
		AGT	Only VBATT_POR	Power-On, Voltage Monitor (0, 1, 2)	
	State of LOCO when a reset occurs	All reset sources except VBATT_POR	Initialized to enable	State persists through reset	Table 6.5
Clock Generation Circuit	MOSC - Resonator Frequency	USB Boot Mode	4,6,8,12 MHz	Not Applicable	Table 9.1
	Clock Source	USB Clock (UCLK)	PLL	PLL or HOCO (HOCO used only when USBFS is used the device controller)	Table 9.2
	USB Clock Control Register (USBCKCR)		Not Applicable	Exists	9.2.26
Low Power Modes	I2C Bus Interface (IIC0)	Snooze Mode	Operation prohibited	Selectable	Table 11.2
	High-Speed Analog Comparator (ACMPHSn, n=0, 1)	All low power modes	Selectable	ACMPHSn Does Not Exist	
	Standby Control Register (SBYCR)	Bit 14 - OPE bit	Bus control signal ALE does not exist	Can retain the value of the bus control signal ALE	11.2.1
	Module Stop Control Register A (MSTPCRA)	Bit 1	MSTPA1; Value after reset is 0	Reserved; Value after reset is 1	11.2.2
	Module Stop Control Register B (MSTPCRB)	Bit 5	MSTPB5	Reserved	11.2.3

Table 1. 2 Specification Difference (2 of 20)

Specification			S3A7	S3A3	S3A3 HWM Reference
Low Power Modes	Module Stop Control Register C (MSTPCRC)	Bit 7	MSTPC7	Reserved	11.2.4
	Module Stop Control Register D (MSTPCRD)	Bit 19	Reserved	MSTPD19; When Bit 19 is set to 0, set Bit 29 to 0	11.2.5
		Bit 28	MSTPD28	Reserved	
		Bit 30	MSTPD30	Reserved	
Battery Backup Function	VBATT Wakeup I/O n Output Trigger Select Register (n = 0, 1, 2)	VBTWCH0OTSR	Bit 5 is CH0VAGTUTE	Bit 5 is Reserved	12.2.8
		VBTWCH1OTSR	Bit 5 is CH1VAGTUTE	Bit 5 is Reserved	12.2.9
		VBTWCH2OTSR	Bit 5 is CH2VAGTUTE	Bit 5 is Reserved	12.2.10
	VBATT Input Control Register (VBTICTLR)	Bit 0 - VCH0INEN (VBATT Wakeup I/O 0 Input Enable)	Disable or Enable VBATWIO0, RTCIC0, AGTIO0_B, and AGTIO1_B inputs	Disable or Enable VBATWIO0, RTCIC0 inputs	12.2.11
		Bit 1 - VCH1INEN (VBATT Wakeup I/O 1 Input Enable)	Disable or Enable VBATWIO1, RTCIC1, AGTIO0_C, and AGTIO1_C inputs	Disable or Enable VBATWIO1, RTCIC1 inputs	
	VBATT Wakeup Trigger Source Enable Register (VBTWTER)		Bit 5 is VAGTUE	Bit 5 is Reserved	12.2.13
	VBATT Wakeup Trigger Source Flag Register (VBTWFR)		Bit 5 is VAGTUF	Bit 5 is Reserved	12.2.15
	VBATT Wakeup Control Function for AGT		Available as AGT is operated on battery backup power	Not available as AGT is operating on VCC	12.3.5

Table 1. 3 Specification Difference (3 of 20)

Specification			S3A7	S3A3	S3A3 HWM Reference
Battery Backup Function	Backup Register Access Control Register (BKRACR)		Not Applicable	Exists	12.2.16
	VBATT Pin Power Supply	AGT0 and AGT1 Modules	Yes	No; Stopped in low power mode	12.3.1
	Operating States in VBATT Mode	Low-Speed On-Chip Oscillator	Operational	Operation or non-operation can be selected in the LOCOCR.LCSTP bit. Oscillator status does not change when entering VBATT mode	Table 12.2
		I/O Ports	AGTIOn_B port (n = 0,1) AGTIOn_C port (n = 0,1) operating	AGTIOn_B port (n = 0,1) AGTIOn_C port (n = 0, 1) not operating	Table 12.2
Register Write Protection	Association between PRCR bits and registers to be protected	PRC0 – USBCKCR, PRC1 – BKRACR	No	Yes	Table 13.1
Interrupt Controller Unit (ICU)	Peripheral Function Interrupts	Number of Sources	205	209	Table 14.1
	Interrupt Sources for NVIC	Number of Sources	64	32	
	ICU Event Link Setting Register n (IELSRn), where n = Number of Interrupt sources for NVIC	ICU Event Link Select (IELS)	Spans from bit 0 to bit 8. All bits must be written to simultaneously. Requires halfword or word access.	Spans from bit 0 to bit 7. Bit 8 is reserved.	14.2.6
	DMAC Event Link Setting Register n (DELSRn)	Register size/length	Bit 0 to Bit 15	Bit 0 to Bit 31	14.2.7

Table 1. 4 Specification Difference (4 of 20)

Specification			S3A7	S3A3	S3A3 HWM Reference
Interrupt Controller Unit (ICU)	DMAC Event Link Setting Register n (DELSRn)	DMAC Event Link Select (DELS)	Spans from bit 0 to bit 8. All bits must be written to simultaneously. Requires halfword access. Clear the DELS bits 0 to 8 at the end of DMA transfer as a precaution	Spans from bit 0 to bit 7. Bit 8 is reserved. Clear the DELS bits 0 to 7 at the end of DMA transfer as a precaution	14.2.7 17.4.4
		Bit 16	Does Not Exist	IR Flag. Writing 1 to the flag is prohibited.	14.2.7
		Bit 17 to Bit 31	Does Not Exist	Reserved	
	SYS Event Link Setting Register (SELSR0)	SYS Event Link Select (SELS)	Spans from bit 0 to bit 8. Requires halfword access. All bits must be written to simultaneously	Spans from bit 0 to bit 7. Bit 8 is reserved.	14.2.8
	Interrupt Vector Table	Exception # 48 to 79	Exists; Refer to Manual	Does Not Exist; Refer to Manual	14.3.1, Table 14.3
	Event Number		Refer to Manual	Refer to Manual	Table 14.4
Buses	Slave Interface and Protected Slave function	Memory Bus 5	Connected to SRAM1. Address from 20020000h to 2002FFFFh	Does Not Exist	Table 15.1 Table 15.2 Table 16.7
		Internal peripheral bus 4	Connected to peripheral modules SCI, IrDA, GPT, SPI, CRC and SDHI	Connected to peripheral modules SCI, GPT, SPI, CRC and SDHI	Table 15.1 Table 16.7

Table 1. 5 Specification Difference (5 of 20)

Specification			S3A7	S3A3	S3A3 HWM Reference
Buses	Slave Interface and Protected Slave function	Internal peripheral bus 5	Connected to peripheral modules: KINT, AGT, USBFS, OPAMP, ACMPHS, ACMPLP, CTSU and SLCDC	Connected to peripheral modules: KINT, AGT, USBFS, OPAMP, ACMPLP, DAC8, CTSU and SLCDC	Table 15.1 Table 16.7
	External Bus	External address space	Not Applicable	Address/data multiplexed bus: Selectable 8-bit or 16-bit bus space. Refer to Manual for details.	Table 15.3 15.5.2
		CS area controller	Not Applicable	Address/data can be multiplexed or be on separate buses. Refer to Manual for details.	
		Address Output Pins	A16 to A00	A23 to A00	Table 15.4
		ALE Pin	Does Not Exist	Exists	
	CSn Control Register (CSnCR) (n = 0 to 3)	Bit 12	Reserved	MPXEN. Specifies the separate bus interface or Address/Data multiplexed I/O interface for area n; (n = 0 to 3)	15.3.1

Table 1. 6 Specification Difference (6 of 20)

Specification			S3A7	S3A3	S3A3 HWM Reference
Buses	CSn Recovery Cycle Register (CSnREC) (n = 0 to 3)	Condition when the preceding bus access is an address/data multiplexed bus access	Not Applicable	CSnREC is valid when the recovery cycle insertion is enabled with the multiplexed bus recovery cycle insertion enable bit (RCVENMj) (j = 0 to 7)) in CSRECEN	15.3.2
	CS Recovery Cycle Insertion Enable Register (CSRECEN)	Bit 8 to Bit 15	Reserved	RCVENM0 to RCVENM7 (Multiplexed Bus Recovery Cycle Insertion Enable), enables the insertion of read or write recovery cycles when a repeated R/W access is made on an external bus	15.3.3
	CSn Mode Register (CSnMOD) (n = 0 to 3)	Conditions when the address/data multiplexed I/O interface is selected using MXPEN bit in CSnCR	Not Applicable	PRENB bit and PWENB bit are not set to enable page R/W accesses as they are not supported in the address/data multiplexed I/O interface	15.3.4
	CSn Wait Control Register 2 (CSnWCR2) (n = 0 to 3)	Bit 13 and Bit 12	Reserved	AWAIT[1:0]	15.3.6

Table 1. 7 Specification Difference (7 of 20)

Specification			S3A7	S3A3	S3A3 HWM Reference
Buses	CSn Wait Control Register 2 (CSnWCR2) (n = 0 to 3)	Conditions for RDON[2:0] when the address/data multiplexed I/O interface is selected	Not Applicable	CSnWCR2.AWAIT[1:0] value + 2 ≤ CSnWCR2.RDON[2:0] value ≤ CSnWCR1.CSRWAIT[4:0] value	15.3.6
		Conditions for WRON[2:0] when the address/data multiplexed I/O interface is selected	Not Applicable	CSnWCR2.AWAIT[1:0] value + 2 ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value	
		Conditions for WDON[2:0] when the address/data multiplexed I/O interface is selected	Not Applicable	CSnWCR2.AWAIT[1:0] value + 2 ≤ CSnWCR2.WDON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value	
		Conditions for CSON[2:0] when the address/data multiplexed I/O interface is selected	Not Applicable	CSnWCR2.CSON[2:0] value ≤ CSnWCR2.AWAIT[1:0] value	
	Constraints on using address/data multiplexed bus interface.		Not Applicable	Refer to Manual	15.5.7 (2)

Table 1. 8 Specification Difference (8 of 20)

Specification			S3A7	S3A3	S3A3 HWM Reference
Buses	Slave Bus Control Register (BUSSCNT<slave>)	BUSSCNTRAM1	Exists	Does Not Exist	15.3.8
	External Wait Function	External wait is enable (CSnMOD.EWENB = 1)	BCLK and EBCLK must be operated at the same frequency	BCLK and EBCLK can be operated at same or different frequency	15.5.3
	Bus Error Monitoring. Conditions Leading to Illegal Address Access Errors		Refer to Manual	Refer to Manual	15.6.3 Table 15.12
Memory Protection Unit MPU	Security MPU (Protects accesses from non-secure programs to the secure regions)		2 regions (PC), 1 region (code flash) Refer to Manual	2 regions (PC), 4 regions (code flash, SRAM, two secure functions) Refer to Manual	Table 16.1 Table 16.8
	Access Control Register for Memory bus 5 (SMPUSRAM1)		Exists	Does Not Exist	-
	Security MPU Program Counter Start Address Register (SECMPUPCSn) (n = 0, 1)		Value range is 0000 0000h to 000F FFFCh.	Value range is 0000 0000h to 00FF FFFCh and 1FF0 0000h to 200F FFFCh not including the reserved areas; Write value of the lower 2 bits is 0	16.6.1.1

Table 1. 9 Specification Difference (9 of 20)

Specification		S3A7	S3A3	S3A3 HWM Reference
Memory Protection Unit MPU	Security MPU Program Counter End Address Register (SECMPUPCEn) (n = 0, 1)	Value range is 0000 0003h to 000F FFFFh.	Value range is 0000 0003h to 00FF FFFFh and 1FF0 0003h to 200F FFFFh, not including the reserved areas; Write value of the lower 2 bits is 1	16.6.1.2
	Security MPU Region 0 Start Address Register (SECMPUS0)	Value range is 0000 0000h to 00FF FFFCh	Value range is 0000 0000h to 00FF FFFCh not including the reserved areas; Write value of the lower 2 bits is 0	16.6.1.3
	Security MPU Region 1 Start Address Register (SECMPUS1)	Does Not Exist	Exists	16.6.1.5
	Security MPU Region 1 End Address Register (SECMPUE1)	Does Not Exist	Exists	16.6.1.6
	Security MPU Region 2 Start Address Register (SECMPUS2)	Does Not Exist	Exists	16.6.1.7
	Security MPU Region 2 End Address Register (SECMPUE2)	Does Not Exist	Exists	16.6.1.8
	Security MPU Region 3 Start Address Register (SECMPUS3)	Does Not Exist	Exists	16.6.1.9
	Security MPU Region 3 End Address Register (SECMPUE3)	Does Not Exist	Exists	16.6.1.10

Table 1. 10 Specification Difference (10 of 20)

Specification			S3A7	S3A3	S3A3 HWM Reference
Memory Protection Unit MPU	Security MPU Access Control Register (SECMPUAC)		Bit 1, 2 and 3 are reserved	Bit 1, 2 and 3 are DIS1, DIS2 and DIS3 respectively	16.6.1.11
	Memory Protection		Refer to Manual	Refer to Manual	16.6.2
Event Link Controller (ELC)	Event link function	Types of event signals can be directly connected to modules	181	179	Table 19.1
	Event Link Setting Register n (ELSRn)	ELSR13 Register	Associated with DAC12 Channel 1	Does Not exist	19.2.3 Table 19.2
		Event Link Select (ELS)	Spans from Bit 8 to Bit 0.	Spans from Bit 7 to Bit 0	
		Number setting for the event signal to be linked.	0 0000 0001h to 1 1100 1010h	0000 0001h to 1101 0100h	
	Association between event signal names set in ELSRn.ELS bits and signal numbers		Refer to Manual	Refer to Manual	Table 19.3
I/O Ports	Total Number I/O pins in Packages	144 pins, 145 pins	124	126 (Added P914, P915)	Table 20.1
		121 pins	102	104 (Added P914, P915)	
		100 pins	82	84 (Added P914, P915)	
		64 pins	50	52 (Added P914, P915)	
	Number of CMOS I/O available (based on different pin packages)		Up to 121	Up to 123	Features
	Number of 5-V tolerant input/output (based on different pin packages)		Up to 10	Up to 11	Features

Table 1. 11 Specification Difference (11 of 20)

Specificatioon			S3A7	S3A3	S3A3 HWM Reference
I/O Ports	Functions - P408	Drive Capacity Switching	Low/Middle	Low/Middle/Middle(IIC)	Table 20.2
		5-V Tolerant	No	Yes	
	Port mn Pin Function Select Register (PmnPFS/PmnPFS_HA/PmnPFS_BY) (m= 0 to 9; n = 00 to 15)		Bit 11 is reserved	Bit 11 is P408	20.2.5
			P914 and P915 do not exist	Initial Value P914: 0001 0000h P915: 0001 0000h	
	Selecting USB_DP and USB_DM Pins		Not Applicable	Refer to Manual	20.5.6
	Pull-up/Pull-down Setting for P914 and P915 using USBFS/GPIO Function		Not Applicable	Refer to Manual	20.5.7
	Register settings for input/output pin function		Refer to Manual	Refer to Manual	Table 20.5 to Table 20.17
Port Output Enable for GPT (POEG)	Input Pins	External trigger input pin GTETRGC, GTETRGD	Exists	Does Not Exist	Table 22.2
	POEG Group n Setting Register (POEGGn)		Bit 8 is CDRE0, Bit 9 is CDRE1	Bit 8, Bit 9 are reserved	22.2.1
	Output-Disable Control Operation	ACMPHS Interrupt Request Detection	Refer to Manual	Not Applicable	22.3
	Interrupt Sources and Conditions	POEG Group C and Group D Interrupt	Refer to Manual	Not Applicable	22.4 Table 22.3
General PWM Timer (GPT)	Functions	32 bit channels	10	4	Table 23.1
		16 bit channels	None	6	

Table 1. 12 Specification Difference (12 of 20)

Specification		S3A7	S3A3	S3A3 HWM Reference
General PWM Timer (GPT)	General PWM Timer Start Source Select Register (GTSSR)	Bit 4 is SSGTRGCR	Bit 4 is reserved	23.2.5
		Bit 5 is SSGTRGCF	Bit 5 is reserved	
		Bit 6 is SSGTRGDR	Bit 6 is reserved	
		Bit 7 is SSGTRGDF	Bit 7 is reserved	
	General PWM Timer Stop Source Select Register (GTPSR)	Bit 4 is PSGTRGCR	Bit 4 is reserved	23.2.6
		Bit 5 is PSGTRGCF	Bit 5 is reserved	
		Bit 6 is PSGTRGDR	Bit 6 is reserved	
		Bit 7 is PSGTRGDF	Bit 7 is reserved	
	General PWM Timer Clear Source Select Register (GTCSR)	Bit 4 is CSGTRGCR	Bit 4 is reserved	23.2.7
		Bit 5 is CSGTRGCF	Bit 5 is reserved	
		Bit 6 is CSGTRGDR	Bit 6 is reserved	
		Bit 7 is CSGTRGDF	Bit 7 is reserved	
	General PWM Timer Up Count Source Select Register (GTUPSR)	Bit 4 is USGTRGCR	Bit 4 is reserved	23.2.8
		Bit 5 is USGTRGCF	Bit 5 is reserved	
		Bit 6 is USGTRGDR	Bit 6 is reserved	
		Bit 7 is USGTRGDF	Bit 7 is reserved	

Table 1. 13 Specification Difference (13 of 20)

Specification			S3A7	S3A3	S3A3 HWM Reference
General PWM Timer (GPT)	General PWM Timer Down Count Source Select Register (GTDNSR)		Bit 4 is DSGTRGCR	Bit 4 is reserved	23.2.9
			Bit 5 is DSGTRGCF	Bit 5 is reserved	
			Bit 6 is DSGTRGDR	Bit 6 is reserved	
			Bit 7 is DSGTRGDF	Bit 7 is reserved	
	General PWM Timer Input Capture Source Select Register A (GTICASR)		Bit 4 is ASGTRGCR	Bit 4 is reserved	23.2.10
			Bit 5 is ASGTRGCF	Bit 5 is reserved	
			Bit 6 is ASGTRGDR	Bit 6 is reserved	
			Bit 7 is ASGTRGDF	Bit 7 is reserved	
	General PWM Timer Input Capture Source Select Register B(GTICBSR)		Bit 4 is BSGTRGCR	Bit 4 is reserved	23.2.11
			Bit 5 is BSGTRGCF	Bit 5 is reserved	
			Bit 6 is BSGTRGDR	Bit 6 is reserved	
			Bit 7 is BSGTRGDF	Bit 7 is reserved	
	General PWM Timer Interrupt Output Setting Register (GTINTAD)	Bit 25, Bit 24 - GRP[1:0] Output Disable Source Select	Group A, B, C and D	Group A and B	23.2.15
	General PWM Timer Register GPT16m (m = 4 to 9)	GTCNT	Not Applicable	The upper 16 bits for access in a 32-bit unit are always read as 0000h and writing to these bits is ignored.	23.2.18
		GTCCRn (n = A to F)			23.2.19
		GTPR			23.2.20
		GTPBR			23.2.21
		GTDVU			23.2.23

Table 1. 14 Specification Difference (14 of 20)

Specification			S3A7	S3A3	S3A3 HWM Reference
General PWM Timer (GPT)	Synchronized Operation by Hardware	GTCNT counters can be triggered by hardware sources	Output trigger input ELC event input GTIOCA/GTIOCB pin input	Output trigger input ELC event input	23.3.8.2
Asynchronous General Purpose Timer (AGT)	Condition before accessing the AGT registers after a cold start		Always set the VBTCR1.BPWSWSTP bit to 1	No prior conditions to access AGT register	
	I/O Pins	AGTIOn (n = 1, 2)	Can also be input during AGT operation using the voltage from the VBATT pin	Only P402 and P403 can be used as input	Table 24.2 24.2.10
	AGT I/O Control Register (AGTIOC)	Event counter mode operation performed during Software Standby mode	Battery backup function, and the digital filter function cannot be used	The digital filter function cannot be used	24.2.7
	Usage Notes when Count Source Clock Frequency is over 32 kHz		Refer to Manual	No such constraint	
USB 2.0 Full-Speed Module (USBFS)	HOCO clock that can be used as USB clock		No	Yes	Table 28.1
Serial Communications Interface (SCI)	Asynchronous Mode	Transmission/Reception	All SCI channels support FIFO	Only SCI0 and SCI1 support FIFO	Table 29.1

Table 1. 15 Specification Difference (15 of 20)

Specification			S3A7	S3A3	S3A3 HWM Reference
IrDA Interface	Interface sends and receives IrDA data communication waveforms in cooperation with the SCI1		Exists	Does Not Exist	
I2C Bus Interface (IIC)	I2C Bus Wakeup Unit Register 2 (ICWUR2)		Bit 0 is reserved	Bit 1 is Wakeup Function Synchronous Enable	30.2.12
			Bit 1 is reserved; Value after reset is 1	Bit 1 is Wakeup Function Asynchronous Operation Status Flag; Value after rest is 0	
			Bit 2 is reserved	Bit 2 is Wakeup Function Synchronous Operation Status Flag	
	Resets and Function States for ICWUR2 when issuing each condition		Not Applicable	Refer to Manual	30.15 Table 30.11
Serial Peripheral Interface (SPI)	Transmit/Receive Buffer		Both are 128 bit channels	SPI0: 128 bit SPI1: 32 bit	Table 32.1 32.3.10.1 (3)
	Maximum number of frames that can be transferred in one round of transmission or reception.		Four frames for both channels	SPI0: 4 frames SPI1: 1 frames	Table 32.1
	Control in master transfer	Burst Transfer	Available for all channels	Only available for SPI0	Table 32.1 32.3.10.1 (4)
	SPI Status Register (SPSR)	IDLNF flag, Master Mode Clearing Conditions	Refer to Manual	Refer to Manual	32.2.4

Table 1. 16 Specification Difference (16 of 20)

Specification			S3A7	S3A3	S3A3 HWM Reference
Serial Peripheral Interface (SPI)	SPI Sequence Register	Control (SPICR)	SPI0 and SPI1	SPI0	32.2.6
		Status (SPISR)	SPI0 and SPI1	SPI0	32.2.7
	SPI Data Control Register (SPDCR)	Bit 1, Bit 0	SPFC[1:0] for both channels	SPI0: SPFC[1:0] SPI1: Reserved	32.2.9
	SPI Command Registers 0 to 7 (SPCMD0 to SPCMD7)	Bit 7	SSLKP for both channels	SPI0: SSLKP SPI1: Reserved Refer to Manual	32.2.14
	Data Format	With Parity Disabled/Enabled	SPCMDm.SPB[3:0] for SPI0 and SPI1	SPCMDm.SPB[3:0] for SPI0, SPCMD0.SPB[3:0] for SPI1	32.3.4
Cyclic Redundancy Check (CRC) Calculator	Snoop Address Register (CRCSAR)	CRCSA[13:0] bits Allowed Addresses	Refer to Manual	Refer to Manual	34.2.5
Serial Sound Interface (SSI)	Provides functionality to interface with digital audio devices for transmitting PCM audio data over a serial bus with this MCU		SSI. Refer to Manual for details	SSI Enhanced (SSIE) Refer to Manual for details	Chapter 35
SD/MMC Host Interface (SDHI)	I/O Pins	SD0CD	Does Not Exist	Exists	Table 37.2
	SD Card Interrupt Flag Register 1 (SD_INFO1)		Bit 3 is reserved	Bit 3 is SDCDRM	36.2.10
			Bit 4 is reserved	Bit 4 is SDCDIN	
			Bit 5 is reserved. Value after reset is 1	Bit 5 is SDCDMON. Value after reset is undefined	
	SD INFO1 Interrupt Mask Register (SD_INFO1_MASK)		Bit 3 is reserved	Bit 3 is SDCDRMM	36.2.12
			Bit 4 is reserved	Bit 4 is SDCDINM	

Table 1. 17 Specification Difference (17 of 20)

Specification			S3A7	S3A3	S3A3 HWM Reference
SD/MMC Host Interface (SDHI)	SD Card Access Control Option Register (SD_OPTION)		Bit [3:0] are reserved	Bit [3:0] is CTOP [3:0]	36.2.16
	Operation	Card Detect	Refer to Manual	Refer to Manual	37.3.2.1
Boundary Scan	Register	ID Code Register	082D B447h	0834 1447h	Table 37.3
	USBFS dedicated pins (USB_DP and USB_DM)		Cannot be Boundary-Scanned	Can be Boundary-Scanned	37.4
14-Bit A/D Converter (ADC14)	Relationship between ADC14, OPAMP and ACMPLP		ACMPHS also there. Refer to Manual	Refer to Manual	38.8.13 Table 38.12
12-Bit D/A Converter (DAC12)	Output Channel		2 Channels	1 Channels	Table 39.1
	Event Link Function (input)		DA0 and DA1	DA0	Table 39.1 Table 39.2
	D/A Control Register		DADR0, DADR1	DADR0	39.2.1
	D/A Control Register (DACR)		Bit 7 is DAOE1	Bit 7 is reserved	39.2.2
Operational Amplifier (OPAMP)	OPAMP can be used to input signals to the respective positive and negative sides of the ACMPHS that provides output signals from the units		Yes	Not Applicable	Chapter 41
High-Speed Analog Comparator (ACMPHS)	Used to compare a test voltage with a reference voltage and to provide a digital output based on the result of conversion.		Exists	Does Not Exist	

Table 1. 18 Specification Difference (18 of 20)

Specification			S3A7	S3A3	S3A3 HWM Reference
Low Power Analog Comparator (ACMPLP)	Comparator Pin Configuration		Refer to Manual	Refer to Manual	Table 42.2
	ACMPLP Mode Setting Register (COMPMDR)		Refer to Manual	Refer to Manual	42.2.1
	Comparator Input Select Register (COMPSEL0)		Does Not Exist	Exists	42.2.4
	Comparator Reference Voltage Select Register (COMPSEL1)		Does Not Exist	Exists	42.2.5
	Procedure for setting the ACMPLP associated registers (i = 0, 1)		Refer to Manual	Refer to Manual	42.3
8-Bit D/A Converter (DAC8)	8-bit D/A converts data and does not include an output amplifier (DAC8). The DAC8 is used only as the reference voltage for ACMPLP.		Does Not Exist	Exists	Chapter 43
Capacitive Touch Sensing Unit (CTSU)	Pins	Electrostatic Capacitance Measurement	31 channels (TS00, TS01, TS03 to TS22, TS26 to TS27, TS29 to TS35)	27 channels (TS00 to TS13, TS17 to TS22, TS27 to TS31, TS34, TS35)	Table 44.1
	CTSU Measurement Channel Register 0 (CTSUMCH0)		CTSHMCH0[5:0] 31 channels	CTSHMCH0[5:0] 27 channels	44.2.5
	CTSU Measurement Channel Register 1 (CTSUMCH1)		CTSUMCH1[5:0] 31 channels	CTSUMCH1[5:0] 27 channels	44.2.6
	CTSU Channel Enable Control Register 0 (CTSUCHAC0)		CTSUCHAC0[7:0] specify bits TS00, TS01, and TS03 to TS07 pins.	CTSUCHAC0[7:0] specify bits TS00 to TS07 pins.	44.2.7
	CTSU Channel Enable Control Register 1 (CTSUCHAC1)		CTSUCHAC1[7:0] specify bits TS08 to TS15 pins.	CTSUCHAC1[7:0] specify bits TS08 to TS13 pins.	44.2.8

Table 1. 19 Specification Difference (19 of 20)

Specification			S3A7	S3A3	S3A3 HWM Reference
Capacitive Touch Sensing Unit (CTSU)	CTSU Channel Enable Control Register 2 (CTSUCHAC2)		CTSUCHAC2[7:0] specify bits TS16 to TS22 pins.	CTSUCHAC2[7:0] specify bits TS17 to TS22 pins.	44.2.9
	CTSU Channel Enable Control Register 3 (CTSUCHAC3)		CTSUCHAC3[7:0] specify bits TS26, TS27, and TS29 to TS31 pins.	CTSUCHAC0[7:0] specify bits TS27 to TS31 pins.	44.2.10
	CTSU Channel Enable Control Register 4 (CTSUCHAC4)		CTSUCHAC4[7:0] specify bits TS32 to TS35 pins.	CTSUCHAC4[7:0] specify bits TS34 and TS35 pins.	44.2.11
	CTSU Channel Transmit/Receive Control Register 0 (CTSUCHTRC0)		CTSUCHTRC0[7:0] specify bits TS00, TS01, and TS03 to TS07 pins	CTSUCHTRC0[7:0] specify bits TS00 to TS07 pins	44.2.12
	CTSU Channel Transmit/Receive Control Register 1 (CTSUCHTRC1)		CTSUCHTRC1[7:0] specify bits TS08 to TS15 pins.	CTSUCHTRC1[7:0] specify bits TS08 to TS13 pins.	45.2.13
	CTSU Channel Transmit/Receive Control Register 2 (CTSUCHTRC2)		CTSUCHTRC2[7:0] specify bits TS16 to TS22 pins.	CTSUCHTRC2[7:0] specify bits TS17 to TS22 pins.	45.2.14
	CTSU Channel Transmit/Receive Control Register 3 (CTSUCHTRC3)		CTSUCHTRC3[7:0] specify bits TS26, TS27, and TS29 to TS31 pins.	CTSUCHTRC3[7:0] specify bits TS27 to TS31 pins.	44.2.15
	CTSU Channel Transmit/Receive Control Register 4 (CTSUCHTRC4)		CTSUCHTRC4[3:0] specify bits TS32 to TS35 pins.	CTSUCHTRC4[3:0] specify bits TS34 and TS35 pins.	44.2.16
SRAM	SRAM Capacity	Without ECC	SRAM0: 112 KB SRAM1: 64 KB	SRAM0: 80 KB	Table 46.1

Table 1. 20 Specification Difference (20 of 20)

Specification			S3A7	S3A3	S3A3 HWM Reference
Flash Memory	Code Flash Memory Capacity		1 MB	512 KB	Table 47.1
	Data Flash Memory Capacity		16 KB	8 KB	
	Read and P/E addresses of code flash memory		Refer to Manual	Refer to Manual	Table 47.2
	Read and P/E addresses of data flash memory		Refer to Manual	Refer to Manual	Table 47.3
	Flash Cache 1 (FCACHE1)	Capacity	256 B	128 B	Table 47.4
		Associativity	8-way set associative, 4 entries/ways	2-way set associative, 8 entries/ways	
Segment LCD Controller (SLCDC)	SLCDC display function pins		SEG00 to SEG 51. Up to 52 segments × 4 commons, Up to 48 segments × 8 commons; Refer to Manual for additional differences.	SEG00 to SEG53. Up to 54 segments × 4 commons, Up to 50 segments × 8 commons; Refer to Manual for additional differences.	Table 48.1 to Table 48.9
Electrical Characteristics			Numerous differences; Refer to Manual	Numerous differences; Refer to Manual	Chapter 50

6. Port Select Function Difference

Tables 2.1, 3.1, and 4.1 compare the PSEL, ASEL, and ISEL functions for the Synergy S3A7 MCU Group and S3A3 MCU Group respectively. For each port number, the first row specifies the bitwise select values. The second row specifies the functionality enabled by the select values on the S3A7 MCU Group. The third column specifies the functionality enabled by the select values on the S3A3 MCU. Differences in functionality are notated with bold text and highlighted background. The comments section provides additional details or specifies the migration type from S3A7 MCU Group to S3A3 MCU Group. For more information on the comments column please refer to the Numbering Notation table in this application note.

Note: Some pin names have the added suffix of _A, _B, _C, _D, _E and _F. When assigning the GPT, IIC, SPI, SSIE, ETHERC (RMII), SDHI, and GLCDC functionality, select the functional pins with the same suffix. The other pins can be selected regardless of the suffix. **Assigning the same function to two or more pins simultaneously is prohibited.**

The following typographic notation is used for the pin differences sections of the document to denote the changes happening at the individual ports:

Example	Description
▲PIXD0_B	The '▲' denotes that signal PIXD0_B is being added to the previously unused/reserved or replacing a deprecated function.
▼ET1_TX_CLK	The '▼' denotes that signal ET1_TX_CLK is being deprecated at the bit position and being replaced by a new signal or remain unused/reserved.

The following gradients visualize whether signals are added, replaced, or removed from the Synergy S3A7 MCU and S3A3 MCU Group**.**

Example	Description
	Highlights a bit position where a new function is being added to the previously unused/reserved bit position.
	Highlights a bit position where a new function is replacing an existing function in the bit position.
	Highlights a bit position it is being reserved by deprecating the function that existed at that bit position.

Appendix 1. 64 Pin Package

Table 2. 1 64 Pin Package Difference (2.1 of 9)

Port	MCU	Select								Comments
P000		PSEL 01100B	ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL				▼IVREF0/IVCMP0
	S3A7	TS21	AN000	IVREF0/IVCMP0	AMP0+	IRQ6				
	S3A3	TS21	AN000	-	AMP0+	IRQ6				
P001		PSEL 01100B	ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL				▼IVREF1/IVCMP1
	S3A7	TS22	AN001	IVREF1/IVCMP1	AMP0-	IRQ7				
	S3A3	TS22	AN001	-	AMP0-	IRQ7				
P002		ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL					▲IRQ2
	S3A7	AN002	IVREF2/IVCMP2	AMP0O	IRQ8					▼IVREF2/IVCMP2
	S3A3	AN002	-	AMP0O	IRQ2					▼IRQ8
P003		ASEL ADC	ASEL CMP	ASEL OPAMP						▼IVREF3/IVCMP3
	S3A7	AN003	IVREF3/IVCMP3	AMP1O						
	S3A3	AN003	-	AMP1O						
P004		ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL					▲IRQ3, ▼IRQ9, ▼IVCMP0
	S3A7	AN004	IVCMP0	AMP2O	IRQ9					
	S3A3	AN004	-	AMP2O	IRQ3					
P010		PSEL 01100B	ASEL ADC	ASEL OPAMP	ISEL					▲AN005, ▼AN010
	S3A7	TS30	AN010	AMP2-	IRQ14					
	S3A3	TS30	AN005	AMP2-	IRQ14					
P011		PSEL 01100B	ASEL ADC	ASEL OPAMP	ISEL					▲AN006, ▼AN011
	S3A7	TS31	AN011	AMP2+	IRQ15					
	S3A3	TS31	AN006	AMP2+	IRQ15					

Table 2. 2 64 Pin Package Difference (2.2 of 9)

Port	MCU	Select								Comments
P012		ASEL ADC	ASEL OPAMP							▲AN007, ▼AN012
	S3A7	AN012	AMP1-							
	S3A3	AN007	AMP1-							
P013		ASEL ADC	ASEL OPAMP							▲AN013, ▼AN008
	S3A7	AN013	AMP1+							
	S3A3	AN008	AMP1+							
P014		ASEL ADC	ASEL CMP	ASEL DAC						▲AN009, ▼AN014, ▼IVREF5/IVREF2
	S3A7	AN014	IVREF5/IVREF2	DA0						
	S3A3	AN009	-	DA0						
P015		PSEL 01100B	ASEL ADC	ASEL CMP	ASEL DAC	ISEL				▲TS28, ▲AN010, ▲IRQ7, ▼AN015, ▼IVCMP5/IVCMP2, ▼DA1, ▼IRQ13
	S3A7	-	AN015	IVCMP5/IVCMP2	DA1	IRQ13				
	S3A3	TS28	AN010	-	-	IRQ7				
P100		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 00111B	PSEL 01000B	▲AN022, ▲GTIOC5B, ▼AN027
	S3A7	AGTIO0	GTETRGA	-	RXD0	SCK1	MISOA	SCL1	KR00	
	S3A3	AGTIO0	GTETRGA	GTIOC5B	RXD0	SCK1	MISOA	SCL1	KR00	
		PSEL 01011B	PSEL 01101B	ASEL ADC	ASEL CMP	ISEL				
	S3A7	D0	VL1	AN027	CMPIN0	IRQ2				
	S3A3	D0	VL1	AN022	CMPIN0	IRQ2				
P101		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 00111B	PSEL 01000B	▲AN021, ▲GTIOC5A, ▼AN026
	S3A7	AGTEE0	GTETRGB	-	TXD0	CTS1	MOSIA	SDA1	KR01	
	S3A3	AGTEE0	GTETRGB	GTIOC5A	TXD0	CTS1	MOSIA	SDA1	KR01	
		PSEL 01011B	PSEL 01101B	ASEL ADC	ASEL CMP	ISEL				
	S3A7	D1	VL2	AN026	CMPREF0	IRQ1				
	S3A3	D1	VL2	AN021	CMPREF0	IRQ1				

Table 2. 3 64 Pin Package Difference (2.3 of 9)

Port	MCU	Select								Comments
P102		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01000B	PSEL 01010B	▲TXD2, ▲CRX0, ▲AN020, ▼AN025
	S3A7	AGTO0	GTOWLO	GTIOC2B	SCK0	-	RSPCKA	KR02	ADTRG0	
	S3A3	AGTO0	GTOWLO	GTIOC2B	SCK0	TXD2	RSPCKA	KR02	ADTRG0	
		PSEL 01011B	PSEL 01101B	PSEL 10000B	ASEL ADC	ASEL CMP				
	S3A7	D2	VL3	-	AN025	CMPIN1				
	S3A3	D2	VL3	CRX0	AN020	CMPIN1				
P103		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00110B	PSEL 01000B	PSEL 01011B	PSEL 01101B	PSEL 10000B	▲CTX0, ▲AN019, ▼AN024
	S3A7	GTOWUP	GTIOC2A	CTS0	SSLA0	KR03	D3	VL4	-	
	S3A3	GTOWUP	GTIOC2A	CTS0	SSLA0	KR03	D3	VL4	CTX0	
		ASEL ADC	ASEL CMP							
	S3A7	AN024	CMPREF1							
	S3A3	AN019	CMPREF1							
P104		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00110B	PSEL 01000B	PSEL 01011B	PSEL 01100B	PSEL 01101B	▲GTIOC1B, ▲RXD0, ▲TS13
	S3A7	GTETRGB	-	-	SSLA1	KR04	D4	-	COM0	
	S3A3	GTETRGB	GTIOC1B	RXD0	SSLA1	KR04	D4	TS13	COM0	
		ISEL								
	S3A7	IRQ1								
	S3A3	IRQ1								
P105		PSEL 00010B	PSEL 00011B	PSEL 00110B	PSEL 01000B	PSEL 01011B	PSEL 01100B	PSEL 01101B	ISEL	▲GTIOC1A, ▲TS34
	S3A7	GTETRGA	-	SSLA2	KR05	D5	-	COM1	IRQ0	
	S3A3	GTETRGA	GTIOC1A	SSLA2	KR05	D5	TS34	COM1	IRQ0	
P108		PSEL 00000B	PSEL 00010B	PSEL 00011B	PSEL 00101B	PSEL 00110B				▲GTOULO
	S3A7	TMS/SWDIO	-	GTIOC0B	CTS9	SSLB0				
	S3A3	TMS/SWDIO	GTOULO	GTIOC0B	CTS9	SSLB0				

Table 2. 4 64 Pin Package Difference (2.4 of 9)

Port	MCU	Select								Comments
P109		PSEL 00000B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01001B	PSEL 01100B	▲SCK1, ▲TS10, ▲SEG52, ▲CTX0
	S3A7	TDO/TRACESWO	GTOVUP	GTIOC1A	-	TXD9	MOSIB	CLKOUT	-	
	S3A3	TDO/TRACESWO	GTOVUP	GTIOC1A	SCK1	TXD9	MOSIB	CLKOUT	TS10	
		PSEL 01101B	PSEL 10000B							
	S3A7	-	-							
	S3A3	SEG52	CTX0							
P110		PSEL 00000B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01001B	PSEL 01101B	▲SEG53, ▲CRX0
	S3A7	TDI	GTOVLO	GTIOC1B	CTS2	RXD9	MISOB	VCOUT	-	
	S3A3	TDI	GTOVLO	GTIOC1B	CTS2	RXD9	MISOB	VCOUT	SEG53	
		PSEL 10000B	ISEL							
	S3A7	-	IRQ3							
	S3A3	CRX0	IRQ3							
P111		PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01011B	PSEL 01100B	PSEL 01101B	ISEL	▲TS12
	S3A7	GTIOC3A	SCK2	SCK9	RSPCKB	A5	-	CAPH	IRQ4	
	S3A3	GTIOC3A	SCK2	SCK9	RSPCKB	A5	TS12	CAPH	IRQ4	
P112		PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01011B	PSEL 01100B	PSEL 01101B	PSEL 10010B	▲SCK1, ▲SSLB0, ▲TSCAP
	S3A7	GTIOC3B	TXD2	-	-	A4	-	CAPL	SSISCK0	
	S3A3	GTIOC3B	TXD2	SCK1	SSLB0	A4	TSCAP	CAPL	SSISCK0	
P113		PSEL 00011B	PSEL 00100B	PSEL 01011B	PSEL 01100B	PSEL 01101B	PSEL 10010B			▲GTIOC2A, ▲TS27 ▲SSILRCK0/SSIFS0
	S3A7	-	RXD2	A3	-	SEG0/COM4	SSIWS0			
	S3A3	GTIOC2A	RXD2	A3	TS27	SEG0/COM4	SSILRCK0/SSIFS0			▼SSIWS0

Table 2. 5 64 Pin Package Difference (2.5 of 9)

Port	MCU	Select								Comments
P204		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 00111B	PSEL 01010B	▲A18 ▼SSISCK1
	S3A7	AGTIO1	GTIW	GTIOC4B	SCK4	SCK9	RSPCKB	SCL0	CACREF	
	S3A3	AGTIO1	GTIW	GTIOC4B	SCK4	SCK9	RSPCKB	SCL0	CACREF	
		PSEL 01011B	PSEL 01100B	PSEL 01101B	PSEL 10010B	PSEL 10011B	PSEL 10101B			
	S3A7	-	TS0	SEG23	SSISCK1	USB_OVRCURB	SD0DAT4			
	S3A3	A18	TS0	SEG23	-	USB_OVRCURB	SD0DAT4			
P205		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 00111B	PSEL 01001B	▲SEG20, ▼SSIWS1
	S3A7	AGTO1	GTIV	GTIOC4A	TXD4	CTS9	SSLB0	SCL1	CLKOUT	
	S3A3	AGTO1	GTIV	GTIOC4A	TXD4	CTS9	SSLB0	SCL1	CLKOUT	
		PSEL 01011B	PSEL 01100B	PSEL 01101B	PSEL 10010B	PSEL 10011B	PSEL 10101B	ISEL		
	S3A7	A16	TSCAP	-	SSIWS1	USB_OVRCURA	SD0DAT3	IRQ1		
	S3A3	A16	TSCAP	SEG20	-	USB_OVRCURA	SD0DAT3	IRQ1		
P206		PSEL 00010B	PSEL 00100B	PSEL 00110B	PSEL 00111B	PSEL 01011B	PSEL 01100B	PSEL 01101B	PSEL 10010B	▲SEG12, ▼SSIDATA1
	S3A7	GTIU	RXD4	SSLB1	SDA1	WAIT	TS1	-	SSIDATA1	
	S3A3	GTIU	RXD4	SSLB1	SDA1	WAIT	TS1	SEG12	-	
		PSEL 10011B	PSEL 10101B	ISEL						
	S3A7	USB_VBUSEN	SD0DAT2	IRQ0						
	S3A3	USB_VBUSEN	SD0DAT2	IRQ0						
P212/EXTAL		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00101B	ISEL				▲GTETRGB, ▲GTIOC0B, ▼GTETRGD
	S3A7	AGTEE1	GTETRGD	-	RXD1	IRQ3				
	S3A3	AGTEE1	GTETRGB	GTIOC0B	RXD1	IRQ3				
P213/XTAL		PSEL 00010B	PSEL 00011B	PSEL 00101B	ISEL					▲GTETRGA, ▲GTIOC0A, ▼GTETRGC
	S3A7	GTETRGC	-	TXD1	IRQ2					
	S3A3	GTETRGA	GTIOC0A	TXD1	IRQ2					

Table 2. 6 64 Pin Package Difference (6 of 9)

Port	MCU	Select								Comments
P300		PSEL 00000B	PSEL 00010B	PSEL 00011B	PSEL 00110B					▲GTOUUP
	S3A7	TCK/SWCLK	-	GTIOC0A	SSLB1					
	S3A3	TCK/SWCLK	GTOUUP	GTIOC0A	SSLB1					
P301		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01011B	PSEL 01100B	▲AGTIO0, ▲CTS9, ▲TS9
	S3A7	-	GTOULO	GTIOC4B	RXD2	-	SSLB2	A6	-	
	S3A3	AGTIO0	GTOULO	GTIOC4B	RXD2	CTS9	SSLB2	A6	TS9	
		PSEL 01101B	ISEL							
	S3A7	SEG1/COM5	IRQ6							
	S3A3	SEG1/COM5	IRQ6							
P302		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00110B	PSEL 01011B	PSEL 01100B	PSEL 01101B	ISEL	▲TS8
	S3A7	GTOUUP	GTIOC4A	TXD2	SSLB3	A7	-	SEG2/COM6	IRQ5	
	S3A3	GTOUUP	GTIOC4A	TXD2	SSLB3	A7	TS8	SEG2/COM6	IRQ5	
P303		PSEL 00011B	PSEL 01011B	PSEL 01100B	PSEL 01101B	PSEL 10101B				▲TS2, ▲SD0DAT0
	S3A7	GTIOC7B	A8	-	SEG3/COM7	-				
	S3A3	GTIOC7B	A8	TS2	SEG3/COM7	SD0DAT0				
P304		PSEL 00011B	PSEL 01011B	PSEL 01100B	PSEL 01101B	PSEL 10101B	ISEL			▲TS11, ▲SD0WP
	S3A7	GTIOC7A	A9	-	SEG17	-	IRQ9			
	S3A3	GTIOC7A	A9	TS11	SEG17	SD0WP	IRQ9			
P400		PSEL 00001B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00111B	PSEL 01010B	PSEL 01100B	PSEL 01101B	▲AGTIO1, ▲SCK1, ▲CACREF, ▲SEG4
	S3A7	-	GTIOC6A	SCK4	-	SCL0	-	TS20	-	
	S3A3	AGTIO1	GTIOC6A	SCK4	SCK1	SCL0	CACREF	TS20	SEG4	
		PSEL 10010B	ISEL							
	S3A7	AUDIO_CLK	IRQ0							
	S3A3	AUDIO_CLK	IRQ0							

Table 2. 7 64 Pin Package Difference (7 of 9)

Port	MCU	Select								Comments
P401		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00111B	PSEL 01100B	PSEL 01101B	PSEL 10000B	▲TDX1, ▲SEG5
	S3A7	GTETRGA	GTIOC6B	CTS4	-	SDA0	TS19	-	CTX0	
	S3A3	GTETRGA	GTIOC6B	CTS4	TXD1	SDA0	TS19	SEG5	CTX0	
		ISEL								
	S3A7	IRQ5								
	S3A3	IRQ5								
P402		PSEL 00001B	PSEL 00101B	PSEL 01100B	PSEL 01101B	PSEL 10000B	ISEL	PSEL Don't Care		▲RXD1, ▲SEG6, ▲AGTIO0_E/AGTIO1
	S3A7	-	-	TS18	-	CRX0	IRQ4	RTCIC0/AGTIO0/ AGTIO1		
	S3A3	AGTIO0_E/AGTIO1	RXD1	TS18	SEG6	CRX0	IRQ4	RTCIC0		
P407		PSEL 00001B	PSEL 00100B	PSEL 00110B	PSEL 00111B	PSEL 01001B	PSEL 01010B	PSEL 01100B	PSEL 01101B	▲AGTIO0, ▲SEG11
	S3A7	-	CTS4	SSLB3	SDA0	RTCOUT	ADTRG0	TS3	-	
	S3A3	AGTIO0	CTS4	SSLB3	SDA0	RTCOUT	ADTRG0	TS3	SEG11	
		PSEL 10011B								
	S3A7	USB_VBUS								
	S3A3	USB_VBUS								
P408		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00111B	PSEL 01100B	PSEL 01101B	PSEL 10011B	▲GTIOC5B, ▲CTS1, ▲SCL0, ▲SEG10
	S3A7	GTOWLO	-	-	RXD3	-	TS4	-	USB_ID	
	S3A3	GTOWLO	GTIOC5B	CTS1	RXD3	SCL0	TS4	SEG10	USB_ID	
		ISEL								
	S3A7	IRQ7								
	S3A3	IRQ7								
P409		PSEL 00010B	PSEL 00011B	PSEL 00101B	PSEL 01100B	PSEL 01101B	PSEL 10011B	ISEL		▲GTIOC5A, ▲SEG9
	S3A7	GTOWUP	-	TXD3	TS5	-	USB_EXICEN	IRQ6		
	S3A3	GTOWUP	GTIOC5A	TXD3	TS5	SEG9	USB_EXICEN	IRQ6		

Table 2. 8 64 Pin Package Difference (8 of 9)

Port	MCU	Select								Comments
P410		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01100B	PSEL 01101B	▲SEG8
	S3A7	AGTOB1	GTOVLO	GTIOC9B	RXD0	SCK3	MISOA	TS6	-	
	S3A3	AGTOB1	GTOVLO	GTIOC9B	RXD0	SCK3	MISOA	TS6	SEG8	
		PSEL 10101B	ISEL							
	S3A7	SD0DAT1	IRQ5							
	S3A3	SD0DAT1	IRQ5							
P411		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01100B	PSEL 01101B	▲SEG7
	S3A7	AGTOA1	GTOVUP	GTIOC9A	TXD0	CTS3	MOSIA	TS7	-	
	S3A3	AGTOA1	GTOVUP	GTIOC9A	TXD0	CTS3	MOSIA	TS7	SEG7	
		PSEL 10101B	ISEL							
	S3A7	SD0DAT0	IRQ4							
	S3A3	SD0DAT0	IRQ4							
P500		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 01101B	PSEL 10001B	PSEL 10011B	ASEL ADC	ASEL CMP	▲GTIOC2A, ▲CMPREF1
	S3A7	AGTOA0	GTIU	-	SEG48	QSPCLK	USB_VBUSEN	AN016	-	
	S3A3	AGTOA0	GTIU	GTIOC2A	SEG48	QSPCLK	USB_VBUSEN	AN016	CMPREF1	
P501		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00101B	PSEL 01101B	PSEL 10001B	PSEL 10011B	ASEL ADC	▲GTIOC2B, ▲TXD3, ▲CMPIN1
	S3A7	AGTOB0	GTIV	-	-	SEG49	QSSL	USB_OVRCURA	AN017	
	S3A3	AGTOB0	GTIV	GTIOC2B	TXD3	SEG49	QSSL	USB_OVRCURA	AN017	
		ASEL CMP	ISEL							
	S3A7	-	IRQ11							
	S3A3	CMPIN1	IRQ11							

Table 2. 9 64 Pin Package Difference (9 of 9)

Port	MCU	Select								Comments
		PSEL 00010B	PSEL 00011B	PSEL 00101B	PSEL 01101B	PSEL 10001B	PSEL 10011B	ASEL ADC	ASEL CMP	▲GTIOC3B, ▲RXD3, ▲CMPREF0
P502	S3A7	GTIW	-	-	SEG50	QIO0	USB_OVRCURB	AN018	-	
	S3A3	GTIW	GTIOC3B	RXD3	SEG50	QIO0	USB_OVRCURB	AN018	CMPREF0	
		ISEL								
	S3A7	IRQ12								
	S3A3	IRQ12								

Appendix 2. 100 Pin Package

Table 3. 1 100 Pin Package Difference (1 of 13)

Port	MCU	Select								Comments
P000		PSEL 01100B	ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL				▼IVREF0/IVCMP0
	S3A7	TS21	AN000	IVREF0/IVCMP0	AMP0+	IRQ6				
	S3A3	TS21	AN000	-	AMP0+	IRQ6				
P001		PSEL 01100B	ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL				▼IVREF1/IVCMP1
	S3A7	TS22	AN001	IVREF1/IVCMP1	AMP0-	IRQ7				
	S3A3	TS22	AN001	-	AMP0-	IRQ7				
P002		ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL					▲IRQ2
	S3A7	AN002	IVREF2/IVCMP2	AMP0O	IRQ8					▼IVREF2/IVCMP2
	S3A3	AN002	-	AMP0O	IRQ2					▼IRQ8
P003		ASEL ADC	ASEL CMP	ASEL OPAMP						▼IVREF3/IVCMP3
	S3A7	AN003	IVREF3/IVCMP3	AMP1O						
	S3A3	AN003	-	AMP1O						
P004		ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL					▲IRQ3, ▼IRQ9, ▼IVCMP0
	S3A7	AN004	IVCMP0	AMP2O	IRQ9					
	S3A3	AN004	-	AMP2O	IRQ3					
P005		PSEL 01100B	ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL				▲AN011, ▼TS26, ▼AN005, ▼IVREF0
	S3A7	TS26	AN005	IVREF0	AMP3+	IRQ10				
	S3A3	-	AN011	-	AMP3+	IRQ10				
P006		PSEL 01100B	ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL				▲AN012, ▼TS27, ▼IVREF4/IVREF1, ▼AN006
	S3A7	TS27	AN006	IVREF4/IVREF1	AMP3-	IRQ11				
	S3A3	-	AN012	-	AMP3-	IRQ11				

Table 3. 2 100 Pin Package Difference (2 of 13)

Port	MCU	Select								Comments
P007		ASEL ADC	ASEL CMP	ASEL OPAMP						▲AN013, ▼AN007, ▼IVCMP4/IVCMP1
	S3A7	AN007	IVCMP4/IVCMP1	AMP3O						
	S3A3	AN013	-	AMP3O						
P008		PSEL 01100B	ASEL ADC	ISEL						▲AN014, ▼TS29, ▼AN008
	S3A7	TS29	AN008	IRQ12						
	S3A3	-	AN014	IRQ12						
P010		PSEL 01100B	ASEL ADC	ASEL OPAMP	ISEL					▲AN005, ▼AN010
	S3A7	TS30	AN010	AMP2-	IRQ14					
	S3A3	TS30	AN005	AMP2-	IRQ14					
P011		PSEL 01100B	ASEL ADC	ASEL OPAMP	ISEL					▲AN006, ▼AN011
	S3A7	TS31	AN011	AMP2+	IRQ15					
	S3A3	TS31	AN006	AMP2+	IRQ15					
P012		ASEL ADC	ASEL OPAMP							▲AN007, ▼AN012
	S3A7	AN012	AMP1-							
	S3A3	AN007	AMP1-							
P013		ASEL ADC	ASEL OPAMP							▲AN013, ▼AN008
	S3A7	AN013	AMP1+							
	S3A3	AN008	AMP1+							
P014		ASEL ADC	ASEL CMP	ASEL DAC						▲AN009, ▼AN014, ▼IVREF5/IVREF2
	S3A7	AN014	IVREF5/IVREF2	DA0						
	S3A3	AN009	-	DA0						
P015		PSEL 01100B	ASEL ADC	ASEL CMP	ASEL DAC	ISEL				▲TS28, ▲AN010, ▲IRQ7, ▼AN015, ▼IVCMP5/IVCMP2, ▼DA1, ▼IRQ13
	S3A7	-	AN015	IVCMP5/IVCMP2	DA1	IRQ13				
	S3A3	TS28	AN010	-	-	IRQ7				

Table 3. 3 100 Pin Package Difference (3 of 13)

Port	MCU	Select								Comments
P100		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 00111B	PSEL 01000B	▲AN022, ▲GTIOC5B, ▼AN027
	S3A7	AGTIO0	GTETRGA	-	RXD0	SCK1	MISOA	SCL1	KR00	
	S3A3	AGTIO0	GTETRGA	GTIOC5B	RXD0	SCK1	MISOA	SCL1	KR00	
		PSEL 01011B	PSEL 01101B	ASEL ADC	ASEL CMP	ISEL				
	S3A7	D0	VL1	AN027	CMPIN0	IRQ2				
	S3A3	D0	VL1	AN022	CMPIN0	IRQ2				
P101		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 00111B	PSEL 01000B	▲AN021, ▲GTIOC5A, ▼AN026
	S3A7	AGTEE0	GTETRGB	-	TXD0	CTS1	MOSIA	SDA1	KR01	
	S3A3	AGTEE0	GTETRGB	GTIOC5A	TXD0	CTS1	MOSIA	SDA1	KR01	
		PSEL 01011B	PSEL 01101B	ASEL ADC	ASEL CMP	ISEL				
	S3A7	D1	VL2	AN026	CMPREF0	IRQ1				
	S3A3	D1	VL2	AN021	CMPREF0	IRQ1				
P102		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01000B	PSEL 01010B	▲TXD2, ▲CRX0, ▲AN020, ▼AN025
	S3A7	AGTO0	GTOWLO	GTIOC2B	SCK0	-	RSPCKA	KR02	ADTRG0	
	S3A3	AGTO0	GTOWLO	GTIOC2B	SCK0	TXD2	RSPCKA	KR02	ADTRG0	
		PSEL 01011B	PSEL 01101B	PSEL 10000B	ASEL ADC	ASEL CMP				
	S3A7	D2	VL3	-	AN025	CMPIN1				
	S3A3	D2	VL3	CRX0	AN020	CMPIN1				
P103		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00110B	PSEL 01000B	PSEL 01011B	PSEL 01101B	PSEL 10000B	▲CTX0, ▲AN019, ▼AN024
	S3A7	GTOWUP	GTIOC2A	CTS0	SSLA0	KR03	D3	VL4	-	
	S3A3	GTOWUP	GTIOC2A	CTS0	SSLA0	KR03	D3	VL4	CTX0	
		ASEL ADC	ASEL CMP							
	S3A7	AN024	CMPREF1							
	S3A3	AN019	CMPREF1							

Table 3. 4 100 Pin Package Difference (4 of 13)

Port	MCU	Select								Comments
P104		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00110B	PSEL 01000B	PSEL 01011B	PSEL 01100B	PSEL 01101B	▲GTIOC1B, ▲RXD0, ▲TS13
	S3A7	GTETRGB	-	-	SSLA1	KR04	D4	-	COM0	
	S3A3	GTETRGB	GTIOC1B	RXD0	SSLA1	KR04	D4	TS13	COM0	
		ISEL								
	S3A7	IRQ1								
	S3A3	IRQ1								
P105		PSEL 00010B	PSEL 00011B	PSEL 00110B	PSEL 01000B	PSEL 01011B	PSEL 01100B	PSEL 01101B	ISEL	▲GTIOC1A, ▲TS34
	S3A7	GTETRGA	-	SSLA2	KR05	D5	-	COM1	IRQ0	
	S3A3	GTETRGA	GTIOC1A	SSLA2	KR05	D5	TS34	COM1	IRQ0	
P108		PSEL 00000B	PSEL 00010B	PSEL 00011B	PSEL 00101B	PSEL 00110B				▲GTOULO
	S3A7	TMS/SWDIO	-	GTIOC0B	CTS9	SSLB0				
	S3A3	TMS/SWDIO	GTOULO	GTIOC0B	CTS9	SSLB0				
P109		PSEL 00000B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01001B	PSEL 01100B	▲SCK1, ▲TS10, ▲SEG52, ▲CTX0
	S3A7	TDO/TRACESWO	GTOVUP	GTIOC1A	-	TXD9	MOSIB	CLKOUT	-	
	S3A3	TDO/TRACESWO	GTOVUP	GTIOC1A	SCK1	TXD9	MOSIB	CLKOUT	TS10	
		PSEL 01101B	PSEL 10000B							
	S3A7	-	-							
	S3A3	SEG52	CTX0							
P110		PSEL 00000B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01001B	PSEL 01101B	▲SEG53, ▲CRX0
	S3A7	TDI	GTOVLO	GTIOC1B	CTS2	RXD9	MISOB	VCOUT	-	
	S3A3	TDI	GTOVLO	GTIOC1B	CTS2	RXD9	MISOB	VCOUT	SEG53	
		PSEL 10000B	ISEL							
	S3A7	-	IRQ3							
	S3A3	CRX0	IRQ3							

Table 3. 5 100 Pin Package Difference (5 of 13)

Port	MCU	Select								Comments
P111		PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01011B	PSEL 01100B	PSEL 01101B	ISEL	▲TS12
	S3A7	GTIOC3A	SCK2	SCK9	RSPCKB	A5	-	CAPH	IRQ4	
	S3A3	GTIOC3A	SCK2	SCK9	RSPCKB	A5	TS12	CAPH	IRQ4	
P112		PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01011B	PSEL 01100B	PSEL 01101B	PSEL 10010B	▲SCK1, ▲SSLB0, ▲TSCAP
	S3A7	GTIOC3B	TXD2	-	-	A4	-	CAPL	SSISCK0	
	S3A3	GTIOC3B	TXD2	SCK1	SSLB0	A4	TSCAP	CAPL	SSISCK0	
P113		PSEL 00011B	PSEL 00100B	PSEL 01011B	PSEL 01100B	PSEL 01101B	PSEL 10010B			▲GTIOC2A, ▲TS27
	S3A7	-	RXD2	A3	-	SEG0/COM4	SSIWS0			
	S3A3	GTIOC2A	RXD2	A3	TS27	SEG0/COM4	SSILRCK0/SSIFS0			
P114		PSEL 00011B	PSEL 01011B	PSEL 01100B	PSEL 01101B	PSEL 10010B				▲GTIOC2B, ▲TS29
	S3A7	-	A2	-	SEG24	SSIRXD0				
	S3A3	GTIOC2B	A2	TS29	SEG24	SSIRXD0				
P115		PSEL 00011B	PSEL 01011B	PSEL 01100B	PSEL 01101B	PSEL 10010B				▲GTIOC4A, ▲TS35
	S3A7	-	A1	-	SEG25	SSITXD0				
	S3A3	GTIOC4A	A1	TS35	SEG25	SSITXD0				
P202		PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01011B	PSEL 01101B	PSEL 10000B	PSEL 10101B	▼CRX0
	S3A7	GTIOC5B	SCK2	RXD9	MISOB	WR1/BC1	SEG21	CRX0	SD0DAT6	
	S3A3	GTIOC5B	SCK2	RXD9	MISOB	WR1/BC1	SEG21	-	SD0DAT6	
		ISEL								
	S3A7	IRQ3								
	S3A3	IRQ3								

Table 3. 6 100 Pin Package Difference (6 of 13)

Port	MCU	Select								Comments
P203		PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01011B	PSEL 01100B	PSEL 01101B	PSEL 10000B	▲A19, ▼CTX0
	S3A7	GTIOC5A	CTS2	TXD9	MOSIB	-	TSCAP	SEG22	CTX0	
	S3A3	GTIOC5A	CTS2	TXD9	MOSIB	A19	TSCAP	SEG22	-	
		PSEL 10101B	ISEL							
	S3A7	SD0DAT5	IRQ2							
	S3A3	SD0DAT5	IRQ2							
P204		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 00111B	PSEL 01010B	▲A18, ▼SSISCK1
	S3A7	AGTIO1	GTIW	GTIOC4B	SCK4	SCK9	RSPCKB	SCL0	CACREF	
	S3A3	AGTIO1	GTIW	GTIOC4B	SCK4	SCK9	RSPCKB	SCL0	CACREF	
		PSEL 01011B	PSEL 01100B	PSEL 01101B	PSEL 10010B	PSEL 10011B	PSEL 10101B			
	S3A7	-	TS0	SEG23	SSISCK1	USB_OVRCURB	SD0DAT4			
	S3A3	A18	TS0	SEG23	-	USB_OVRCURB	SD0DAT4			
P205		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 00111B	PSEL 01001B	▲SEG20, ▼SSIWS1
	S3A7	AGTO1	GTIV	GTIOC4A	TXD4	CTS9	SSLB0	SCL1	CLKOUT	
	S3A3	AGTO1	GTIV	GTIOC4A	TXD4	CTS9	SSLB0	SCL1	CLKOUT	
		PSEL 01011B	PSEL 01100B	PSEL 01101B	PSEL 10010B	PSEL 10011B	PSEL 10101B	ISEL		
	S3A7	A16	TSCAP	-	SSIWS1	USB_OVRCURA	SD0DAT3	IRQ1		
	S3A3	A16	TSCAP	SEG20	-	USB_OVRCURA	SD0DAT3	IRQ1		
P206		PSEL 00010B	PSEL 00100B	PSEL 00110B	PSEL 00111B	PSEL 01011B	PSEL 01100B	PSEL 01101B	PSEL 10010B	▲SEG12, ▼SSIDATA1
	S3A7	GTIU	RXD4	SSLB1	SDA1	WAIT	TS1	-	SSIDATA1	
	S3A3	GTIU	RXD4	SSLB1	SDA1	WAIT	TS1	SEG12	-	
		PSEL 10011B	PSEL 10101B	ISEL						
	S3A7	USB_VBUSEN	SD0DAT2	IRQ0						
	S3A3	USB_VBUSEN	SD0DAT2	IRQ0						

Table 3. 7 100 Pin Package Difference (7 of 13)

Port	MCU	Select								Comments
P212/EXTAL		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00101B	ISEL				▲GTETRGB, ▲GTIOC0B, ▼GTETRGD
	S3A7	AGTEE1	GTETRGD	-	RXD1	IRQ3				
	S3A3	AGTEE1	GTETRGB	GTIOC0B	RXD1	IRQ3				
P213/XTAL		PSEL 00010B	PSEL 00011B	PSEL 00101B	ISEL					▲GTETRGA, ▲GTIOC0A, ▼GTETRGC
	S3A7	GTETRGC	-	TXD1	IRQ2					
	S3A3	GTETRGA	GTIOC0A	TXD1	IRQ2					
P300		PSEL 00000B	PSEL 00010B	PSEL 00011B	PSEL 00110B					▲GTOUUP
	S3A7	TCK/SWCLK	-	GTIOC0A	SSLB1					
	S3A3	TCK/SWCLK	GTOUUP	GTIOC0A	SSLB1					
P301		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01011B	PSEL 01100B	▲AGTIO0, ▲CTS9, ▲TS9
	S3A7	-	GTOULO	GTIOC4B	RXD2	-	SSLB2	A6	-	
	S3A3	AGTIO0	GTOULO	GTIOC4B	RXD2	CTS9	SSLB2	A6	TS9	
		PSEL 01101B	ISEL							
	S3A7	SEG1/COM5	IRQ6							
	S3A3	SEG1/COM5	IRQ6							
P302		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00110B	PSEL 01011B	PSEL 01100B	PSEL 01101B	ISEL	▲TS8
	S3A7	GTOUUP	GTIOC4A	TXD2	SSLB3	A7	-	SEG2/COM6	IRQ5	
	S3A3	GTOUUP	GTIOC4A	TXD2	SSLB3	A7	TS8	SEG2/COM6	IRQ5	
P303		PSEL 00011B	PSEL 01011B	PSEL 01100B	PSEL 01101B	PSEL 10101B				▲TS2, ▲SD0DAT0
	S3A7	GTIOC7B	A8	-	SEG3/COM7	-				
	S3A3	GTIOC7B	A8	TS2	SEG3/COM7	SD0DAT0				
P304		PSEL 00011B	PSEL 01011B	PSEL 01100B	PSEL 01101B	PSEL 10101B	ISEL			▲TS11, ▲SD0WP
	S3A7	GTIOC7A	A9	-	SEG17	-	IRQ9			
	S3A3	GTIOC7A	A9	TS11	SEG17	SD0WP	IRQ9			

Table 3. 8 100 Pin Package Difference (8 of 13)

Port	MCU	Select								Comments
P305		PSEL 01011B	PSEL 01101B	PSEL 10001B	PSEL 10101B	ISEL				▲QSPCLK, ▲SD0CD
	S3A7	A10	SEG16	-	-	IRQ8				
	S3A3	A10	SEG16	QSPCLK	SD0CD	IRQ8				
P306		PSEL 01011B	PSEL 01101B	PSEL 10001B						▲QSSL
	S3A7	A11	SEG15	-						
	S3A3	A11	SEG15	QSSL						
P307		PSEL 01011B	PSEL 01101B	PSEL 10001B						▲QIO0
	S3A7	A12	SEG14	-						
	S3A3	A12	SEG14	QIO0						
P400		PSEL 00001B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00111B	PSEL 01010B	PSEL 01100B	PSEL 01101B	▲AGTIO1, ▲SCK1, ▲CACREF, ▲SEG4
	S3A7	-	GTIOC6A	SCK4	-	SCL0	-	TS20	-	
	S3A3	AGTIO1	GTIOC6A	SCK4	SCK1	SCL0	CACREF	TS20	SEG4	
		PSEL 10010B	ISEL							
	S3A7	AUDIO_CLK	IRQ0							
	S3A3	AUDIO_CLK	IRQ0							
P401		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00111B	PSEL 01100B	PSEL 01101B	PSEL 10000B	▲TDX1, ▲SEG5
	S3A7	GTETRGA	GTIOC6B	CTS4	-	SDA0	TS19	-	CTX0	
	S3A3	GTETRGA	GTIOC6B	CTS4	TXD1	SDA0	TS19	SEG5	CTX0	
		ISEL								
	S3A7	IRQ5								
	S3A3	IRQ5								

Table 3. 9 100 Pin Package Difference (9 of 13)

Port	MCU	Select								Comments
P402		PSEL 00001B	PSEL 00101B	PSEL 01100B	PSEL 01101B	PSEL 10000B	ISEL	PSEL Don't Care		▲RXD1, ▲SEG6, ▲AGTIO0_E/AGTIO1
	S3A7	-	-	TS18	-	CRX0	IRQ4	RTCIC0/AGTIO0/ AGTIO1		
	S3A3	AGTIO0_E/AGTIO1	RXD1	TS18	SEG6	CRX0	IRQ4	RTCIC0		
P403		PSEL 00001B	PSEL 00011B	PSEL 00101B	PSEL 01100B	PSEL 10010B	PSEL Don't Care			▲CTS1 ▲AGTIO0_F/AGTIO1
	S3A7	-	GTIOC3A	-	TS17	SSISCK0	RTCIC1/AGTIO0/ AGTIO1			
	S3A3	AGTIO0_F/AGTIO1	GTIOC3A	CTS1	TS17	SSISCK0	RTCIC1			
P404		PSEL 00011B	PSEL 01100B	PSEL 10010B	PSEL Don't Care					▼TS16
	S3A7	GTIOC3B	TS16	SSIWS0	RTCIC2					
	S3A3	GTIOC3B	-	SSIWS0	RTCIC2					
P405		PSEL 00011B	PSEL 01100B	PSEL 10010B						▼TS15
	S3A7	GTIOC1A	TS15	SSITXD0						
	S3A3	GTIOC1A	-	SSITXD0						
P406		PSEL 00011B	PSEL 00110B	PSEL 01100B	PSEL 10010B					▲SSLA3, ▼TS14
	S3A7	GTIOC1B	-	TS14	SSIRXD0					
	S3A3	GTIOC1B	SSLA3	-	SSIRXD0					
P407		PSEL 00001B	PSEL 00100B	PSEL 00110B	PSEL 00111B	PSEL 01001B	PSEL 01010B	PSEL 01100B	PSEL 01101B	▲AGTIO0, ▲SEG11
	S3A7	-	CTS4	SSLB3	SDA0	RTCOUT	ADTRG0	TS3	-	
	S3A3	AGTIO0	CTS4	SSLB3	SDA0	RTCOUT	ADTRG0	TS3	SEG11	
		PSEL 10011B								
	S3A7	USB_VBUS								
	S3A3	USB_VBUS								

Table 3. 10 100 Pin Package Difference (10 of 13)

Port	MCU	Select								Comments
P402		PSEL 00001B	PSEL 00101B	PSEL 01100B	PSEL 01101B	PSEL 10000B	ISEL	PSEL Don't Care		▲RXD1, ▲SEG6, ▲AGTIO0_E/AGTIO1
	S3A7	-	-	TS18	-	CRX0	IRQ4	RTCIC0/AGTIO0/ AGTIO1		
	S3A3	AGTIO0_E/AGTIO1	RXD1	TS18	SEG6	CRX0	IRQ4	RTCIC0		
P403		PSEL 00001B	PSEL 00011B	PSEL 00101B	PSEL 01100B	PSEL 10010B	PSEL Don't Care			▲CTS1 ▲AGTIO0_F/AGTIO1
	S3A7	-	GTIOC3A	-	TS17	SSISCK0	RTCIC1/AGTIO0/ AGTIO1			
	S3A3	AGTIO0_F/AGTIO1	GTIOC3A	CTS1	TS17	SSISCK0	RTCIC1			
P404		PSEL 00011B	PSEL 01100B	PSEL 10010B	PSEL Don't Care					▼TS16
	S3A7	GTIOC3B	TS16	SSIWS0	RTCIC2					
	S3A3	GTIOC3B	-	SSILRCK0/SSIFS0	RTCIC2					
P405		PSEL 00011B	PSEL 01100B	PSEL 10010B						▼TS15
	S3A7	GTIOC1A	TS15	SSITXD0						
	S3A3	GTIOC1A	-	SSITXD0						
P406		PSEL 00011B	PSEL 00110B	PSEL 01100B	PSEL 10010B					▲SSLA3, ▼TS14
	S3A7	GTIOC1B	-	TS14	SSIRXD0					
	S3A3	GTIOC1B	SSLA3	-	SSIRXD0					
P407		PSEL 00001B	PSEL 00100B	PSEL 00110B	PSEL 00111B	PSEL 01001B	PSEL 01010B	PSEL 01100B	PSEL 01101B	▲AGTIO0, ▲SEG11
	S3A7	-	CTS4	SSLB3	SDA0	RTCOUT	ADTRG0	TS3	-	
	S3A3	AGTIO0	CTS4	SSLB3	SDA0	RTCOUT	ADTRG0	TS3	SEG11	
		PSEL 10011B								
	S3A7	USB_VBUS								
	S3A3	USB_VBUS								

Table 3. 11 100 Pin Package Difference (11 of 13)

Port	MCU	Select								Comments
P413		PSEL 00010B	PSEL 00100B	PSEL 00110B	PSEL 01100B	PSEL 10101B				▼TS9
	S3A7	GTOUUP	CTS0	SSLA0	TS9	SD0CLK				
	S3A3	GTOUUP	CTS0	SSLA0	-	SD0CLK				
P414		PSEL 00011B	PSEL 00110B	PSEL 01100B	PSEL 10101B	ISEL				▲GTIOC0B, ▲IRQ9, ▼TS10
	S3A7	-	SSLA1	TS10	SD0WP	-				
	S3A3	GTIOC0B	SSLA1	-	SD0WP	IRQ9				
P415		PSEL 00011B	PSEL 00110B	PSEL 01100B	PSEL 10101B	ISEL				▲GTIOC0A, ▲SD0CD, ▲IRQ8, ▼TS11
	S3A7	-	SSLA2	TS11	-	-				
	S3A3	GTIOC0A	SSLA2	-	SD0CD	IRQ8				
P500		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 01101B	PSEL 10001B	PSEL 10011B	ASEL ADC	ASEL CMP	▲GTIOC2A, ▲CMPREF1
	S3A7	AGTOA0	GTIU	-	SEG48	QSPCLK	USB_VBUSEN	AN016	-	
	S3A3	AGTOA0	GTIU	GTIOC2A	SEG48	QSPCLK	USB_VBUSEN	AN016	CMPREF1	
P501		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00101B	PSEL 01101B	PSEL 10001B	PSEL 10011B	ASEL ADC	▲GTIOC2B, ▲TXD3, ▲CMPIN1
	S3A7	AGTOB0	GTIV	-	-	SEG49	QSSL	USB_OVRCURA	AN017	
	S3A3	AGTOB0	GTIV	GTIOC2B	TXD3	SEG49	QSSL	USB_OVRCURA	AN017	
		ASEL CMP	ISEL							
	S3A7	-	IRQ11							
	S3A3	CMPIN1	IRQ11							
P502		PSEL 00010B	PSEL 00011B	PSEL 00101B	PSEL 01101B	PSEL 10001B	PSEL 10011B	ASEL ADC	ASEL CMP	▲GTIOC3B, ▲RXD3, ▲CMPREF0
	S3A7	GTIW	-	-	SEG50	QIO0	USB_OVRCURB	AN018	-	
	S3A3	GTIW	GTIOC3B	RXD3	SEG50	QIO0	USB_OVRCURB	AN018	CMPREF0	
		ISEL								
	S3A7	IRQ12								
	S3A3	IRQ12								

Table 3. 12 100 Pin Package Difference (12 of 13)

Port	MCU	Select								Comments
P503		PSEL 00010B	PSEL 00100B	PSEL 00101B	PSEL 01101B	PSEL 10001B	PSEL 10011B	ASEL ADC	ASEL CMP	▲GTETRGA, ▲CTS2, ▲SCK3, ▲AN023, ▲CMPIN0, ▼AN019, ▼GTETRGC
	S3A7	GTETRGC	-	-	SEG51	QIO1	USB_EXICEN	AN019	-	
	S3A3	GTETRGA	CTS2	SCK3	SEG51	QIO1	USB_EXICEN	AN023	CMPIN0	
P504		PSEL 00010B	PSEL 00100B	PSEL 00101B	PSEL 01011B	PSEL 10001B	PSEL 10011B	ASEL ADC		▲GTETRGB, ▲SCK2, ▲CTS3, ▲AN024, ▲ALE, ▼AN020, ▼GTETRGD
	S3A7	GTETRGD	-	-	-	QIO2	USB_ID	AN020		
	S3A3	GTETRGB	SCK2	CTS3	ALE	QIO2	USB_ID	AN024		
P505		PSEL 00100B	PSEL 10001B	ASEL ADC	ISEL					▲RXD2, ▲AN025, ▼AN021
	S3A7	-	QIO3	AN021	IRQ14					
	S3A3	RXD2	QIO3	AN025	IRQ14					
P600		PSEL 00011B	PSEL 00101B	PSEL 01011B	PSEL 01101B	PSEL 10101B				▲GTIOC6B, ▲SCK9, ▲SD0DAT7
	S3A7	-	-	RD	SEG41	-				
	S3A3	GTIOC6B	SCK9	RD	SEG41	SD0DAT7				
P601		PSEL 00011B	PSEL 00101B	PSEL 01011B	PSEL 01101B	PSEL 10101B				▲GTIOC6A, ▲RXD9, ▲SD0DAT6
	S3A7	-	-	WR/WR0	SEG40	-				
	S3A3	GTIOC6A	RXD9	WR/WR0	SEG40	SD0DAT6				
P602		PSEL 00011B	PSEL 00101B	PSEL 01011B	PSEL 01101B	PSEL 10101B				▲GTIOC7B, ▲TXD9, ▲SD0DAT5
	S3A7	-	-	EBCLK	SEG39	-				
	S3A3	GTIOC7B	TXD9	EBCLK	SEG39	SD0DAT5				
P603		PSEL 00011B	PSEL 00101B	PSEL 01011B	PSEL 01101B	PSEL 10101B				▲GTIOC7A, ▲CTS9, ▲SD0DAT4
	S3A7	-	-	D13	SEG38	-				
	S3A3	GTIOC7A	CTS9	D13	SEG38	SD0DAT4				
P608		PSEL 00011B	PSEL 01011B	PSEL 01101B	PSEL 10101B					▲GTIOC4B, ▲SD0DAT1
	S3A7	-	A0/BC0	SEG28	-					
	S3A3	GTIOC4B	A0/BC0	SEG28	SD0DAT1					

Table 3. 13 100 Pin Package Difference (13 of 13)

Port	MCU	Select								Comments
P609		PSEL 00011B	PSEL 01011B	PSEL 01101B	PSEL 10101B					▲GTIOC5A, ▲SD0DAT2
	S3A7	-	CS1#	SEG29	-					
	S3A3	GTIOC5A	CS1#	SEG29	SD0DAT2					
P610		PSEL 00011B	PSEL 01011B	PSEL 01101B	PSEL 10101B					▲GTIOC5B, ▲SD0DAT3
	S3A7	-	CS0#	SEG30	-					
	S3A3	GTIOC5B	CS0#	SEG30	SD0DAT3					
P708		PSEL 00101B	PSEL 00110B	PSEL 01010B	PSEL 01100B	ISEL				▼CACREF, ▼TS12
	S3A7	RXD1	SSLA3	CACREF	TS12	IRQ11				
	S3A3	RXD1	SSLA3	-	-	IRQ11				
P808		PSEL 01101B	PSEL 10101B							▲SD0CLK
	S3A7	SEG18	-							
	S3A3	SEG18	SD0CLK							
P809		PSEL 01101B	PSEL 10101B							▲SD0CMD
	S3A7	SEG19	-							
	S3A3	SEG19	SD0CMD							

Appendix 3. 144 Pin Package

Table 4. 1 144 Pin Package Difference (1 of 17)

Port	MCU	Select								Comments
P000		PSEL 01100B	ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL				▼IVREF0/IVCMP0
	S3A7	TS21	AN000	IVREF0/IVCMP0	AMP0+	IRQ6				
	S3A3	TS21	AN000	-	AMP0+	IRQ6				
P001		PSEL 01100B	ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL				▼IVREF1/IVCMP1
	S3A7	TS22	AN001	IVREF1/IVCMP1	AMP0-	IRQ7				
	S3A3	TS22	AN001	-	AMP0-	IRQ7				
P002		ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL					▲IRQ2 ▼IVREF2/IVCMP2 ▼IRQ8
	S3A7	AN002	IVREF2/IVCMP2	AMP0O	IRQ8					
	S3A3	AN002	-	AMP0O	IRQ2					
P003		ASEL ADC	ASEL CMP	ASEL OPAMP						▼IVREF3/IVCMP3
	S3A7	AN003	IVREF3/IVCMP3	AMP1O						
	S3A3	AN003	-	AMP1O						
P004		ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL					▲IRQ3, ▼IRQ9, ▼IVCMP0
	S3A7	AN004	IVCMP0	AMP2O	IRQ9					
	S3A3	AN004	-	AMP2O	IRQ3					
P005		PSEL 01100B	ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL				▲AN011, ▼TS26, ▼AN005, ▼IVREF0
	S3A7	TS26	AN005	IVREF0	AMP3+	IRQ10				
	S3A3	-	AN011	-	AMP3+	IRQ10				
P006		PSEL 01100B	ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL				▲AN012, ▼TS27, ▼IVREF4/IVREF1, ▼AN006
	S3A7	TS27	AN006	IVREF4/IVREF1	AMP3-	IRQ11				
	S3A3	-	AN012	-	AMP3-	IRQ11				

Table 4. 2 144 Pin Package Difference (2 of 17)

Port	MCU	Select								Comments
P007		ASEL ADC	ASEL CMP	ASEL OPAMP						▲AN013, ▼AN007, ▼IVCMP4/IVCMP1
	S3A7	AN007	IVCMP4/IVCMP1	AMP3O						
	S3A3	AN013	-	AMP3O						
P008		PSEL 01100B	ASEL ADC	ISEL						▲AN014, ▼TS29, ▼AN008
	S3A7	TS29	AN008	IRQ12						
	S3A3	-	AN014	IRQ12						
P009		ASEL ADC	ISEL							▲AN015, ▼AN009
	S3A7	AN009	IRQ13							
	S3A3	AN015	IRQ13							
P010		PSEL 01100B	ASEL ADC	ASEL OPAMP	ISEL					▲AN005, ▼AN010
	S3A7	TS30	AN010	AMP2-	IRQ14					
	S3A3	TS30	AN005	AMP2-	IRQ14					
P011		PSEL 01100B	ASEL ADC	ASEL OPAMP	ISEL					▲AN006, ▼AN011
	S3A7	TS31	AN011	AMP2+	IRQ15					
	S3A3	TS31	AN006	AMP2+	IRQ15					
P012		ASEL ADC	ASEL OPAMP							▲AN007, ▼AN012
	S3A7	AN012	AMP1-							
	S3A3	AN007	AMP1-							
P013		ASEL ADC	ASEL OPAMP							▲AN013, ▼AN008
	S3A7	AN013	AMP1+							
	S3A3	AN008	AMP1+							
P014		ASEL ADC	ASEL CMP	ASEL DAC						▲AN009, ▼AN014, ▼IVREF5/IVREF2
	S3A7	AN014	IVREF5/IVREF2	DA0						
	S3A3	AN009	-	DA0						

Table 4. 3 144 Pin Package Difference (3 of 17)

Port	MCU	Select								Comments
P015		PSEL 01100B	ASEL ADC	ASEL CMP	ASEL DAC	ISEL				▲TS28, ▲AN010, ▲IRQ7, ▼AN015, ▼IVCMP5/IVCMP2, ▼DA1, ▼IRQ13
	S3A7	-	AN015	IVCMP5/IVCMP2	DA1	IRQ13				
	S3A3	TS28	AN010	-	-	IRQ7				
P100		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 00111B	PSEL 01000B	▲AN022, ▲GTIOC5B, ▼AN027
	S3A7	AGTIO0	GTETRGA	-	RXD0	SCK1	MISOA	SCL1	KR00	
	S3A3	AGTIO0	GTETRGA	GTIOC5B	RXD0	SCK1	MISOA	SCL1	KR00	
		PSEL 01011B	PSEL 01101B	ASEL ADC	ASEL CMP	ISEL				
	S3A7	D0	VL1	AN027	CMPIN0	IRQ2				
	S3A3	D0	VL1	AN022	CMPIN0	IRQ2				
P101		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 00111B	PSEL 01000B	▲AN021, ▲GTIOC5A, ▼AN026
	S3A7	AGTEE0	GTETRGB	-	TXD0	CTS1	MOSIA	SDA1	KR01	
	S3A3	AGTEE0	GTETRGB	GTIOC5A	TXD0	CTS1	MOSIA	SDA1	KR01	
		PSEL 01011B	PSEL 01101B	ASEL ADC	ASEL CMP	ISEL				
	S3A7	D1	VL2	AN026	CMPREF0	IRQ1				
	S3A3	D1	VL2	AN021	CMPREF0	IRQ1				
P102		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01000B	PSEL 01010B	▲TXD2, ▲CRX0, ▲AN020, ▼AN025
	S3A7	AGTO0	GTOWLO	GTIOC2B	SCK0	-	RSPCKA	KR02	ADTRG0	
	S3A3	AGTO0	GTOWLO	GTIOC2B	SCK0	TXD2	RSPCKA	KR02	ADTRG0	
		PSEL 01011B	PSEL 01101B	PSEL 10000B	ASEL ADC	ASEL CMP				
	S3A7	D2	VL3	-	AN025	CMPIN1				
	S3A3	D2	VL3	CRX0	AN020	CMPIN1				

Table 4. 4 144 Pin Package Difference (4 of 17)

Port	MCU	Select								Comments
P103		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00110B	PSEL 01000B	PSEL 01011B	PSEL 01101B	PSEL 10000B	▲CTX0, ▲AN019, ▼AN024
	S3A7	GTOWUP	GTIOC2A	CTS0	SSLA0	KR03	D3	VL4	-	
	S3A3	GTOWUP	GTIOC2A	CTS0	SSLA0	KR03	D3	VL4	CTX0	
		ASEL ADC	ASEL CMP							
	S3A7	AN024	CMPREF1							
	S3A3	AN019	CMPREF1							
P104		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00110B	PSEL 01000B	PSEL 01011B	PSEL 01100B	PSEL 01101B	▲GTIOC1B, ▲RXD0, ▲TS13
	S3A7	GTETRGB	-	-	SSLA1	KR04	D4	-	COM0	
	S3A3	GTETRGB	GTIOC1B	RXD0	SSLA1	KR04	D4	TS13	COM0	
		ISEL								
	S3A7	IRQ1								
	S3A3	IRQ1								
P105		PSEL 00010B	PSEL 00011B	PSEL 00110B	PSEL 01000B	PSEL 01011B	PSEL 01100B	PSEL 01101B	ISEL	▲GTIOC1A, ▲TS34
	S3A7	GTETRGA	-	SSLA2	KR05	D5	-	COM1	IRQ0	
	S3A3	GTETRGA	GTIOC1A	SSLA2	KR05	D5	TS34	COM1	IRQ0	
P108		PSEL 00000B	PSEL 00010B	PSEL 00011B	PSEL 00101B	PSEL 00110B				▲GTOULO
	S3A7	TMS/SWDIO	-	GTIOC0B	CTS9	SSLB0				
	S3A3	TMS/SWDIO	GTOULO	GTIOC0B	CTS9	SSLB0				
P109		PSEL 00000B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01001B	PSEL 01100B	▲SCK1, ▲TS10, ▲SEG52, ▲CTX0
	S3A7	TDO/TRACESWO	GTOVUP	GTIOC1A	-	TXD9	MOSIB	CLKOUT	-	
	S3A3	TDO/TRACESWO	GTOVUP	GTIOC1A	SCK1	TXD9	MOSIB	CLKOUT	TS10	
		PSEL 01101B	PSEL 10000B							
	S3A7	-	-							
	S3A3	SEG52	CTX0							

Table 4. 5 144 Pin Package Difference (5 of 17)

Port	MCU	Select								Comments
P110		PSEL 00000B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01001B	PSEL 01101B	▲SEG53, ▲CRX0
	S3A7	TDI	GTOVLO	GTIOC1B	CTS2	RXD9	MISOB	VCOUT	-	
	S3A3	TDI	GTOVLO	GTIOC1B	CTS2	RXD9	MISOB	VCOUT	SEG53	
		PSEL 10000B	ISEL							
	S3A7	-	IRQ3							
	S3A3	CRX0	IRQ3							
P111		PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01011B	PSEL 01100B	PSEL 01101B	ISEL	▲TS12
	S3A7	GTIOC3A	SCK2	SCK9	RSPCKB	A5	-	CAPH	IRQ4	
	S3A3	GTIOC3A	SCK2	SCK9	RSPCKB	A5	TS12	CAPH	IRQ4	
P112		PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01011B	PSEL 01100B	PSEL 01101B	PSEL 10010B	▲SCK1, ▲SSLB0, ▲TSCAP
	S3A7	GTIOC3B	TXD2	-	-	A4	-	CAPL	SSISCK0	
	S3A3	GTIOC3B	TXD2	SCK1	SSLB0	A4	TSCAP	CAPL	SSISCK0	
P113		PSEL 00011B	PSEL 00100B	PSEL 01011B	PSEL 01100B	PSEL 01101B	PSEL 10010B			▲GTIOC2A, ▲TS27
	S3A7	-	RXD2	A3	-	SEG0/COM4	SSIWS0			
	S3A3	GTIOC2A	RXD2	A3	TS27	SEG0/COM4	SSILRCK0/SSIFS0			
P114		PSEL 00011B	PSEL 01011B	PSEL 01100B	PSEL 01101B	PSEL 10010B				▲GTIOC2B, ▲TS29
	S3A7	-	A2	-	SEG24	SSIRXD0				
	S3A3	GTIOC2B	A2	TS29	SEG24	SSIRXD0				
P115		PSEL 00011B	PSEL 01011B	PSEL 01100B	PSEL 01101B	PSEL 10010B				▲GTIOC4A, ▲TS35
	S3A7	-	A1	-	SEG25	SSITXD0				
	S3A3	GTIOC4A	A1	TS35	SEG25	SSITXD0				

Table 4. 6 144 Pin Package Difference (6 of 17)

Port	MCU	Select								Comments
P202		PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01011B	PSEL 01101B	PSEL 10000B	PSEL 10101B	▼CRX0
	S3A7	GTIOC5B	SCK2	RXD9	MISOB	WR1/BC1	SEG21	CRX0	SD0DAT6	
	S3A3	GTIOC5B	SCK2	RXD9	MISOB	WR1/BC1	SEG21	-	SD0DAT6	
		ISEL								
	S3A7	IRQ3								
	S3A3	IRQ3								
P203		PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01011B	PSEL 01100B	PSEL 01101B	PSEL 10000B	▲A19, ▼CTX0
	S3A7	GTIOC5A	CTS2	TXD9	MOSIB	-	TSCAP	SEG22	CTX0	
	S3A3	GTIOC5A	CTS2	TXD9	MOSIB	A19	TSCAP	SEG22	-	
		PSEL 10101B	ISEL							
	S3A7	SD0DAT5	IRQ2							
	S3A3	SD0DAT5	IRQ2							
P204		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 00111B	PSEL 01010B	▲A18, ▼SSISCK1
	S3A7	AGTIO1	GTIW	GTIOC4B	SCK4	SCK9	RSPCKB	SCL0	CACREF	
	S3A3	AGTIO1	GTIW	GTIOC4B	SCK4	SCK9	RSPCKB	SCL0	CACREF	
		PSEL 01011B	PSEL 01100B	PSEL 01101B	PSEL 10010B	PSEL 10011B	PSEL 10101B			
	S3A7	-	TS0	SEG23	SSISCK1	USB_OVRCURB	SD0DAT4			
	S3A3	A18	TS0	SEG23	-	USB_OVRCURB	SD0DAT4			
P205		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 00111B	PSEL 01001B	▲SEG20, ▼SSIWS1
	S3A7	AGTO1	GTIV	GTIOC4A	TXD4	CTS9	SSLB0	SCL1	CLKOUT	
	S3A3	AGTO1	GTIV	GTIOC4A	TXD4	CTS9	SSLB0	SCL1	CLKOUT	
		PSEL 01011B	PSEL 01100B	PSEL 01101B	PSEL 10010B	PSEL 10011B	PSEL 10101B	ISEL		
	S3A7	A16	TSCAP	-	SSIWS1	USB_OVRCURA	SD0DAT3	IRQ1		
	S3A3	A16	TSCAP	SEG20	-	USB_OVRCURA	SD0DAT3	IRQ1		

Table 4. 7 144 Pin Package Difference (7 of 17)

Port	MCU	Select								Comments
P206		PSEL 00010B	PSEL 00100B	PSEL 00110B	PSEL 00111B	PSEL 01011B	PSEL 01100B	PSEL 01101B	PSEL 10010B	▲SEG12, ▼SSIDATA1
	S3A7	GTIU	RXD4	SSLB1	SDA1	WAIT	TS1	-	SSIDATA1	
	S3A3	GTIU	RXD4	SSLB1	SDA1	WAIT	TS1	SEG12	-	
		PSEL 10011B	PSEL 10101B	ISEL						
	S3A7	USB_VBUSEN	SD0DAT2	IRQ0						
	S3A3	USB_VBUSEN	SD0DAT2	IRQ0						
P212/EXTAL		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00101B	ISEL				▲GTETRGB, ▲GTIOC0B, ▼GTETRGD
	S3A7	AGTEE1	GTETRGD	-	RXD1	IRQ3				
	S3A3	AGTEE1	GTETRGB	GTIOC0B	RXD1	IRQ3				
P213/EXTAL		PSEL 00010B	PSEL 00011B	PSEL 00101B	ISEL					▲GTETRGA, ▲GTIOC0A, ▼GTETRGC
	S3A7	GTETRGC	-	TXD1	IRQ2					
	S3A3	GTETRGA	GTIOC0A	TXD1	IRQ2					
P300		PSEL 00000B	PSEL 00010B	PSEL 00011B	PSEL 00110B					▲GTOUUP
	S3A7	TCK/SWCLK	-	GTIOC0A	SSLB1					
	S3A3	TCK/SWCLK	GTOUUP	GTIOC0A	SSLB1					
P301		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01011B	PSEL 01100B	▲AGTIO0, ▲CTS9, ▲TS9
	S3A7	-	GTOULO	GTIOC4B	RXD2	-	SSLB2	A6	-	
	S3A3	AGTIO0	GTOULO	GTIOC4B	RXD2	CTS9	SSLB2	A6	TS9	
		PSEL 01101B	ISEL							
	S3A7	SEG1/COM5	IRQ6							
	S3A3	SEG1/COM5	IRQ6							
P302		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00110B	PSEL 01011B	PSEL 01100B	PSEL 01101B	ISEL	▲TS8
	S3A7	GTOUUP	GTIOC4A	TXD2	SSLB3	A7	-	SEG2/COM6	IRQ5	
	S3A3	GTOUUP	GTIOC4A	TXD2	SSLB3	A7	TS8	SEG2/COM6	IRQ5	

Table 4. 8 144 Pin Package Difference (8 of 17)

Port	MCU	Select								Comments
P303		PSEL 00011B	PSEL 01011B	PSEL 01100B	PSEL 01101B	PSEL 10101B				▲TS2, ▲SD0DAT0
	S3A7	GTIOC7B	A8	-	SEG3/COM7	-				
	S3A3	GTIOC7B	A8	TS2	SEG3/COM7	SD0DAT0				
P304		PSEL 00011B	PSEL 01011B	PSEL 01100B	PSEL 01101B	PSEL 10101B	ISEL			▲TS11, ▲SD0WP
	S3A7	GTIOC7A	A9	-	SEG17	-	IRQ9			
	S3A3	GTIOC7A	A9	TS11	SEG17	SD0WP	IRQ9			
P305		PSEL 01011B	PSEL 01101B	PSEL 10001B	PSEL 10101B	ISEL				▲QSPCLK, ▲SD0CD
	S3A7	A10	SEG16	-	-	IRQ8				
	S3A3	A10	SEG16	QSPCLK	SD0CD	IRQ8				
P306		PSEL 01011B	PSEL 01101B	PSEL 10001B						▲QSSL
	S3A7	A11	SEG15	-						
	S3A3	A11	SEG15	QSSL						
P307		PSEL 01011B	PSEL 01101B	PSEL 10001B						▲QIO0
	S3A7	A12	SEG14	-						
	S3A3	A12	SEG14	QIO0						
P308		PSEL 01011B	PSEL 01101B	PSEL 10001B						▲QIO1
	S3A7	A13	SEG13	-						
	S3A3	A13	SEG13	QIO1						
P309		PSEL 00101B	PSEL 01011B	PSEL 01101B	PSEL 10001B					▲RXD3, ▲QIO2, ▼SEG12
	S3A7	-	A14	SEG12	-					
	S3A3	RXD3	A14	-	QIO2					
P310		PSEL 00001B	PSEL 00101B	PSEL 01011B	PSEL 01101B	PSEL 10001B				▲AGTEE1, ▲TXD3, ▲QIO3, ▼SEG11
	S3A7	-	-	A15	SEG11	-				
	S3A3	AGTEE1	TXD3	A15	-	QIO3				

Table 4. 9 144 Pin Package Difference (9 of 17)

Port	MCU	Select								Comments
P311		PSEL 00001B	PSEL 00101B	PSEL 01011B	PSEL 01101B					▲AGTOB1, ▲SCK3, ▼SEG10
	S3A7	-	-	CS2#	SEG10					
	S3A3	AGTOB1	SCK3	CS2#	-					
P312		PSEL 00001B	PSEL 00101B	PSEL 01011B	PSEL 01101B					▲AGTOA1, ▲CTS3, ▼SEG9
	S3A7	-	-	CS3#	SEG9					
	S3A3	AGTOA1	CTS3	CS3#	-					
P313		PSEL 01011B	PSEL 01101B	PSEL 10101B						▲A20, ▼SEG20
	S3A7	-	SEG20	SD0DAT7						
	S3A3	A20	-	SD0DAT7						
P314		PSEL 01010B	PSEL 01011B	PSEL 01101B						▲A21, ▲ADTRG0, ▼SEG4
	S3A7	-	-	SEG4						
	S3A3	ADTRG0	A21	-						
P315		PSEL 00100B	PSEL 01011B	PSEL 01101B						▲A22, ▲RXD4, ▼SEG5
	S3A7	-	-	SEG5						
	S3A3	RXD4	A22	-						
P400		PSEL 00001B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00111B	PSEL 01010B	PSEL 01100B	PSEL 01101B	▲AGTIO1, ▲SCK1, ▲CACREF, ▲SEG4
	S3A7	-	GTIOC6A	SCK4	-	SCL0	-	TS20	-	
	S3A3	AGTIO1	GTIOC6A	SCK4	SCK1	SCL0	CACREF	TS20	SEG4	
		PSEL 10010B	ISEL							
	S3A7	AUDIO_CLK	IRQ0							
	S3A3	AUDIO_CLK	IRQ0							

Table 4. 10 144 Pin Package Difference (10 of 17)

Port	MCU	Select								Comments
P401		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00111B	PSEL 01100B	PSEL 01101B	PSEL 10000B	▲TDX1, ▲SEG5
	S3A7	GTETRGA	GTIOC6B	CTS4	-	SDA0	TS19	-	CTX0	
	S3A3	GTETRGA	GTIOC6B	CTS4	TXD1	SDA0	TS19	SEG5	CTX0	
		ISEL								
	S3A7	IRQ5								
	S3A3	IRQ5								
P402		PSEL 00001B	PSEL 00101B	PSEL 01100B	PSEL 01101B	PSEL 10000B	ISEL	PSEL Don't Care		▲RXD1, ▲SEG6, ▲AGTIO0_E/AGTIO1
	S3A7	-	-	TS18	-	CRX0	IRQ4	RTCIC0/AGTIO0/ AGTIO1		
	S3A3	AGTIO0_E/AGTIO1	RXD1	TS18	SEG6	CRX0	IRQ4	RTCIC0		
P403		PSEL 00001B	PSEL 00011B	PSEL 00101B	PSEL 01100B	PSEL 10010B	PSEL Don't Care			▲CTS1 ▲AGTIO0_F/AGTIO1
	S3A7	-	GTIOC3A	-	TS17	SSISCK0	RTCIC1/AGTIO0/ AGTIO1			
	S3A3	AGTIO0_F/AGTIO1	GTIOC3A	CTS1	TS17	SSISCK0	RTCIC1			
P404		PSEL 00011B	PSEL 01100B	PSEL 10010B	PSEL Don't Care					▼TS16
	S3A7	GTIOC3B	TS16	SSIWS0	RTCIC2					
	S3A3	GTIOC3B	-	SSIWS0	RTCIC2					
P405		PSEL 00011B	PSEL 01100B	PSEL 10010B						▼TS15
	S3A7	GTIOC1A	TS15	SSITXD0						
	S3A3	GTIOC1A	-	SSITXD0						
P406		PSEL 00011B	PSEL 00110B	PSEL 01100B	PSEL 10010B					▲SSLA3, ▼TS14
	S3A7	GTIOC1B	-	TS14	SSIRXD0					
	S3A3	GTIOC1B	SSLA3	-	SSIRXD0					

Table 4. 11 144 Pin Package Difference (11 of 17)

Port	MCU	Select								Comments
P407		PSEL 00001B	PSEL 00100B	PSEL 00110B	PSEL 00111B	PSEL 01001B	PSEL 01010B	PSEL 01100B	PSEL 01101B	▲AGTIO0, ▲SEG11
	S3A7	-	CTS4	SSLB3	SDA0	RTCOUT	ADTRG0	TS3	-	
	S3A3	AGTIO0	CTS4	SSLB3	SDA0	RTCOUT	ADTRG0	TS3	SEG11	
		PSEL 10011B								
	S3A7	USB_VBUS								
	S3A3	USB_VBUS								
P408		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00111B	PSEL 01100B	PSEL 01101B	PSEL 10011B	▲GTIOC5B, ▲CTS1, ▲SCL0, ▲SEG10
	S3A7	GTOWLO	-	-	RXD3	-	TS4	-	USB_ID	
	S3A3	GTOWLO	GTIOC5B	CTS1	RXD3	SCL0	TS4	SEG10	USB_ID	
		ISEL								
	S3A7	IRQ7								
	S3A3	IRQ7								
P409		PSEL 00010B	PSEL 00011B	PSEL 00101B	PSEL 01100B	PSEL 01101B	PSEL 10011B	ISEL		▲GTIOC5A, ▲SEG9
	S3A7	GTOWUP	-	TXD3	TS5	-	USB_EXICEN	IRQ6		
	S3A3	GTOWUP	GTIOC5A	TXD3	TS5	SEG9	USB_EXICEN	IRQ6		
P410		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01100B	PSEL 01101B	▲SEG8
	S3A7	AGTOB1	GTOVLO	GTIOC9B	RXD0	SCK3	MISOA	TS6	-	
	S3A3	AGTOB1	GTOVLO	GTIOC9B	RXD0	SCK3	MISOA	TS6	SEG8	
		PSEL 10101B	ISEL							
	S3A7	SD0DAT1	IRQ5							
	S3A3	SD0DAT1	IRQ5							

Table 4. 12 144 Pin Package Difference (12 of 17)

Port	MCU	Select								Comments
P411		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01100B	PSEL 01101B	▲SEG7
	S3A7	AGTOA1	GTOVUP	GTIOC9A	TXD0	CTS3	MOSIA	TS7	-	
	S3A3	AGTOA1	GTOVUP	GTIOC9A	TXD0	CTS3	MOSIA	TS7	SEG7	
		PSEL 10101B	ISEL							
	S3A7	SD0DAT0	IRQ4							
	S3A3	SD0DAT0	IRQ4							
P412		PSEL 00010B	PSEL 00100B	PSEL 00110B	PSEL 01100B	PSEL 10101B				▼TS8
	S3A7	GTOULO	SCK0	RSPCKA	TS8	SD0CMD				
	S3A3	GTOULO	SCK0	RSPCKA	-	SD0CMD				
P413		PSEL 00010B	PSEL 00100B	PSEL 00110B	PSEL 01100B	PSEL 10101B				▼TS9
	S3A7	GTOUUP	CTS0	SSLA0	TS9	SD0CLK				
	S3A3	GTOUUP	CTS0	SSLA0	-	SD0CLK				
P414		PSEL 00011B	PSEL 00110B	PSEL 01100B	PSEL 10101B	ISEL				▲GTIOC0B, ▲IRQ9, ▼TS10
	S3A7	-	SSLA1	TS10	SD0WP	-				
	S3A3	GTIOC0B	SSLA1	-	SD0WP	IRQ9				
P415		PSEL 00011B	PSEL 00110B	PSEL 01100B	PSEL 10101B	ISEL				▲GTIOC0A, ▲SD0CD, ▲IRQ8, ▼TS11
	S3A7	-	SSLA2	TS11	-	-				
	S3A3	GTIOC0A	SSLA2	-	SD0CD	IRQ8				
P500		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 01101B	PSEL 10001B	PSEL 10011B	ASEL ADC	ASEL CMP	▲GTIOC2A, ▲CMPREF1
	S3A7	AGTOA0	GTIU	-	SEG48	QSPCLK	USB_VBUSEN	AN016	-	
	S3A3	AGTOA0	GTIU	GTIOC2A	SEG48	QSPCLK	USB_VBUSEN	AN016	CMPREF1	

Table 4. 13 144 Pin Package Difference (13 of 17)

Port	MCU	Select								Comments
P501		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00101B	PSEL 01101B	PSEL 10001B	PSEL 10011B	ASEL ADC	▲GTIOC2B, ▲TXD3, ▲CMPIN1
	S3A7	AGTOB0	GTIV	-	-	SEG49	QSSL	USB_OVRCURA	AN017	
	S3A3	AGTOB0	GTIV	GTIOC2B	TXD3	SEG49	QSSL	USB_OVRCURA	AN017	
		ASEL CMP	ISEL							
	S3A7	-	IRQ11							
	S3A3	CMPIN1	IRQ11							
P502		PSEL 00010B	PSEL 00011B	PSEL 00101B	PSEL 01101B	PSEL 10001B	PSEL 10011B	ASEL ADC	ASEL CMP	▲GTIOC3B, ▲RXD3, ▲CMPREF0
	S3A7	GTIW	-	-	SEG50	QIO0	USB_OVRCURB	AN018	-	
	S3A3	GTIW	GTIOC3B	RXD3	SEG50	QIO0	USB_OVRCURB	AN018	CMPREF0	
		ISEL								
	S3A7	IRQ12								
	S3A3	IRQ12								
P503		PSEL 00010B	PSEL 00100B	PSEL 00101B	PSEL 01101B	PSEL 10001B	PSEL 10011B	ASEL ADC	ASEL CMP	▲GTETRGA, ▲CTS2, ▲SCK3, ▲AN023, ▲CMPIN0, ▼AN019, ▼GTETRGC
	S3A7	GTETRGC	-	-	SEG51	QIO1	USB_EXICEN	AN019	-	
	S3A3	GTETRGA	CTS2	SCK3	SEG51	QIO1	USB_EXICEN	AN023	CMPIN0	
P504		PSEL 00010B	PSEL 00100B	PSEL 00101B	PSEL 01011B	PSEL 10001B	PSEL 10011B	ASEL ADC		▲GTETRGB, ▲SCK2, ▲CTS3, ▲AN024, ▲ALE, ▼AN020, ▼GTETRGD
	S3A7	GTETRGD	-	-	-	QIO2	USB_ID	AN020		
	S3A3	GTETRGB	SCK2	CTS3	ALE	QIO2	USB_ID	AN024		
P505		PSEL 00100B	PSEL 10001B	ASEL ADC	ISEL					▲RXD2, ▲AN025, ▼AN021
	S3A7	-	QIO3	AN021	IRQ14					
	S3A3	RXD2	QIO3	AN025	IRQ14					
P506		PSEL 00100B	ASEL ADC	ISEL						▲TXD2, ▲AN026, ▼AN022
	S3A7	-	AN022	IRQ15						
	S3A3	TXD2	AN026	IRQ15						

Table 4. 14 144 Pin Package Difference (14 of 17)

Port	MCU	Select								Comments
P507		ASEL ADC								▲AN027, ▼AN023
	S3A7	AN023								
	S3A3	AN027								
P511		PSEL 00011B	PSEL 00100B	PSEL 00111B	PSEL 10000B	ISEL				▲CRX0
	S3A7	GTIOC0B	RXD4	SDA2	-	IRQ15				
	S3A3	GTIOC0B	RXD4	SDA2	CRX0	IRQ15				
P512		PSEL 00011B	PSEL 00100B	PSEL 00111B	PSEL 10000B	ISEL				▲CTX0
	S3A7	GTIOC0A	TXD4	SCL2	-	IRQ14				
	S3A3	GTIOC0A	TXD4	SCL2	CTX0	IRQ14				
P600		PSEL 00011B	PSEL 00101B	PSEL 01011B	PSEL 01101B	PSEL 10101B				▲GTIOC6B, ▲SCK9, ▲SD0DAT7
	S3A7	-	-	RD	SEG41	-				
	S3A3	GTIOC6B	SCK9	RD	SEG41	SD0DAT7				
P601		PSEL 00011B	PSEL 00101B	PSEL 01011B	PSEL 01101B	PSEL 10101B				▲GTIOC6A, ▲RXD9, ▲SD0DAT6
	S3A7	-	-	WR/WR0	SEG40	-				
	S3A3	GTIOC6A	RXD9	WR/WR0	SEG40	SD0DAT6				
P602		PSEL 00011B	PSEL 00101B	PSEL 01011B	PSEL 01101B	PSEL 10101B				▲GTIOC7B, ▲TXD9, ▲SD0DAT5
	S3A7	-	-	EBCLK	SEG39	-				
	S3A3	GTIOC7B	TXD9	EBCLK	SEG39	SD0DAT5				
P603		PSEL 00011B	PSEL 00101B	PSEL 01011B	PSEL 01101B	PSEL 10101B				▲GTIOC7A, ▲CTS9, ▲SD0DAT4
	S3A7	-	-	D13	SEG38	-				
	S3A3	GTIOC7A	CTS9	D13	SEG38	SD0DAT4				
P604		PSEL 00011B	PSEL 01011B	PSEL 01101B						▲GTIOC8B
	S3A7	-	D12	SEG37						
	S3A3	GTIOC8B	D12	SEG37						

Table 4. 15 144 Pin Package Difference (15 of 17)

Port	MCU	Select								Comments
P605		PSEL 00011B	PSEL 01011B	PSEL 01101B						▲GTIOC8A
	S3A7	-	D11	SEG36						
	S3A3	GTIOC8A	D11	SEG36						
P606		PSEL 01001B	PSEL 01101B							▲RTCOUT_B
	S3A7	-	SEG35							
	S3A3	RTCOUT_B	SEG35							
P608		PSEL 00011B	PSEL 01011B	PSEL 01101B	PSEL 10101B					▲GTIOC4B, ▲SD0DAT1
	S3A7	-	A0/BC0	SEG28	-					
	S3A3	GTIOC4B	A0/BC0	SEG28	SD0DAT1					
P609		PSEL 00011B	PSEL 01011B	PSEL 01101B	PSEL 10101B					▲GTIOC5A, ▲SD0DAT2
	S3A7	-	CS1#	SEG29	-					
	S3A3	GTIOC5A	CS1#	SEG29	SD0DAT2					
P610		PSEL 00011B	PSEL 01011B	PSEL 01101B	PSEL 10101B					▲GTIOC5B, ▲SD0DAT3
	S3A7	-	CS0#	SEG30	-					
	S3A3	GTIOC5B	CS0#	SEG30	SD0DAT3					
P700		PSEL 00011B	PSEL 00110B	PSEL 01100B						▲MISOA, ▼TS32
	S3A7	GTIOC5A	-	TS32						
	S3A3	GTIOC5A	MISOA	-						
P701		PSEL 00011B	PSEL 00110B	PSEL 01100B						▲MISOA, ▼TS33
	S3A7	GTIOC5B	-	TS33						
	S3A3	GTIOC5B	MISOA	-						
P702		PSEL 00011B	PSEL 00110B	PSEL 01100B						▲RSPCKA, ▼TS34
	S3A7	GTIOC6A	-	TS34						
	S3A3	GTIOC6A	RSPCKA	-						

Table 4. 16 144 Pin Package Difference (16 of 17)

Port	MCU	Select								Comments
P703		PSEL 00011B	PSEL 00110B	PSEL 01001B						▲SSLA0, ▲VCOUT
	S3A7	GTIOC6B	-	-						
	S3A3	GTIOC6B	SSLA0	VCOUT						
P704		PSEL 00001B	PSEL 00110B							▲AGTO0, ▲SSLA1
	S3A7	-	-							
	S3A3	AGTO0	SSLA1							
P705		PSEL 00001B	PSEL 00110B							▲AGTIO0, ▲SSLA2
	S3A7	-	-							
	S3A3	AGTIO0	SSLA2							
P708		PSEL 00101B	PSEL 00110B	PSEL 01010B	PSEL 01100B	ISEL				▼CACREF, ▼TS12
	S3A7	RXD1	SSLA3	CACREF	TS12	IRQ11				
	S3A3	RXD1	SSLA3	-	-	IRQ11				
P709		PSEL 00101B	PSEL 01100B	ISEL						▼TS13
	S3A7	TXD1	TS13	IRQ10						
	S3A3	TXD1	-	IRQ10						
P710		PSEL 00101B	PSEL 01011B	PSEL 01100B						▲A17, ▼TS35
	S3A7	SCK1	-	TS35						
	S3A3	SCK1	A17	-						
P711		PSEL 00001B	PSEL 00101B							▲AGTEE0
	S3A7	-	CTS1							
	S3A3	AGTEE0	CTS1							
P712		PSEL 00001B	PSEL 00011B							▲AGTOB0
	S3A7	-	GTIOC2B							
	S3A3	AGTOB0	GTIOC2B							

Table 4. 17 144 Pin Package Difference (17 of 17)

Port	MCU	Select								Comments
P713		PSEL 00001B	PSEL 00011B							▲AGTOA0
	S3A7	-	GTIOC2A							
	S3A3	AGTOA0	GTIOC2A							
P804		PSEL 00011B	PSEL 01101B							▲GTIOC9B
	S3A7	-	SEG43							
	S3A3	GTIOC9B	SEG43							
P805		PSEL 00011B	PSEL 01101B							▲GTIOC9A
	S3A7	-	SEG42							
	S3A3	GTIOC9A	SEG42							
P808		PSEL 01101B	PSEL 10101B							▲SD0CLK
	S3A7	SEG18	-							
	S3A3	SEG18	SD0CLK							
P809		PSEL 01101B	PSEL 10101B							▲SD0CMD
	S3A7	SEG19	-							
	S3A3	SEG19	SD0CMD							
P900		PSEL 00100B	PSEL 01011B	PSEL 01101B						▲A23, ▲TXD4, ▼SEG6
	S3A7	-	-	SEG6						
	S3A3	TXD4	A23	-						
P901		PSEL 00001B	PSEL 00100B	PSEL 01101B						▲AGTIO1, ▲SCK4, ▼SEG7
	S3A7	-	-	SEG7						
	S3A3	AGTIO1	SCK4	-						
P902		PSEL 00001B	PSEL 00100B	PSEL 01101B						▲AGTO1, ▲CTS4, ▼SEG8
	S3A7	-	-	SEG8						
	S3A3	AGTO1	CTS4	-						

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Aug 28, 2017	-	Initial Release

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