Renesas Synergy™ Platform

S7G2 MCUs High-Speed USB 2.0 Board Design Guidelines

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Introduction

This document describes the guidelines for High-Speed USB 2.0 board design.

Verification Kits

The application explained in this document can be verified on the following kits:

- PE-HMI1
- DK_S7G2

This list is not all-inclusive and this document should be reviewed during any High-Speed USB 2.0 board design using the Renesas Synergy™ S7G2 microcontroller.

Note: The contents in this document are provided as a reference example based on the USB specification; the signal system quality is not guaranteed. When implementing this example into an existing system, the overall system should be thoroughly evaluated, and the user should integrate at their own discretion.

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1. Introduction

This document is described by using the pin names of S7G2. Table 1 lists the outline of the BGA 224 and BGA 176 module pins while Table 2 lists the outline of the LQFP 176 USB 2.0 module pins.

Table 1 S7G2 BGA 224 (BGA 176) USB 2.0 High-Speed Pins

Pin number	Pin Name	I/O	Name	Function
F14 (F14)*	USBHS_DP	I/O	USB D+ data	Connect to D+ pin of USB bus.
F15 (F15)*	USBHS_DM	I/O	USB D- data	Connect to D- pin of USB bus.
K13 (K13)*	USBHS_VBUS	I	VBUS input	USB cable connection monitor input pin.
G13 (G13)*	USBHS_RREF	I	Reference input	USBHS reference current source pin. This pin should be connected to the AVSS_USBHS pin through a resistor of 2.2 kΩ (±1%).
H13 (H13)*	AVCC_USBHS	I	Transceiver analog pin power supply	3.3V analog power supply for pins.
G14 (G14)*	AVSS_USBHS	I	Transceiver analog pin ground	Analog ground pin for the USBHS. Must be shorted to the PVSS_USBHS pin.
F13 (F13)*	VCC_USBHS	I	Transceiver digital pin power supply	3.3V digital power supply for pins.
F12 (F12)* F13 (F13)*	VSS1_USBHS VSS2_USBHS	I	Transceiver digital pin ground	3.3V digital ground for pins.
G15 (G15)*	PVSS_USBHS	I	Power supply for I/O circuit	PLL circuit ground pin for the USBHS. Must be shorted to the AVSS_USBHS pin.
C14 (B15)*	USBHS_EXCEN	O	Low-power control signal for OTG	This pin should be connected to the OTG power supply IC.
B15 (D13)*	USBHS_ID	I	MicroAB ID signal	This pin should be connected to the OTG power supply IC.
L15 (L15)* L14 (L14)*	USBHS_OVRCURA USBHS_OVRCURB	I	Overcurrent detection	Overcurrent pin for USB.
H9(J12)*	USBHS_VBUSEN-A USBHS_VBUSEN-B	O	VBUS Enable	VBUS power enable pin for USB.

*Note: The ( ) in the pin number denotes the pin number for the 176 pin package.

Table 2 S7G2 LQFP 176 USB 2.0 High-Speed Pins

Pin number	Pin Name	I/O	Name	Function
32	USBHS_DP	I/O	USB D+ data	USB bus D+ data pin.
31	USBHS_DM	I/O	USB D- data	USB bus D- data pin.
17	USBHS_VBUS	I	VBUS input	USB cable connection monitor input pin.
27	USBHS_RREF	I	Reference input	USBHS reference current source pin. This pin should be connected to the AVSS_USBHS pin through a resistor of 2.2 kΩ (±1%).
26	AVCC_USBHS	I	Transceiver analog pin power supply	3.3V analog power supply for pins.
28	AVSS_USBHS	I	Transceiver analog pin ground	Analog ground pin for the USBHS. Must be shorted to the PVSS_USBHS pin.
34	VCC_USBHS	I	Transceiver digital pin power supply	3.3V digital power supply for pins.
33 30	VSS1_USBHS VSS2_USBHS	I	Transceiver digital pin ground	3.3V digital ground for pins.
29	PVSS_USBHS	I	Power supply for I/O circuit	PLL circuit ground pin for the USBHS. Must be shorted to the AVSS_USBHS pin.
42	USBHS_EXCEN	O	Low-power control signal for OTG	This pin should be connected to the OTG power supply IC.
43	USBHS_ID	I	MicroAB ID signal	This pin should be connected to the OTG power supply IC.
15 14	USBHS_OVRCURA USBHS_OVRCURB	I	Overcurrent detection	Overcurrent pin for USB.
16	USBHS_VBUSEN-A USBHS_VBUSEN-B	O	VBUS Enable	VBUS power enable pin for USB.

2. USB Transmission Line

The USB transmission line refers to the printed circuit board wiring pattern that connects the USB connector to the S7G2 microcontroller (MCU). USB 2.0 has three communication modes: High-Speed, Full-Speed and Low-Speed. High-Speed mode can transmit and receive at up to 480 Mbps. Therefore, for USB High-Speed, the board traces between the S7G2 MCU and the USB connector must be designed as a high-frequency circuit transmission line. Impedance control is required for the USB transmission lines. Notes on designing the wiring pattern of the USB transmission lines are described below:

- The differential characteristic impedance required for the USB transmission lines is the differential impedance 90 Ω+/-15%.
- The common-mode characteristic impedance should be 21 Ω to 39 Ω (the impedance from any one USB signal trace to ground should be 42 Ω to 78 Ω).
- The circuit board USB transmission lines on Host and Device sides of the USB connection must not add more than 4 ns to the total delay between the Host Controller and the Device Controller. Table 3 shows how this breaks down to the acceptable USB transmission line delays on the Host and the Device side.

Table 3 Recommended Value for the Wiring Pattern Length of USB Transmission Line

	Maximum Delay Time (USB Specification)	Wiring Length	D+ and D- Wiring Length Differential
Host Controller	3 ns	300 mm or less	2.5 mm or less
Peripheral Controller	1 ns	100 mm or less	2.5 mm or less

- The pattern width and pattern pitch for impedance control vary depending on board thickness, material, and layer configuration. Contact the board manufacturer for more details.
- The wiring pattern length of the USB transmission lines from the S7G2 to the USB connector must be designed not to exceed the maximum delay time which is regulated by the USB specification. Table 2 lists the recommended values for the wiring pattern length of USB transmission lines for Host and Device.
- The lower layer of the USB transmission lines must be a ground plane. The ground plane must be at least 2 mm wider than the USB transmission lines. The power supply ground should be the same as the ground plane GND.
- Do not allocate other signal lines near the USB transmission lines. Particularly lines of heavily fluctuating signals, such as clock and data bus lines, must be allocated far from the USB transmission lines. Moreover, the USB transmission lines and other lines must not cross.
- The same layer (surface layer) as the USB transmission lines should be allocated 1 mm from the USB transmission lines, and grounded with a guard ring.
- USB transmission lines should be allocated on the same layer without passing through a hole. In addition, wiring should not be stretch or diverge widely.
- The USB transmission lines should be wired with uniform spaces.
- The USB transmission lines should be allocated far from the oscillator, power supply circuit, and other I/O connectors.
- The USB transmission lines should be wired with straight lines. If they are bent, they should be bent gently in an arc or up to 135 degrees, and not bent at acute angles (right angles).
- It is recommended that the clock, reset, read, write and chip select signals should be grounded with a guard ring.

Figure 1 shows a design example of a Host controller USB transmission line pattern. Figure 2 shows a design example of a Device controller USB transmission line pattern.

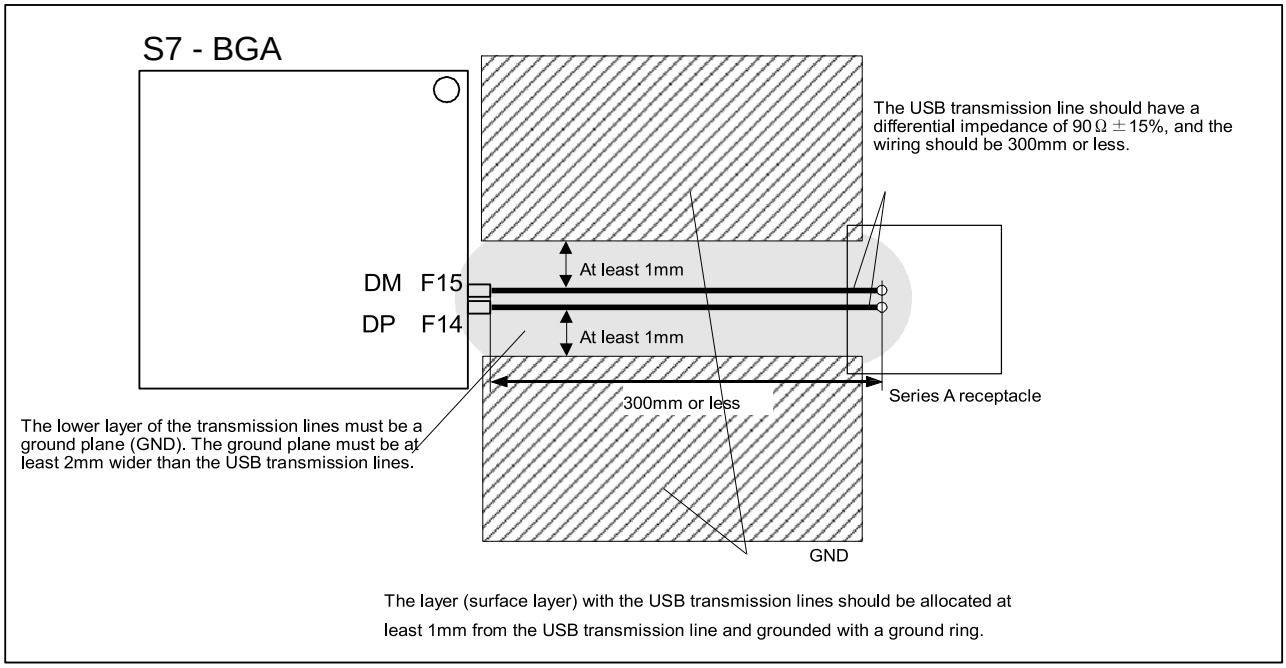


Figure 1 Design Example of a Host Controller USB Transmission Line Pattern

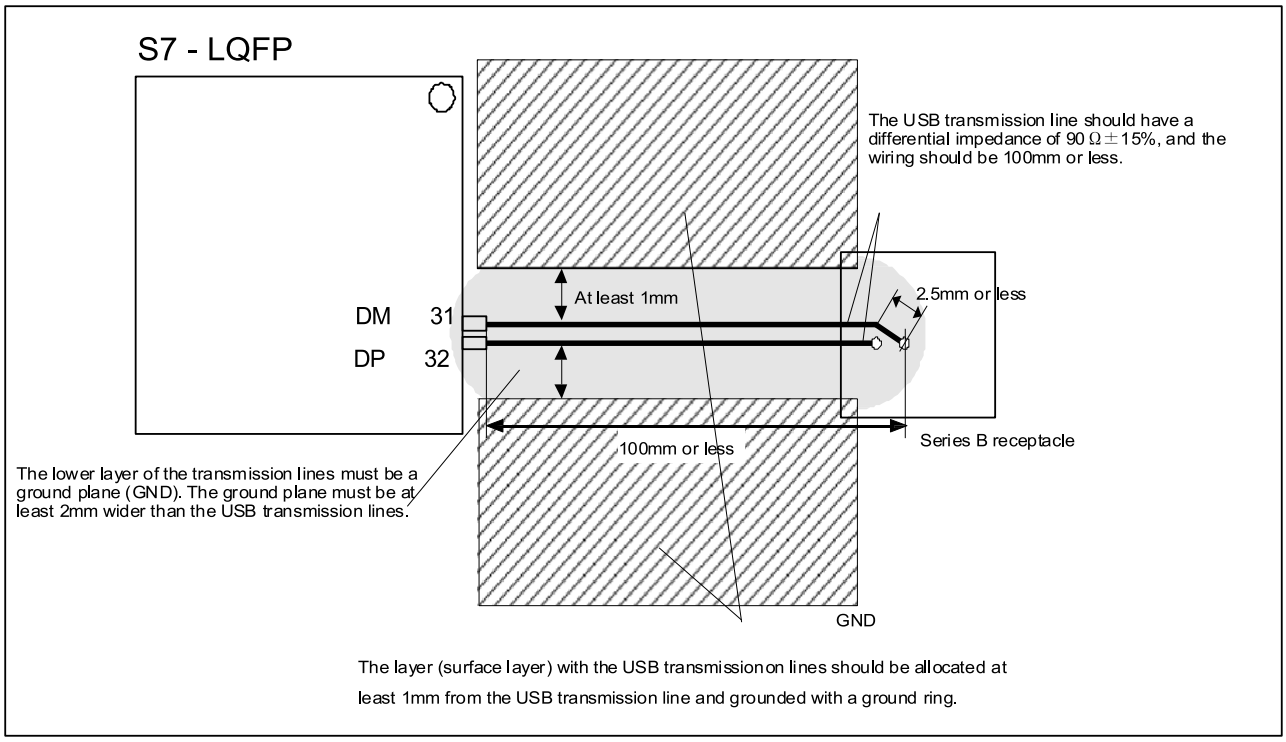


Figure 2 Design Example of a Device Controller USB Transmission Line Pattern

2.1 Routing Guidelines (from USB.org)

The High-Speed USB validation efforts focused on a four-layer motherboard where the first layer is a signal layer, the second layer is power, the third layer is ground and the fourth is a signal layer. This results in placing most of the routing on the fourth layer closest to the ground layer, and allowing a higher component density on the first layer.

- Place the high-speed USB host controller and major components on the unrouted board first.
- With minimum trace lengths, route high-speed clock and high-speed USB differential pairs first. Maintain maximum possible distance between high-speed clocks/periodic signals to high speed USB differential pairs and any connector leaving the PCB (such as, I/O connectors, control and signal headers, or power connectors).
- Route high-speed USB signals on bottom whenever possible.
- Route high-speed USB signals using a minimum of vias and corners. This reduces signal reflections and impedance changes.
- When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.
- Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
- Stubs on high speed USB signals should be avoided, as stubs will cause signal reflections and affect signal quality. If a stub is unavoidable in the design, no stub should be greater than 200 mils.
- Route all traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces as much as practical. It is preferable to change layers to avoid crossing a plane split. Refer to Section 3.6 Plane Splits, Voids and Cut-Outs (Anti-Etch) for more details on plane splits.
- Separate signal traces into similar categories and route similar signal traces together (such as routing differential pairs together).
- Keep high-speed USB signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out.
- Follow the 20*h rule of thumb by keeping traces at least 20*(height above the plane) away from the edge of the plane (VCC or GND, depending on the plane the trace is over). For the suggested stack-up the height above the plane is 4.5 mils. This calculates to a 90-mil spacing requirement from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.

Use the following separation guidelines. Figure 3 provides an illustration of the recommended trace spacing.

- Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90 ohms differential impedance. Deviations will normally occur due to package breakout and routing to connector pins. Just ensure the amount and length of the deviations are kept to the minimum possible.
- Use an impedance calculator to determine the trace width and spacing required for the specific board stack-up being used. 7.5- mil traces with 7.5-mil spacing results in approximately 90 ohms differential trace impedance.
- Minimize the length of high-speed clock and periodic signal traces that run parallel to high speed USB signal lines, to minimize crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50 mils.
- Based on simulation data, use 20-mil minimum spacing between high-speed USB signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.

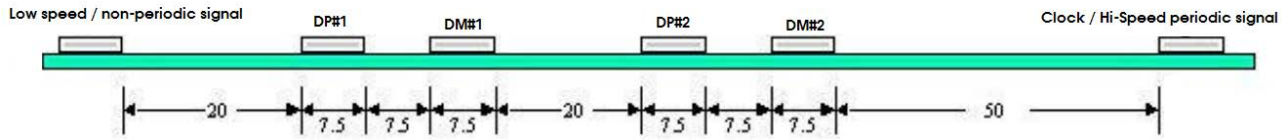


Figure 3 Recommended Trace Spacing

3. Power Supply and Ground Pattern

Notes on designing a power supply/ground pattern are described below:

- Power supplies and ground patterns should be separated into digital and analog. Table 3 and Table 4 list the power supply and ground classifications.

Table 4 USB Power Supply Classifications

S7G2 Pin Name	Power Supply Classifications			
	Analog Power Supply (3.3 V)	Digital Power Supply (3.3 V)	Digital Power Supply (1.8 V)	Digital Core Power Supply
AVCC_USBHS	0			
VCC_USBHS		0		

0: Indicates power used.

Table 5 USB Ground Classifications

S7G2 Pin Name/ USB Connector	Ground Classifications	
	Analog Ground (AGND)	Digital Ground (GND)
AVSS1_USBHS	0	
VSS1_USBHS		0
PVSS_USBHS		0
USB Connector Ground (Including Frame		0

0: Indicates the power used.

- The patterns of power supplies and grounds should be designed with as wide a surface layer as possible.
- Tantalum capacitors or ceramic capacitors having excellent high-frequency characteristics are recommended as power supply capacitors.
- Aluminum electrolytic capacitors affect the jitter value when measuring the EYE pattern. The capacitors should be thoroughly designed and tested before use.
- It is recommended to place the capacitors for the S7G2 USB Power pins as close to possible to the S7G2, with the smallest capacity closest. Figure 4 shows an example of decoupling capacitor placement.
- Please connect digital ground and analog ground by one point near S7G2 MCU.

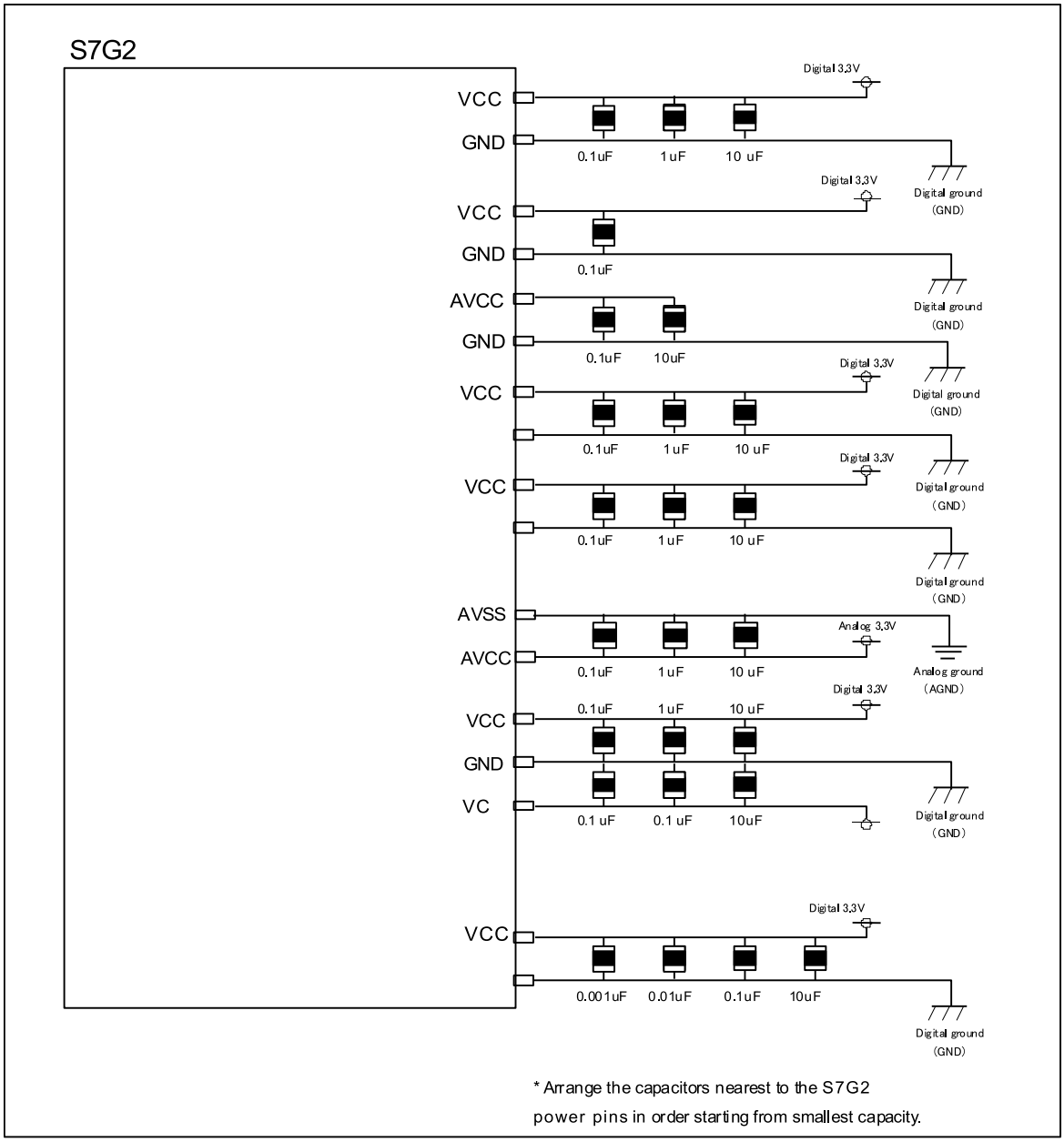


Figure 4 Example of Decoupling Capacitor Allocation

4. VBUS Power Supply Circuit

Notes on designing the VBUS power supply circuit are described below:

- When the S7G2 is used as a Host controller, the additional capacitance of the VBUS line should be designed to be 120 uF or more.
- When the S7G2 is used as a Device controller, the additional capacity of the VBUS line should be designed to be within 1.0 uF to 10 uF.
- The VBUS line should include a filter circuit as an overshoot may be caused by inconsistent impedance when the USB cable is connected. The 1.0-uF to 10-uF capacitor and 100-Ω to 1-kΩ resistor should be added as a filter circuit. The constant should be defined after confirming that an overshoot has not occurred on the board. Also, a resistor of more than 1 kΩ should not be added.
- When the S7G2 is used as a Host controller, the VBUS power should be supplied to the Device devices. A power supply switch IC with over-current protection for the USB power bus (hereinafter called “USB power supply switch IC”) is recommended for the VBUS power supply control. Make sure to consider the maximum current of the VBUS power supply line. This current is based on the current amount used by the system and the USB Device

devices connected. In addition, refer to the USB power supply switch IC datasheet used for VBUS power supply control circuit.

5. RREF Pin

Notes on designing the circuit around the REFRIN pin are described below:

- A resistor of 2.2 kΩ+/-1% (hereinafter called “standard resistor”) should be allocated between the RREF pin and AGND.
- A standard resistor should be allocated as close as possible to the S7G2.
- The RREF pin, the standard resistor, and AGND should be connected with a bold, minimal pattern.
- The standard resistor and AGND should be connected in an exclusive pattern, and then connected to the analog ground. The pattern should be designed to avoid common impedance with other signals.
- To prevent cross talk, heavily fluctuating signals such as D+, D-, clocks, address data, and control signals should neither cross nor go side by side with standard resistor and patterns. It is recommended that standard resistor and patterns be grounded with a guard ring.

Figure 5 shows the block diagram of the pin connection and the design example of pattern around the REFRIN pin.

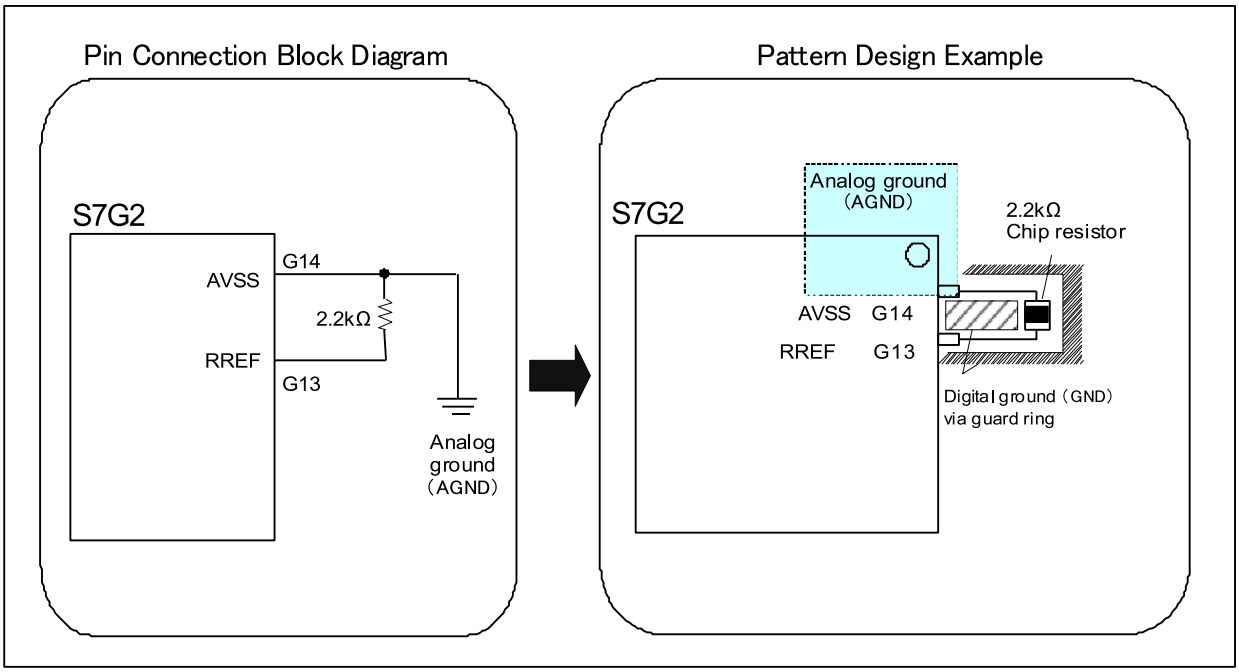


Figure 5 Pin Connection and Design Example of Pattern around the RREF Pin on BGA 224 Pin Module

6. EMI/ESD Workarounds

Notes on EMI/ESD workarounds are described below:

- When components for EMI/ESD workarounds such as coils and diodes are mounted on the USB transmission lines, they should be allocated near the USB transmission lines and the wiring should be as short as possible.
- The components for the EMI/ESD workarounds must be USB 2.0 compliant. Also, by mounting EMI/ESD workaround components, inconsistent impedance may occur on the USB transmission lines, and the waveform may become distorted. Components for use should be selected after thorough evaluation.

Figure 6 shows the block diagram of a connection example when the components for EMI/ESD workarounds are used.

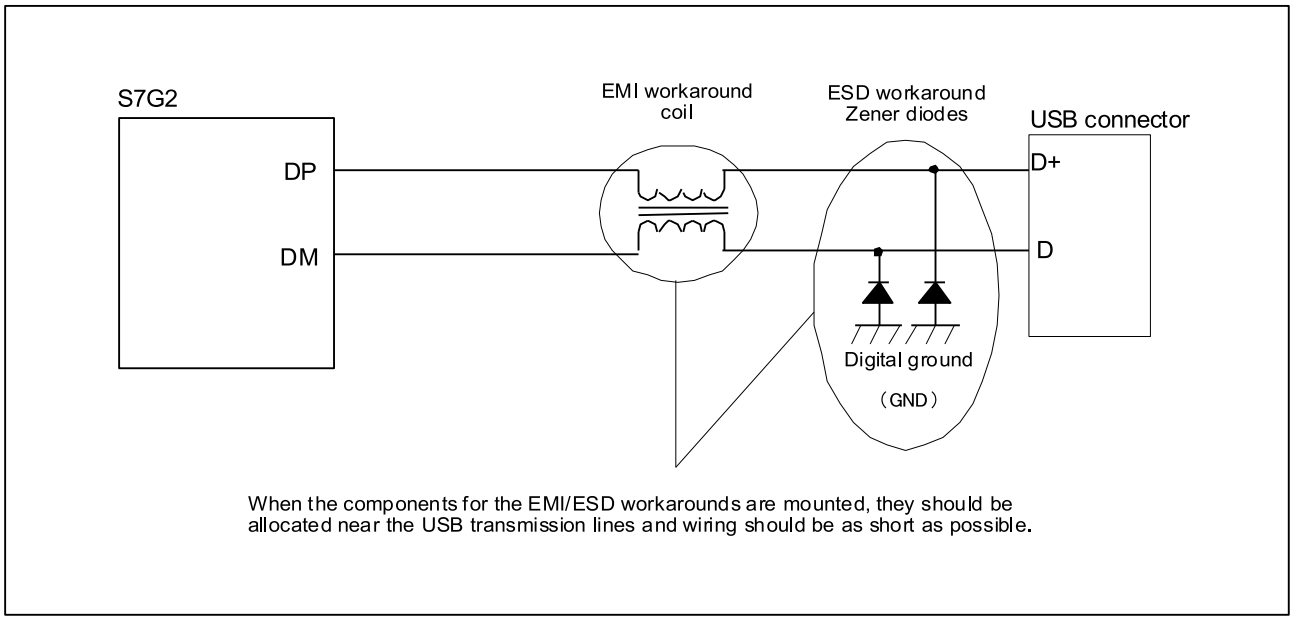
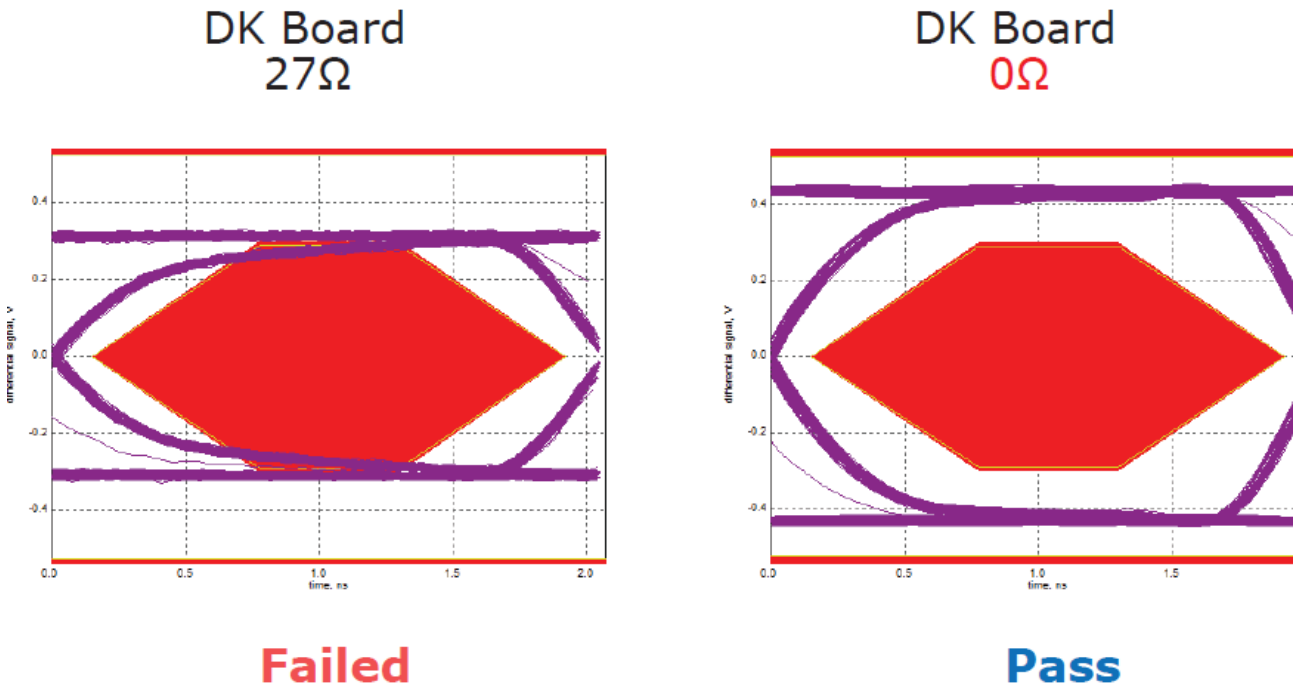


Figure 6 Connection Example When Components for EMI/ESD Workarounds are used

6.1 Signal Quality

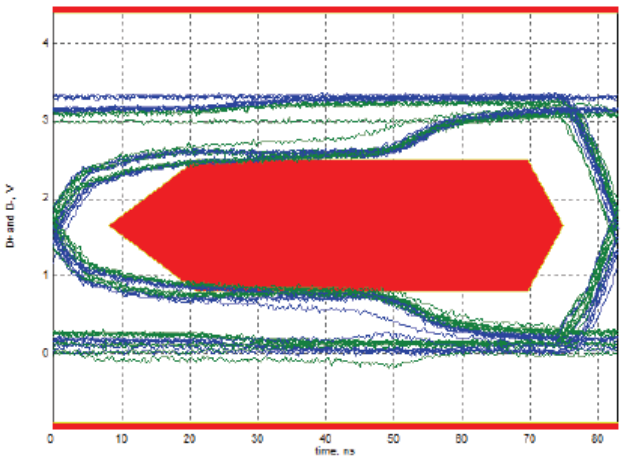
Below is shown an example of good USB High-Speed signal quality using a 0-Ω resistor on the DK-S7G2 development boards (resistors R9 & R10). The eye patterns below are representative of what a high quality signal will look like on the DK boards.

[High-Speed Port – High-Speed Host Operation]



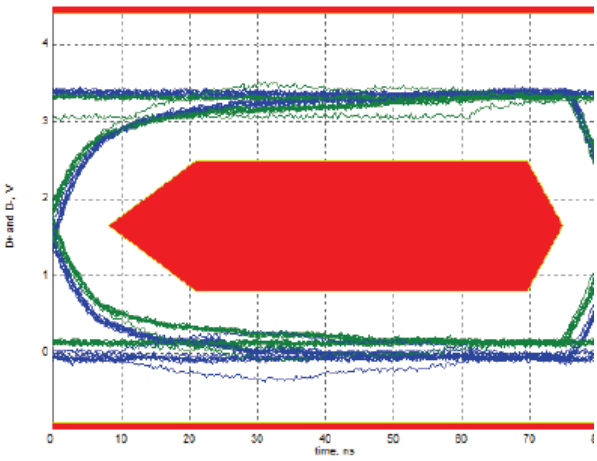
[High-Speed Port – Full-Speed Host Operation]

DK Board
27Ω



Failed

DK Board
0Ω



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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Oct 7, 2015	-	Initial version
1.01	Nov 18, 2016	-	Minor format changes

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