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Introduction
This application note shows the TFT-LCD interfacing example using the SH7764 Microcontrollers (MCUs) on-chip LCD Controller (LCDC).

Target Device
SH7764 (R0K507764E001BR from Renesas Technology Corp.)

Contents
1. Preface .......................................................................................................................... 2
2. Description of the Sample Application ........................................................................ 3
3. Sample Program "lcdc.c" ............................................................................................ 17
4. Documents for Reference ............................................................................................ 24
1. Preface

1.1 Specifications
The SH7764 MCU on-chip LCD controller (LCDC) is connected with a TFT-LCD panel to display the graphic image.

1.2 Module Used
- LCD controller (LCDC)
- General-purpose I/O ports (GPIO)

1.3 Applicable Conditions
- MCU: SH7764
- Operating frequency
  - CPU clock: 324 MHz
  - SuperHyway clock: 108 MHz
  - Peripheral clock: 54 MHz
  - Bus clock: 108 MHz
- Integrated development environment from Renesas Technology Corp.
- C compiler: SuperH RISC Engine Family C/C++ Compiler Package Ver.9.03 Release00 from Renesas Technology Corp.
- Compiler options
  - Default settings of the High-performance Embedded Workshop
  - -cpu=sh4a -endian=little -include="$(WORKSPDIR)\inc"
  - -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -optimize=0
  - -gbr=auto -chgincpath -errorpath
  - -global_volatile=0 -opt_range=all -infinite_loop=0
  - -del_vacant_loop=0 -struct_alloc=1 -nologo

1.4 Related Application Note
Refer to the related application notes as follows:
- SH7764 Group Application Note: SH7764 Example of Initialization (REJ06B0919)
2. Description of the Sample Application

This application note shows the pin connection example and configuration example to display the graphic image by the LCDC. The specifications of the TFT-LCD panel used in this application note are shown in 2.2.

2.1 LCDC Operation

2.1.1 Overview

A unified memory architecture is adopted for the LCD controller (LCDC) so that the image data for display is stored in system memory. The LCDC module reads data from system memory, uses the palette memory to determine the colors, then puts the display on the LCD panel. It is possible to connect the LCDC to the LCD module* other than microcomputer bus interface types and NTSC/PAL types and those that apply the LVDS interface.

Note: * LCD module can be connected to the LVDS interface by using the LSI with LVDS conversion LSI.

2.1.2 Features

Table 1 lists the LCDC features. Figure 1 shows a block diagram of LCDC.

Table 1 LCDC Features

<table>
<thead>
<tr>
<th>Item</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Panel interface</td>
<td>Serial interface method</td>
</tr>
<tr>
<td>Type of LCD</td>
<td>STN/dual-STN/TFT panels</td>
</tr>
<tr>
<td>Panel data formats</td>
<td>8/12/16/18-bit bus width</td>
</tr>
<tr>
<td>Color modes</td>
<td>4/8/15/16-bpp</td>
</tr>
<tr>
<td>Grayscale modes</td>
<td>1/2/4/6-bpp</td>
</tr>
<tr>
<td>Panel sizes</td>
<td>16 × 1 to 1024 × 1024 dots</td>
</tr>
<tr>
<td>Color palette</td>
<td>24-bit</td>
</tr>
<tr>
<td>Display in neutral colors for STN/DSTN panels</td>
<td>24-bit space-modulation FRC with 8-bit RGB values for reduced flicker</td>
</tr>
<tr>
<td>VRAM</td>
<td>A certain area of the synchronous DRAM (CS1 or CS2) is used as VRAM.</td>
</tr>
<tr>
<td>Line buffer</td>
<td>2.4-kbyte</td>
</tr>
<tr>
<td>Signal polarity</td>
<td>Programmable</td>
</tr>
<tr>
<td>Data formats</td>
<td>The endian of bytes is set. A packed pixel method is available.</td>
</tr>
<tr>
<td>Interrupt</td>
<td>An interrupt can be generated at a user-specified position.</td>
</tr>
</tbody>
</table>
2.1.3 I/O Pins

Table 2 lists the LCDC I/O pins.

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>I/O</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCD_D15 to 0</td>
<td>Output</td>
<td>Data for LCD panel</td>
</tr>
<tr>
<td>LCD_DON</td>
<td>Output</td>
<td>Display-on signal (DON)</td>
</tr>
<tr>
<td>LCD_CL1</td>
<td>Output</td>
<td>Shift-clock 1 (STN/DSTN)/horizontal sync signal (HSYNC)</td>
</tr>
<tr>
<td>LCD_CL2</td>
<td>Output</td>
<td>Shift-clock 2 (STN/DSTN)/dot clock (DOTCLK)</td>
</tr>
<tr>
<td>LCD_M_DISP</td>
<td>Output</td>
<td>LCD current-alternating signal/DISP signal</td>
</tr>
<tr>
<td>LCD_FLM</td>
<td>Output</td>
<td>First line marker/vertical sync signal (VSYNC) (TFT)</td>
</tr>
<tr>
<td>LCD_VCPWC</td>
<td>Output</td>
<td>LCD-module power control (VCC)</td>
</tr>
<tr>
<td>LCD_VEPWC</td>
<td>Output</td>
<td>LCD-module power control (VEE)</td>
</tr>
<tr>
<td>LCD_CLK</td>
<td>Input</td>
<td>LCD clock-source input</td>
</tr>
</tbody>
</table>
2.1.4 LCD Module Sizes which can be Displayed

This LCDC is capable of controlling displays with up to $1024 \times 1024$ dots and 16 bpp (bits per pixel). The image data for display is stored in VRAM, which is shared with the CPU. This LCDC should read the data from VRAM before display.

This LSI has a maximum 16-burst (32-bit bus width) memory read operation and a 2.4-Kbyte line buffer, so although a complete breakdown of the display is unlikely, there may be some problems with the display depending on the combination. A recommended size at the frame rate of 60 Hz is $320 \times 240$ dots in 16 bpp or $640 \times 480$ dots in 8 bpp.

As a rough standard, the bus occupation ratio shown below should not exceed 40%. The overhead coefficient becomes 2.00 when the CL2 SDRAM is connected to a 32-bit data bus and 1.825 when connected to a 64-bit data bus. The each value is ideal value under the best condition.

$$
\text{Overhead coefficient} \times \frac{\text{Total number of display pixels} \times (\text{HDCN} + 1) \times 8 \times (\text{VDLN} + 1)}{\text{CLKOUT} \times \text{Bus width} = 32 \text{ bits}} \times \frac{\text{Frame rate} \times \text{Number of colors} \times (\text{bpp})}{100}
$$

Example) Total number of display pixels = $480 \times 640$, Frame rate = 60 Hz,
Number of colors 16 bits, Overhead coefficient = 2.00, Bus clock = 108 MHz

$$
\text{Bus occupation ratio} = \frac{2.00 \times 480 \times 640 \times 60 \times 16}{108 \times 10^6 \times 32} \times 100 = 17.06\%
$$

Figure 2 shows the valid display and the retrace period.

![Figure 2](image-url)

Active Video = Top/ Left Border + Addressable Video + Bottom/ Right Border
Total H Blank = Hsync Time + Back Porch + Front Porch
Total V Blank = Vsync Time + Back Porch + Front Porch

HTCN = H Total Time
HDCN = H Addressable Video
HSYNP = H Addressable Video + Right Border + Front Porch
HSYNW = Hsync Time

VTLN = V Total Time
CDLN = V Addressable Video
VSYNP = V Addressable Video + Bottom Border + Front Porch
VSYNW = Vsync Time

Figure 2  Valid Display and the Retrace Period
2.1.5 Color Palette

Color palette registers are not set in the sample application. If a color palette is to be used, please refer to the SH7764 Group Hardware Manual (REJ09B0360). It gives an outline in this section.

This LCDC has a color palette which outputs 24 bits of data per entry and is able to simultaneously hold 256 entries. The color palette thus allows the simultaneous display of 256 colors chosen from among 16-M colors.

The procedure below may be used to set up color palettes at any time.

1. The PALEN bit in the LDPALCR is 0 (initial value); normal display operation
2. Access LDPALCR and set the PALEN bit to 1; enter color-palette setting mode after three cycles of peripheral clock.
3. Access LDPALCR and confirm that the PALS bit is 1.
4. Access LDPR00 to LDPRFF and write the required values to the PALD00 to PALDFF bits.
5. Access LDPALCR and clear the PALEN bit to 0; return to normal display mode after a cycle of peripheral clock.

Figure 3 shows the data format for a color-palette entry.

```
<table>
<thead>
<tr>
<th>Color</th>
<th>31</th>
<th>23</th>
<th>15</th>
<th>7</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>R7</td>
<td>R6</td>
<td>R5</td>
<td>P4</td>
<td>P3</td>
</tr>
<tr>
<td>Monochrome</td>
<td></td>
<td></td>
<td></td>
<td>M3</td>
<td>M2</td>
</tr>
</tbody>
</table>
```

Figure 3  Data Format for Color-Palette Entry

2.1.6 Clock and LCD Data Signal Example

Figure 4 shows the LCD data signal example.

```
DOTCLK
LCD_CL2
LCD_D15  R05  R15  R25  R35
LCD_D14  R04  R14  R24  R34
LCD_D13  R03  R13  R23  R33
LCD_D12  R02  R12  R22  R32
LCD_D11  R01  R11  R21  R31
LCD_D10  G05  G15  G25  G35
LCD_D9   G04  G14  G24  G34
LCD_D8   G03  G13  G23  G33
LCD_D7   G02  G12  G22  G32
LCD_D6   G01  G11  G21  G31
LCD_D5   G00  G10  G20  G30
LCD_D4   B05  B15  B25  B35
LCD_D3   B04  B14  B24  B34
LCD_D2   B03  B13  B23  B33
LCD_D1   B02  B12  B22  B32
LCD_D0   B01  B11  B21  B31
```

Figure 4  Clock and LCD Data Signal Example (TFT Color 16-Bit Data Bus Module)
2.1.7 Power-Supply Control Sequence

An LCD module normally requires a specific sequence for processing to do with the cutoff of the input power supply. Settings in LDPMMR, LDPSPR, and LDCNTR, in conjunction with the LCD power-supply control pins (LCD_VCPWC, LCD_VEPWC, and LCD_DON), are used to provide processing of power-supply control sequences that suits the requirements of the LCD module.

If LCD module power-supply control-sequence processing is in use by the LCDC or the supply of power is cut off while the LCDC is in its display-on mode, normal operation is not guaranteed. In the worst case, the connected LCD module may be damaged.

Figures 5 is timing charts that show outlines of power-supply control sequences and table 3 is a summary of available power-supply control sequence periods.

---

**Figure 5** Power-Supply Control Sequence and States of the LCD Module

**Table 3** Available Power-Supply Control-Sequence Periods at Typical Frame Rates

<table>
<thead>
<tr>
<th>ONX, OFFX Register Value</th>
<th>Frame Rate 120 Hz</th>
<th>Frame Rate 60 Hz</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>120 Hz</td>
<td>60 Hz</td>
</tr>
<tr>
<td>H'F</td>
<td>((-1+1)/120 = 0.00) (ms)</td>
<td>((-1+1)/60 = 0.00) (ms)</td>
</tr>
<tr>
<td>H'0</td>
<td>((0+1)/120 = 8.33) (ms)</td>
<td>((0+1)/60 = 16.67) (ms)</td>
</tr>
<tr>
<td>H'1</td>
<td>((1+1)/120 = 16.67) (ms)</td>
<td>((1+1)/60 = 33.33) (ms)</td>
</tr>
<tr>
<td>H'2</td>
<td>((2+1)/120 = 25.00) (ms)</td>
<td>((2+1)/60 = 50.00) (ms)</td>
</tr>
<tr>
<td>H'D</td>
<td>((13+1)/120 = 116.67) (ms)</td>
<td>((13+1)/60 = 233.33) (ms)</td>
</tr>
<tr>
<td>H'E</td>
<td>((14+1)/120 = 125.00) (ms)</td>
<td>((14+1)/60 = 250.00) (ms)</td>
</tr>
</tbody>
</table>
2.2 TFT-LCD Panel Specifications

Table 4 lists the specification of the TFT-LCD panel to use in this application. The specifications of the TFT-LCD panel used for this application note (LS037V7DW01, manufactured by Sharp Corporation) are listed in the table below. As detailed specifications differ with the TFT-LCD panel, be sure to check the data sheet for the product you will be using.

2.2.1 General Specifications

Table 4 lists the general specifications of the TFT-LCD panel to use in this application.

<table>
<thead>
<tr>
<th>Item</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>VGA or QVGA</td>
</tr>
<tr>
<td>Number of pixels</td>
<td>H 480 × V 640 (Number of dots: H (480 × 3) × V 640)</td>
</tr>
<tr>
<td>Pixel configuration</td>
<td>R, G, B vertical stripes</td>
</tr>
<tr>
<td>Number of colors</td>
<td>260,000 colors</td>
</tr>
<tr>
<td>Input signal</td>
<td>CMOS RGB (6 bits each digital)</td>
</tr>
</tbody>
</table>

2.2.2 Pin Functions

Table 5 lists the pin functions of the TFT-LCD panel used in this application.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESB</td>
<td>Reset signal</td>
</tr>
<tr>
<td>INI</td>
<td>Power-on control</td>
</tr>
<tr>
<td>DEN</td>
<td>Display-on signal</td>
</tr>
<tr>
<td>HSYNC</td>
<td>Horizontal sync signal</td>
</tr>
<tr>
<td>VSYNC</td>
<td>Vertical sync signal</td>
</tr>
<tr>
<td>CLKIN</td>
<td>Dot clock</td>
</tr>
<tr>
<td>R5-0</td>
<td>Red data signal (MSB: R5)</td>
</tr>
<tr>
<td>G5-0</td>
<td>Green data signal (MSB: G5)</td>
</tr>
<tr>
<td>B5-0</td>
<td>Blue data signal (MSB: B5)</td>
</tr>
</tbody>
</table>
2.2.3 Interface Timing

Figure 6 and figure 7 shows the interface timing of the TFT-LCD panel used in this application. Table 6 lists the timing characteristics.

![Interface Timing Diagram](image)

**Figure 6** TFT-LCD Panel Interface Timing Example (Excerpt from Datasheet)

![Power-Supply Sequence Diagram](image)

**Figure 7** TFT-LCD Panel Power-Supply Sequence (Excerpt from Datasheet)
<table>
<thead>
<tr>
<th>Item</th>
<th>MODE</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK</td>
<td>VGA</td>
<td>$t_{CLK}$</td>
<td>38</td>
<td>39.7</td>
<td>41.7</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>QVGA</td>
<td></td>
<td>152</td>
<td>158.8</td>
<td>167</td>
<td></td>
</tr>
<tr>
<td>Hsync</td>
<td>VGA</td>
<td>$t_{HS}$</td>
<td></td>
<td>648</td>
<td></td>
<td>CLK</td>
</tr>
<tr>
<td></td>
<td>QVGA</td>
<td></td>
<td></td>
<td>324</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Valid width</td>
<td>$t_{HSW}$</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vsync</td>
<td>VGA</td>
<td>$t_{VS}$</td>
<td></td>
<td>648</td>
<td></td>
<td>HCYC</td>
</tr>
<tr>
<td></td>
<td>QVGA</td>
<td></td>
<td></td>
<td>324</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Valid width</td>
<td>$t_{VSW}$</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DEN</td>
<td>VGA</td>
<td>$t_{HBP}$</td>
<td>28</td>
<td>78</td>
<td>166</td>
<td>$t_{CLK}$</td>
</tr>
<tr>
<td></td>
<td>QVGA</td>
<td></td>
<td>14</td>
<td>38</td>
<td>82</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VGA</td>
<td>$t_{HFP}$</td>
<td>0</td>
<td>88</td>
<td>138</td>
<td>$t_{CLK}$</td>
</tr>
<tr>
<td></td>
<td>QVGA</td>
<td></td>
<td>0</td>
<td>44</td>
<td>68</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Valid width</td>
<td>$t_{HHW}$</td>
<td></td>
<td>480</td>
<td></td>
<td>$t_{CLK}$</td>
</tr>
</tbody>
</table>
2.3 TFT-LCD Panel Circuit Example

2.3.1 Pin Connection Example

Figure 8 shows the TFT-LCD panel hardware connection in this application.

![TFT-LCD Panel Hardware Connection Diagram]

---

**Figure 8** TFT-LCD Panel Hardware Connection
2.4 Sample Program Specifications
This section describes the specifications of the sample program and shows the flow chart of each processing.

2.4.1 Specifications
- Outputs the graphic image to the VGA size (V 480 x H 640) TFT-LCD panel.
- Red, green, and blue bars are displayed on the panel.

2.4.2 Main Flow Chart of the Sample Program
Figure 9 shows the main flow chart of the sample program. Initialization of the LCDC by the sample program is shown in figures 10 to 12, and the display is turned on after execution of the processing shown in figure 13. After graphics have been displayed on the TFT-LCD panel over a certain period, the display is turned off following execution of the processing shown in figure 14.

![Main Flow Chart](image)

**Figure 9 Sample Program Main Flow**
2.4.3 Initialization of the LCDC

Figure 10 shows the flow for initialization of the LCDC.

- Select the multiplexed pins
  - [Functions]
  - LCD_DATA[15:0], LCD_CL2, LCD_CL1, LCD_CLK, LCD_FLM, LCD_M_DISP, LCD_DON, LCD_VCP_WC, LCD_VEP_WC pins

Figure 10 Flow for Initialization of the LCDC
2.4.4 Setting the LCDC

Figure 11 and figure 12 show the setting examples of the LCDC. Follow this procedure to set the control signal output for the TFT-LCD panel. Values listed in figure 11 and figure 12 are set according to the TFT-LCD panel specifications described in section 2.2.

- Set the LDICKR (H'2101) [Functions]
  - External clock is selected
  - Division ratio 1/1

- Set the LDMTR (H'C42B) [Functions]
  - VSYNC: low active
  - HSYNC: low active
  - DEN: high active
  - DATA: high active
  - M signal is not output
  - HSYNC output during vertical retrace period
  - DOTCLK output during vertical and horizontal retrace period
  - TFT color 16-bit select

- Set the LDDFR (H'012D) [Functions]
  - Byte data: Little endian
  - Display color: 64K colors (RGB: 565), 16 bpp

- Set the LDSARU [Functions]
  - Set the start address for data fetch of the display data

- Set the LDLAOR (H'1000) [Functions]
  - Set the line address offset

- Set the LDHCNR [Functions]
  - Set the horizontal display character number
  - Set the horizontal total character number

- Set the LDVDLNR [Functions]
  - Set the vertical display line number

- Set the LDVTLNR [Functions]
  - Set the vertical total line number

Figure 11 Setting Examples of the LCDC (1)
Set the LCDC horizontal sync signal register (LDHSYNR)

- Set the LDHSYNR
  [Functions]
  - Set the horizontal sync signal width
  - Set the horizontal sync signal output position

Set the LCDC vertical sync signal register (LDVSYNR)

- Set the LDVSYNR
  [Functions]
  - Set the vertical sync signal width
  - Set the vertical sync signal output position

Set the LCDC power management mode register (LDPMMR)

- Set the LDPMMR (H'0060)
  [Functions]
  - LCD_VCPWC pin used
  - LCD_VEPWC pin used

Set the LCDC power-supply sequence period register (LDPSPR)

- Set the LDPSPR (H'1050)
  [Functions]
  - Set the period from power being supplied to the start of synchronizing signal output.
  - Set the period from the start of synchronizing signal output to LCD power being turned on.
  - Set the period from LCD power being turned off to synchronizing signal output being stopped.
  - Set the period from synchronizing signal output being stopped to the power supply being shut down.

Set the LCDC memory access interval number register (LDLIRNR)

- Set the LDLIRNR (H'0000)
  [Functions]
  - Set the VRAM read bus cycle

END

Figure 12   Setting Examples of the LCDC (2)
2.4.5 Setting the LCDC Starts Display and LCDC Stops Display

Figure 13 shows the setting example of the LCDC starts display, and figure 14 shows the setting example of the LCDC stops display.

When 1s are written to the DON2 bit and the DON bit, the LCDC starts display. When 0 is written to the DON bit, the LCDC stops display.

When display starts or ends, LCDC operation must be in accord with the power-control sequences specified in section 2.4.4, Setting the LCDC. The DON bit must not be manipulated until the given sequence is complete.

![Figure 13](image1.png) Setting Examples of the Start of LCDC Display

![Figure 14](image2.png) Setting Examples of the Stop of LCDC Display
3. Sample Program "lcdc.c"

3.1 Listings of Sample Program "Macro definition"

```c
#include "iodefine.h"

/* ==== Macro definition ==== */
/* ---- TFT panel display module ---- */
#define TFT_TOTAL_CLOCK 648 /* Width including the blanking interval */
#define TFT_TOTAL_LINE 648 /* Height including the blanking interval */
#define TFT_PANEL_CLOCK 480 /* Number of pixels in horizontal direction */
#define TFT_PANEL_LINE 640 /* Number of pixels in vertical direction */
#define TFT_H_FRONT_PORCH 88 /* Horizontal front porch */
#define TFT_HSYNC_START (TFT_PANEL_CLOCK + TFT_H_FRONT_PORCH) /* Display start position in horizontal direction */
#define TFT_HSYNC_WIDTH 8 /* Hsync pulse width (min = 8 dots) */
#define TFT_VSYNC_WIDTH 1 /* Vsync pulse width */
#define LINE_OFFSET 2048 /* Line offset */

/* ==== Function prototype declaration ==== */
void lcdc_main(void);
void lcdc_initial(void);
void lcdc_port_set(void);
void lcdc_control_initial(void);
void lcdc_enable(void);
void lcdc_disable(void);
void fill_rect(unsigned int x, unsigned int y, unsigned int w, unsigned int h, unsigned short color, unsigned int base_address, unsigned int line_offset);
void delay(void);

/* ==== Variable definition ==== */
#pragma section _LCDC_FRAME_BUFFER /* Places on a 512-byte boundary in the cache disabled area */
unsigned short frame_buffer[TFT_PANEL_CLOCK][TFT_PANEL_LINE];

#pragma section
```

3.2 Listings of Sample Program "Display main"

```c
void lcdc_main(void)
{
    /* ---- Initializes the frame buffer ---- */
    fill_rect(0,0,TFT_PANEL_CLOCK / 3,TFT_PANEL_LINE,0xF800,
    (unsigned int)frame_buffer,LINE_OFFSET);
    fill_rect(TFT_PANEL_CLOCK / 3,0,(TFT_PANEL_CLOCK / 3) * 2,TFT_PANEL_LINE,0x07E0,
    (unsigned int)frame_buffer,LINE_OFFSET);
    fill_rect((TFT_PANEL_CLOCK / 3) * 2,0,TFT_PANEL_CLOCK,TFT_PANEL_LINE,0x001F,
    (unsigned int)frame_buffer,LINE_OFFSET);
    /* Draws a color bar in the frame buffer */

    /* ---- Initializes the LCDC module ---- */
    lcdc_initial();

    /* ---- Outputs the color bar on the TFT-LCD ---- */
    lcdc_enable();
    delay(); /* Waits for several seconds */
    lcdc_disable();
}
```
3.3 Listings of Sample Program "LCDC initialization"

```c
/*""FUNC COMMENT""*******************************************************************************
* ID          :
* Outline     : LCDC initialization
*------------------------------------------------------------------------------
* Include     :
*------------------------------------------------------------------------------
* Declaration : void lcdc_initial(void);
*------------------------------------------------------------------------------
* Function    :
*------------------------------------------------------------------------------
* Argument    : void
*------------------------------------------------------------------------------
* Return Value: void
*""FUNC COMMENT END""*******************************************************************************/

void lcdc_initial(void)
{
    lcdc_port_set();  /* I/O pin setting */
    lcdc_control_initial(); /* LCDC setting */
}
```
3.4 Listings of Sample Program "I/O pin setting"

```c
/*""FUNC COMMENT""*********************************************************************/
* ID          :
* Outline     : I/O pin setting
*------------------------------------------------------------------------------
* Declaration : void lcdc_port_set(void);
*------------------------------------------------------------------------------
* Function    : Sets I/O pins for the LCDC.
*------------------------------------------------------------------------------
* Argument    : void
*------------------------------------------------------------------------------
* Return Value: void
***""FUNC COMMENT END""*******************************************************************/

tvoid lcdc_port_set(void)
{
    /* ---- LCD_DATA15,14,13,12,11,10,9,8 ---- */
    GPIO.PTSEL_G.WORD = 0x0000;
    /* ---- LCD_CL2,LCD_DON,LCD_VCP_WC,LCD_VEP_WC ---- */
    GPIO.PTSEL_H.BIT._PTSEL_H3 = GPIO.PTSEL_H.BIT._PTSEL_H2 =
    GPIO.PTSEL_H.BIT._PTSEL_H1 =GPIO.PTSEL_H.BIT._PTSEL_H0 = 0;
    /* ---- LCD_DATA7,6,5,4,3,2,1 ---- */
    GPIO.PTSEL_I.WORD = 0x0000;
    /* ---- LCD_DATA0,LCD_CL1,LCD_CLK,LCD_FLM,LCD_M_DISP ---- */
    GPIO.PTSEL_K.BIT._PTSEL_K4 = GPIO.PTSEL_K.BIT._PTSEL_K3 =
    GPIO.PTSEL_K.BIT._PTSEL_K2 = GPIO.PTSEL_K.BIT._PTSEL_K1 =
    GPIO.PTSEL_K.BIT._PTSEL_K0 = 0;
}
```
3.5 Listings of Sample Program "LCDC initialization"

```c
/*""FUNC COMMENT""**********************************************************************
* ID          : 
* Outline     : LCDC initialization
*------------------------------------------------------------------------------
* Declaration : void lcdc_control_initial(void);
*------------------------------------------------------------------------------
* Function    : Initializes the LCDC.
*------------------------------------------------------------------------------
* Argument    : void
*------------------------------------------------------------------------------
* Return Value: void
*""FUNC COMMENT END""*******************************************************************/
void lcdc_control_initial(void)
{
    /* ---- Clock selection and divider setting ---- */
    LCDC.LDICKR.WORD = 0x2101;
    /* bit13:12(ICKSEL)=01 uses LCD_CLK (external pin) */
    /* bit5:0(DCDR)=000001 divider 1/1 */
    /* ---- Pin polarity selection ---- */
    LCDC.LDMTR.WORD = 0xC42B;
    /* bit15(FLMPOL)=1   VSync is "L" active */
    /* bit14(CL1POL)=1   Hsync is "L" active */
    /* bit13(DISPPOL)=0   DEN is "H" active */
    /* bit12(DPOL)=0   DATA is "H" active */
    /* bit10(MCNT)=1   M signal is not output */
    /* bit9(CL1CNT)=0   Hsync is output during the vertical interval */
    /* bit8(CL2CNT)=0   DotCLK is output during the vertical interval */
    /* bit5:0(MIFTYP)=101011 TFT color-16bit */
    /* ---- Data format setting ---- */
    LCDC.LDDFR.WORD = 0x012D;
    /* bit8(PABD)=1    Little endian */
    /* bit6:0(DSPCOLOR)=0101101 64k-Color RGB:5-6-5 */
    /* Setting for reading images from external memory ---- */
    LCDC.LDSARU = (unsigned long *)frame_buffer;
    /* ---- Line offset setting ---- */
    LCDC.LDLAOR = LINE_OFFSET * sizeof(short);
    /* ---- Settings of the horizontal display character and the total number of characters ---- */
    LCDC.LDHCNR.BIT._HDCN = (TFT_PANEL_CLOCK / 8) - 1;
    LCDC.LDHCNR.BIT._HTCN = (TFT_TOTAL_CLOCK / 8) - 1;
    /* ---- Settings of the vertical display line and the total number of lines ---- */
    LCDC.LDVTLNR.BIT._VTLN = TFT_TOTAL_LINE - 1;
    LCDC.LDVTLNR.BIT._VDLN = TFT_PANEL_LINE - 1;
    /* ---- Horizontal/vertical sync signal timing settings ---- */
    LCDC.LDHSYNR.BIT._HSYNW = (TFT_HSYNC_WIDTH / 8) - 1;
    LCDC.LDHSYNR.BIT._HSYNP = (TFT_HSYNC_START / 8) - 1;
    LCDC.LDVSYNR.BIT._VSYNW = TFT_VSYNC_WIDTH - 1;
    LCDC.LDVSYNR.BIT._VSYNP = (TFT_TOTAL_LINE - TFT_VSYNC_WIDTH) - 2;
    /* ---- Power control pin setting ---- */
    LCDC.LDPMMR.WORD = 0x0060;
    /* bit[6](VCPE) = 1   uses the LCD_VCPWC pin */
    /* bit[5](VEPE) = 1   uses the LCD_VEPE pin */
}```
LCDC.LDPSPR.WORD = 0x1050;

/* bit[15:12](ONA) = 0001 Power-on to start of the sync signal (33.33ms) */
/* bit[11:8](ONB) = 0000 Start of the sync signal to LCD power-on (16.67ms) */
/* bit[7:4](OFFE) = 0101 LCD power-off to end of the sync signal (100ms) */
/* bit[3:0](OFFF) = 0000 End of the sync signal to power-off (16.67ms) */

/* ---- VRAM read clock cycle interval setting ---- */
LCDC.LDLIRNR.WORD = 0x0000;

}
### Listings of Sample Program

"Start LCDC display operation, Stop LCDC display operation"

```c
void lcdc_enable(void)
{
    /* ---- Starts the LCDC display operation ---- */
    LCDC.LDCNTR.BIT._DON2 = 1;
    LCDC.LDCNTR.BIT._DON = 1;
    /* bit[4](DON2) = 1 Starts the LCDC display operation */
    /* bit[0](DON)  = 1 Display-on mode */
}

void lcdc_disable(void)
{
    /* ---- Stops the LCDC display operation ---- */
    LCDC.LDCNTR.BIT._DON = 0;
    /* bit[0](DON)  = 0 Display-off mode */
}
```
4. Documents for Reference

- Hardware Manual
  SH7764 Group Hardware Manual (REJ09B0360)
  The most up-to-date version of this document is available on the Renesas Technology Website.

- Software Manual (REJ09B0003)
  SH-4A Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.
Website and Support

Renesas Technology Website
http://www.renesas.com/

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http://www.renesas.com/inquiry
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