

HIP4080 and HIP4081 Power-up Application

The HIP4080 and HIP4081 H-Bridge Driver ICs require external circuitry to assure reliable start-up conditions of the upper drivers. If not addressed in the application, the H-bridge power MOSFETs may be exposed to shoot-through current, possibly leading to MOSFET failure. Following the instructions below will result in reliable start-up.

HIP4081

The HIP4081 has four inputs, one for each output. Outputs ALO and BLO are directly controlled by input ALI and BLI. By holding ALI and BLI low during start-up no shoot-through conditions can occur. To set the latches to the upper drivers such that the driver outputs, AHO and BHO, are off, the DIS pin must be toggled from low to high after power is applied. This is accomplished with a simple resistor divider, as shown below in Figure 1. As the V_{DD}/V_{CC} supply ramps from zero up, the DIS voltage is below its input threshold of 1.7V due to the R1/R2 resistor divider. When V_{DD}/V_{CC} exceeds approximately 9V to 10V, DIS becomes greater than the input threshold and the chip disables all outputs. It is critical that ALI and BLI be held low prior to DIS reaching its threshold

level of 1.7V while V_{DD}/V_{CC} is ramping up, so that shoot through is avoided. After power is up the chip can be enabled by the ENABLE signal which pulls the DIS pin low.

HIP4080

The HIP4080 does not have an input protocol like the HIP4081 that keeps both lower power MOSFETs off other than through the DIS pin. IN+ and IN- are inputs to a comparator that control the bridge in such a way that only one of the lower power devices is on at a time, assuming DIS is low. However, keeping both lower MOSFETs off can be accomplished by controlling the lower turn-on delay pin, LDEL, while the chip is enabled, as shown in Figure 2. Pulling LDEL to V_{DD} will indefinitely delay the lower turn-on delays through the input comparator and will keep the lower MOSFETs off. With the lower MOSFETs off and the chip enabled, i.e. DIS = low, IN+ or IN- can be switched through a full cycle, properly setting the upper driver outputs. Once this is accomplished, LDEL is released to its normal operating point. It is critical that IN+/IN- switch a full cycle while LDEL is held high, to avoid shoot-through. This start-up procedure can be initiated by the supply voltage and/or the chip enable command by the circuit in Figure 2.

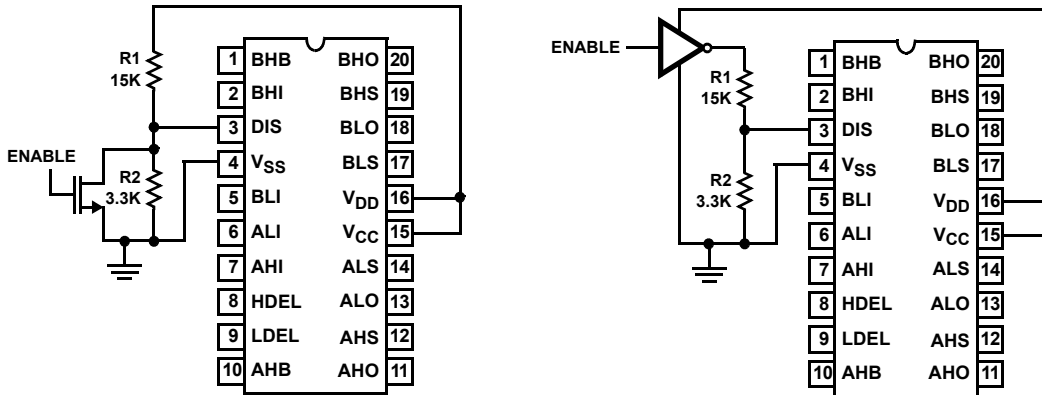


FIGURE 1.

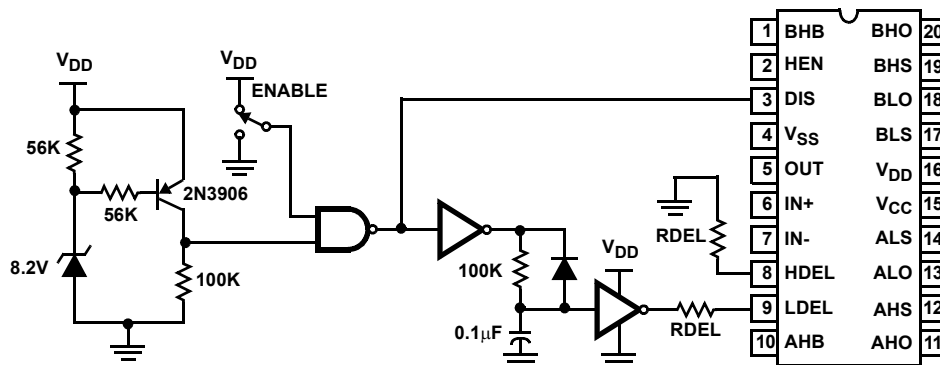
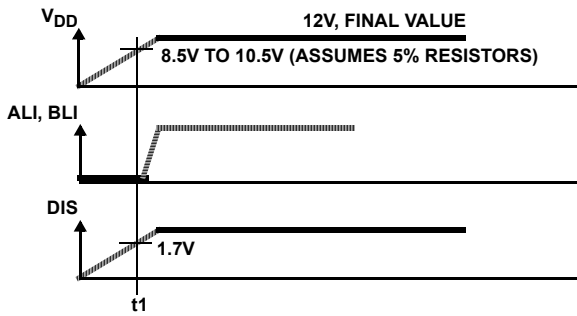


FIGURE 2.

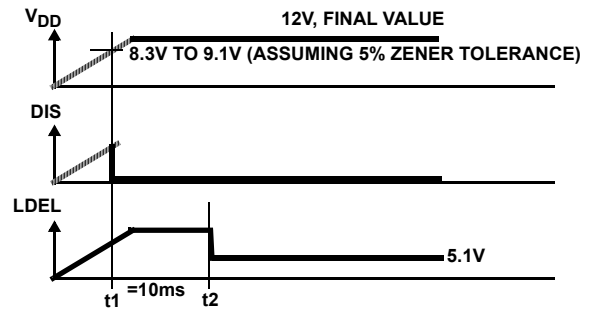
Timing Diagrams



NOTE:

1. ALI and/or BLI may be high after t₁, whereupon the ENABLE pin may also be brought high.

TIMING DIAGRAM FOR FIGURE 1.



NOTE:

1. Between t₁ and t₂ the IN⁺ and IN⁻ inputs must cause the OUT pin to go through one complete cycle (transition order is not important). If the ENABLE pin is low after the undervoltage circuit is satisfied, the ENABLE pin will initiate the 10ms time delay during which the IN⁺ and IN⁻ pins must cycle at least once.

TIMING DIAGRAM FOR FIGURE 2.

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Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852-2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886-2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338