ISL71030M

Radiation Tolerant 5V 16-Channel Analog Multiplexer

The ISL71030M is a radiation tolerant, 16-channel multiplexer that is fabricated using the proprietary P6 SOI process technology to provide excellent latch-up performance. It operates with a single supply range from 3V to 5.5V and has a 4-bit address line plus an enable that can be driven with adjustable logic thresholds to conveniently select one of 16 available channels. An inactive channel is separated from the active channel by a high impedance, which inhibits any interaction between the channels.

The ISL71030M low $r_{DS(ON)}$ allows for improved signal integrity and reduced power losses. The ISL71030M is also designed for cold sparing and is excellent for redundancy in high reliability applications. It is designed to provide a high impedance to the analog source in a powered-off condition, making it easy to add additional backup devices without incurring extra power dissipation. The ISL71030M also has analog overvoltage protection on the input that disables the switch during an overvoltage event to protect upstream and downstream devices.

The ISL71030M is available in a 32 Ld TQFP and operates across the extended temperature range of -55°C to +125°C.

Features

- **Fabricated using P6 SOI process technology**
- **Rail-to-rail operation**
- **No latch-up**
- **Low $r_{DS(ON)}$: <120Ω (maximum)**
- **Single supply operation: 3V to 5.5V**
- **Adjustable logic threshold control**
- **Cold sparing capable: -0.4V to 7V**
- **Analog overvoltage range: -0.4V to 7V**
- Switch input off leakage: 120nA
- Transition times (t_{AHL}): 70ns
- Break-before-make switching
- ESD protection ≥5kV (HBM)
- Passes NASA low outgassing specifications
- NiPdAu lead finish (Pb-free, Sn-free)
- Operating temperature range: -55°C to +125°C
- Radiation tolerance
  - Low dose rate (0.01rad(Si)/s): 30krad(Si)
  - SEL/SEB LET_{TH} (V+ = 6.5V): 43MeV•cm^2/mg

Applications

- Telemetry signal processing
- Harsh environments
  - Down-hole drilling

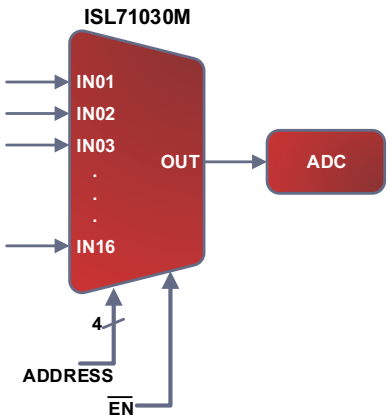


Figure 1. Typical Application

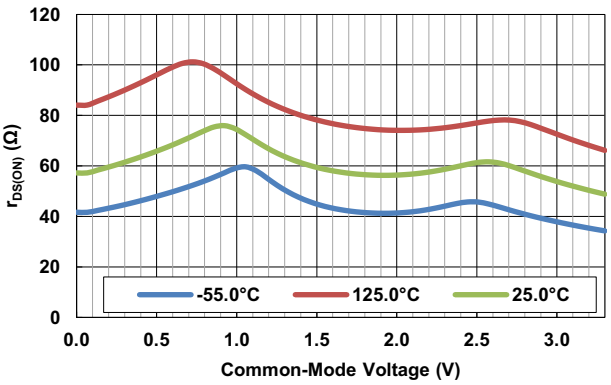


Figure 2. $r_{DS(ON)}$ vs Common-Mode Voltage (V+ = 4.5V)

Contents

1. Overview

1.1 Ordering Information

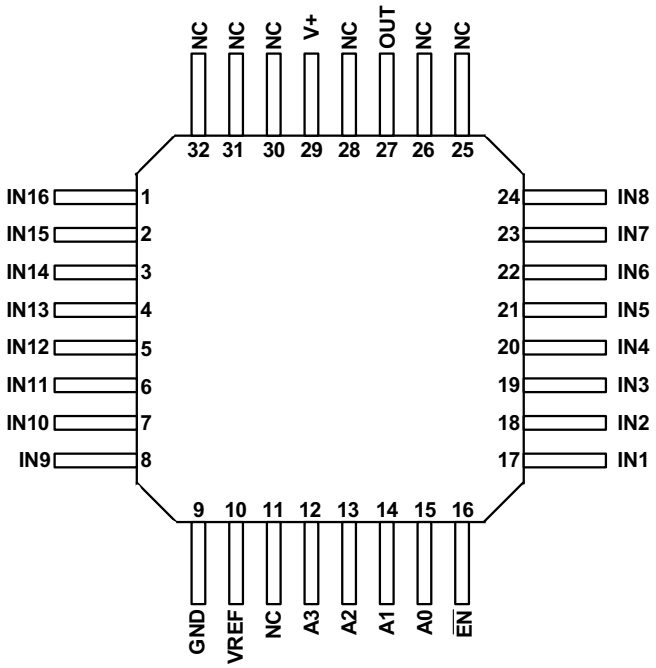
Part Number (Notes 2, 3)	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type (Note 1)	Temp. Range
ISL71030MNZ	ISL7103 0MNZ	32 Ld TQFP	Q32.5X5A	-	-55 to +125°C
ISL71030MNZ-T				1k	
ISL71030MNZ-T7A				250	

Notes:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL71030M device page. For more information about MSL, see TB363.

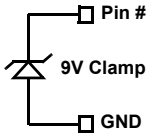
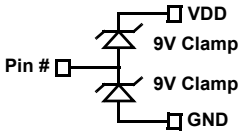
2. Pin Information

2.1 Pin Assignments



Top View

2.2 Pin Descriptions

Pin Number	ESD Circuit	Pin Name	Description
1, 2, 3, 4, 5, 6, 7, 8, 17, 18, 19, 20, 21, 22, 23, 24	1	INx	Multiplexer input
9	-	GND	Ground
10	1	VREF	Reference voltage that sets logic thresholds.
11, 25, 26, 28, 30, 31, 32	-	NC	Not electrically connected
12, 13, 14, 15	1	Ax	Multiplexer address lines
16	1	$\overline{EN}$	Multiplexer Enable control (active low).
27	2	OUT	Multiplexer output
29	1	V+	Positive power supply
 Circuit 1			 Circuit 2

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
Maximum Supply Voltage (V+ to GND)		7	V
Maximum Supply Voltage (V+ to GND) (Note 4)		6.5	V
Analog Input Voltage Range (INx)	-0.4	7	V
Digital Input Voltage Range (EN, Ax)	GND - 0.4	VREF	V
VREF to GND		7	V
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per MIL-STD-883 TM 3015)	5		kV
Charged Device Model (Tested per JS-002-2014)	500		V

Note:
4. Tested in a heavy ion environment at LET=43 MeV•cm^2/mg

3.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32 Ld TQFP (Notes 5, 6)	61	26

Notes:
5. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379.
6. For θ_{JC}, the “case temp” location is taken at the package top center.

Parameter	Minimum	Maximum	Unit
Maximum Operating Junction Temperature		+150	°C
Pb-Free Reflow Profile	See TB493		

3.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage, V_{CC}	3	5.5	V
Ambient Operating Temperature Range	-55	+125	°C
V_{REF} to GND	3	5.5	V

3.4 Electrical Specifications, V+ = 5V

Recommended operating conditions, GND = 0V, V_{REF} = 5V, V_{IH} = 5V, V_{IL} = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over at total ionizing dose of 30krad(Si) with exposure at a low dose rate of <43 MeV•cm^2/mg.**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Analog Input Signal Range	V_{IN}		0		V+	V
Channel On-Resistance	$r_{DS(ON)}$	V+ = 4.5V, V_{IN} = 0V to V+ I_{OUT} = 1mA		40	**120**	Ω
$r_{DS(ON)}$ Match Between Channels	$\Delta r_{DS(ON)}$	V+ = 4.5V, V_{IN} = 0V, 2.25V, 4.5V I_{OUT} = 1mA			**5**	Ω
On-Resistance Flatness	$r_{FLAT(ON)}$	V+ = 4.5V, V_{IN} = 0V to V+			**40**	Ω

Recommended operating conditions, GND = 0V, V_{REF} = 5V, V_{IH} = 5V, V_{IL} = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over at total ionizing dose of 30krad(Si) with exposure at a low dose rate of <43 MeV•cm^2/mg. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Switch Input Off Leakage	$I_{IN(OFF)}$	V+ = 5.5V, V_{IN} = 5V, Unused inputs and V_{OUT} = 0.5V	**-30**		**30**	nA
		V+ = 5.5V, V_{IN} = 0.5V, Unused inputs and V_{OUT} = 5V	**-30**		**30**	nA
Switch Input Off Overvoltage Leakage	$I_{IN(OFF-0V)}$	V+ = 5.5V, V_{IN} = 7V, Unused inputs and V_{OUT} = 0V, T_A = +25°C, -55°C	-30		30	nA
		T_A = +125°C	-30		120	nA
		Post radiation, +25°C	-30		30	nA
Switch Input Off Leakage with Supply Voltage Grounded	$I_{IN(POWER-OFF)}$	V_{IN} = 7V, V_{OUT} = 0V, V+ = V_{EN} = V_{REF} = 0V, T_A = +25°C, -55°C	-20		20	nA
		T_A = +125°C	-20		50	nA
		Post radiation, +25°C	-20		20	nA
Switch Input Off Leakage with Supply Voltage Open	$I_{IN(POWER-OFF)}$	V_{IN} = 7V, V_{OUT} = 0V V+ = V_{EN} = V_{REF} = Open, T_A = +25°C, -55°C	-20		20	nA
		T_A = +125°C	-20		50	nA
		Post radiation, +25°C	-20		20	nA
Switch On Input Leakage with Overvoltage Applied to Input	$I_{IN(ON-0V)}$	V+ = 5.5V, V_{IN} = 7V, V_{OUT} = OPEN	**2.75**		**5.50**	µA
Switch Output Off Leakage	$I_{OUT(OFF)}$	V+ = 5.5V, V_{OUT} = 5V, All inputs = 0.5V, T_A = +25°C, -55°C	-30		30	nA
		T_A = +125°C	0		150	nA
		Post radiation, +25°C	-30		30	nA
		V+ = 5.5V, V_{OUT} = 0.5V, All inputs = 5V, T_A = +25°C, -55°C	**-30**		**30**	nA
		Post radiation, +25°C	-30		30	nA
Switch Output Leakage with Switch Enabled	$I_{OUT(ON)}$	V+ = 5.5V, V_{IN} = V_{OUT} = 5V All unused inputs at 0.5V, T_A = +25°C, -55°C	-30		30	nA
		T_A = +125°C	0		150	nA
		Post radiation, +25°C	-30		30	nA
		V+ = 5.5V, V_{IN} = V_{OUT} = 0.5V All unused inputs at 5V	**-30**		**30**	nA
		Post radiation, +25°C	-30		30	nA
Logic Input Voltage High/Low	$V_{IH/L}$	V+ = 5.5V, V_{REF} = 3.3V	**1.3**		**1.6**	V
Input Current with V_{AH}, V_{ENH}	I_{AH}, I_{ENH}	V+ = 5.5V, V_{EN} = V_A = V_{REF}	**-0.1**		**0.1**	µA
Input Current with V_{AL}, V_{ENL}	I_{AL}, I_{ENL}	V+ = 5.5V, V_{EN} = V_A = 0V	**-0.1**		**0.1**	µA
Quiescent Supply Current	I_{SUPPLY}	V+ = V_{REF} = V_{EN} = 5.5V V_A = 0V, T_A = +25°C, -55°C			100	nA
		T_A = +125°C			300	nA
		Post radiation, +25°C			300	nA
Reference Quiescent Supply Current	I_{REF}	V+ = V_{REF} = V_{EN} = 5.5V V_A = 0V			**200**	nA
Dynamic						
Addressing Transition Time	t_{AHL}	V+ = 4.5V; Figure 3	**10**		**70**	ns

Recommended operating conditions, GND = 0V, V_{REF} = 5V, V_{IH} = 5V, V_{IL} = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over at total ionizing dose of 30krad(Si) with exposure at a low dose rate of <43 MeV•cm^2/mg. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Break-Before-Make-Delay	t_{BBM}	V+ = 4.5V; Figure 7	**5**	18	**40**	ns
Enable Turn-On Time	$t_{EN(ON)}$	V+ = 4.5V; Figure 5			**40**	ns
Enable Turn-Off Time	$t_{EN(OFF)}$	V+ = 4.5V; Figure 5			**40**	ns
Charge Injection	V_{CTE}	C_L = 100pF, V_{IN} = 0V, Figure 9		1.4	5	pC
Off Isolation	V_{ISO}	V_{EN} = V_{REF}, R_L = OPEN, f = 1kHz	**60**			dB
Crosstalk	V_{CT}	V_{EN} = 0V, f = 1kHz, V_{P-P} = 1V, R_L = OPEN	**73**			dB
Input Capacitance	$C_{IN(OFF)}$	f = 1MHz			**5**	pF
Output Capacitance	$C_{OUT(OFF)}$	f = 1MHz			**25**	pF

3.5 Electrical Specifications, V+ = 3.3V

Recommended operating conditions, GND = 0V, V_{REF} = 3.3V, V_{IH} = 3.3V, V_{IL} = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over at total ionizing dose of 30 krad(Si) with exposure at a low dose rate of 43 MeV•cm^2/mg.**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Analog Input Signal Range	V_{IN}		0		V+	V
Channel On-Resistance	$r_{DS(ON)}$	V+ = 3V, V_{IN} = 0V to V+, I_{OUT} = 1mA	**25**	70	**200**	Ω
$r_{DS(ON)}$ Match Between Channels	$\Delta r_{DS(ON)}$	V+ = 3V, V_{IN} = 0.5V, 2.5V, I_{OUT} = 1mA			5	Ω
On-Resistance Flatness	$r_{FLAT(ON)}$	V+ = 3V, V_{IN} = 0V to V+			**50**	Ω
Switch Input Off Leakage	$I_{IN(OFF)}$	V+ = 3.6V, V_{IN} = 3.1V, Unused inputs and V_{OUT} = 0.5V	**-30**		**30**	nA
		V+ = 3.6V, V_{IN} = 0.5V, Unused inputs and V_{OUT} = 3.1V	**-30**		**30**	nA
Switch Input Off Overvoltage Leakage	$I_{IN(OFF-OV)}$	V+ = 3.6V, V_{IN} = 7V, Unused inputs and V_{OUT} = 0V, T_A = +25°C, -55°C	-30		30	nA
		T_A = +125°C	-30		100	nA
		Post radiation, +25°C	-30		30	
Switch On Input Leakage with Overvoltage Applied to the Input	$I_{IN(ON-OV)}$	V+ = 3.6V, V_{IN} = 7V, V_{OUT} = OPEN	**1.8**		**3.6**	µA
Switch Output Off Leakage	$I_{OUT(OFF)}$	V+ = 3.6V, V_{OUT} = 3.1V, All inputs = 0.5V, T_A = +25°C, -55°C	-30		30	nA
		T_A = +125°C	0		60	nA
		Post radiation, +25°C	-30		30	nA
		V+ = 3.6V, V_{OUT} = 0.5V, All inputs = 3.1V, T_A = +25°C, -55°C	-30		30	nA
		T_A = +125°C	0		30	nA
		Post radiation, +25°C	-30		30	nA

Recommended operating conditions, GND = 0V, V_{REF} = 3.3V, V_{IH} = 3.3V, V_{IL} = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over at total ionizing dose of 30 krad(Si) with exposure at a low dose rate of 43 MeV•cm^2/mg. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Switch Output Leakage with Switch Enabled	$I_{OUT(ON)}$	V+ = 3.6V, V_{IN} = V_{OUT} = 3.1V All unused inputs at 0.5V, T_A = +25°C, -55°C	-30		30	nA
		T_A = +125°C	0		30	nA
		Post radiation, +25°C	-30		30	nA
		V+ = 3.6V, V_{IN} = V_{OUT} = 0.5V All unused inputs at 3.1V, T_A = +25°C, -55°C	-30		30	nA
		T_A = +125°C	0		30	nA
		Post radiation, +25°C	-30		30	nA
Quiescent Supply Current	I_{SUPPLY}	V+ = V_{REF} = V_{EN} = 3.6V V_A = 0V, T_A = +25°C, -55°C			100	nA
		T_A = +125°C			300	nA
		Post radiation, +25°C			300	nA
Reference Quiescent Supply Current	I_{REF}	V+ = V_{REF} = V_{EN} = 3.6V, V_A = 0V			**200**	nA
Dynamic						
Addressing Transition Time	t_{AHL}	V+ = 3V; Figure 3	**10**		**100**	ns
Break-Before-Make Delay	t_{BBM}	V+ = 3V; Figure 7	**5**	25	**50**	ns
Enable Turn-On Time	$t_{EN(ON)}$	V+ = 3V; Figure 5			**50**	ns
Enable Turn-Off Time	$t_{EN(OFF)}$	V+ = 3V; Figure 5			**50**	ns

Note:
7. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

3.6 Truth Table

A3	A2	A1	A0	$\overline{EN}$	"ON" Channel
X	X	X	X	1	None
0	0	0	0	0	1
0	0	0	1	0	2
0	0	1	0	0	3
0	0	1	1	0	4
0	1	0	0	0	5
0	1	0	1	0	6
0	1	1	0	0	7
0	1	1	1	0	8
1	0	0	0	0	9
1	0	0	1	0	10
1	0	1	0	0	11
1	0	1	1	0	12
1	1	0	0	0	13
1	1	0	1	0	14
1	1	1	0	0	15
1	1	1	1	0	16

Note: X = Don't care, 1 = Logic High, 0 = Logic Low.

3.7 Timing Diagrams

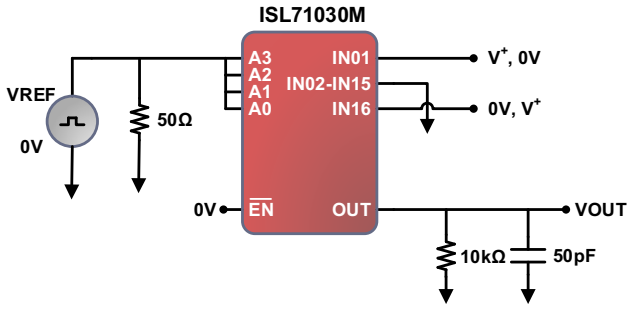


Figure 3. Address Time to Output Test Circuit

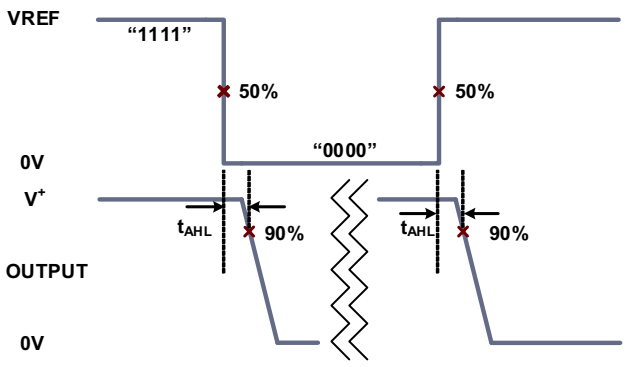


Figure 4. Address Time to Output Diagram

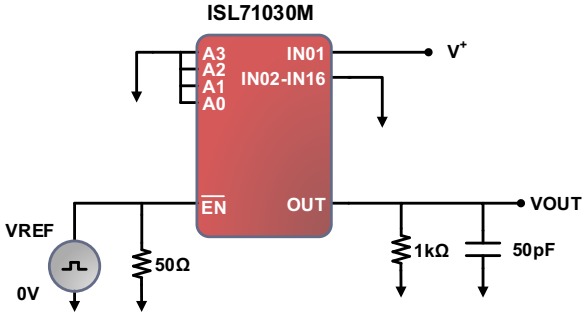


Figure 5. Time to Enable/Disable Output Test Circuit

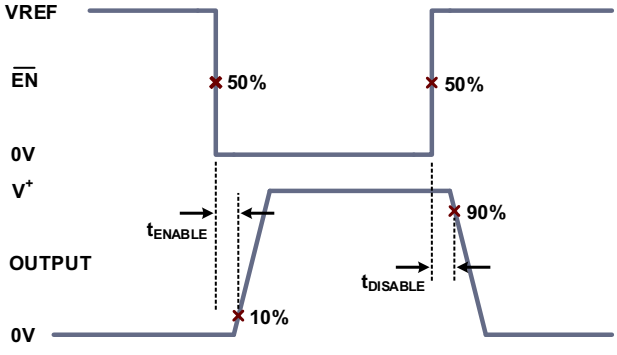


Figure 6. Time to Enable/Disable Output Diagram

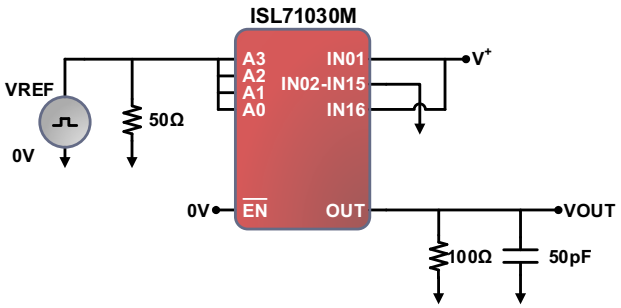


Figure 7. Break-Before-Make Test Circuit

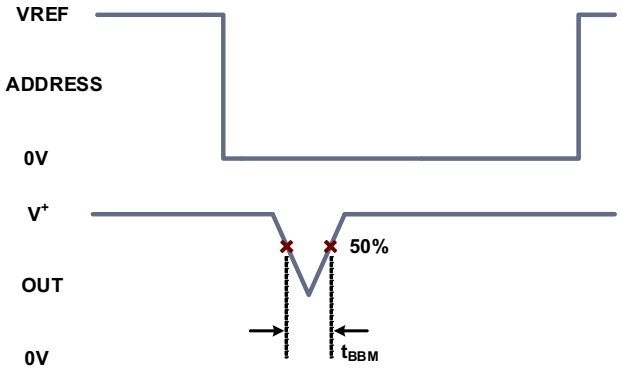


Figure 8. Break-Before-Make Diagram

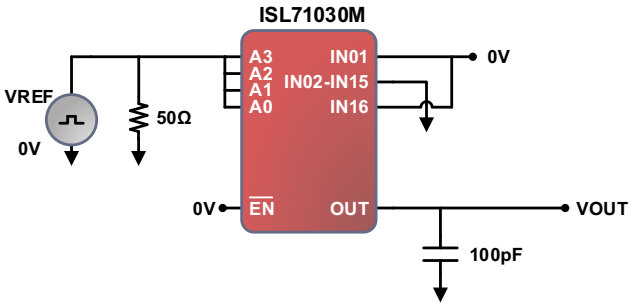


Figure 9. Charge Injection Test Circuit

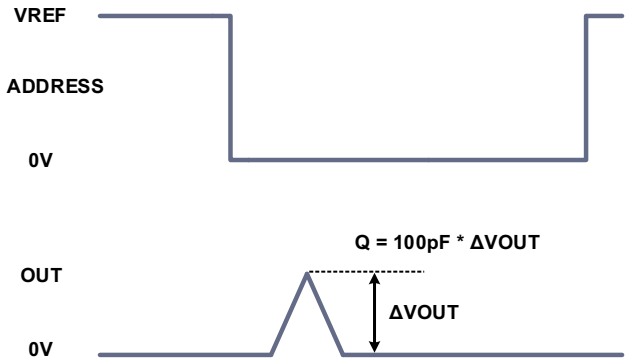


Figure 10. Charge Injection Diagram

4. Typical Performance Graphs

V+ = 5V, V_{REF} = 3.3V, V_{IN} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified

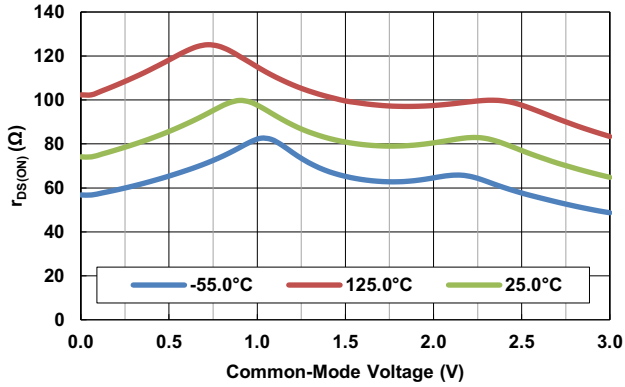


Figure 11. $r_{DS(ON)}$ vs Common-Mode Voltage (V+ = 3V)

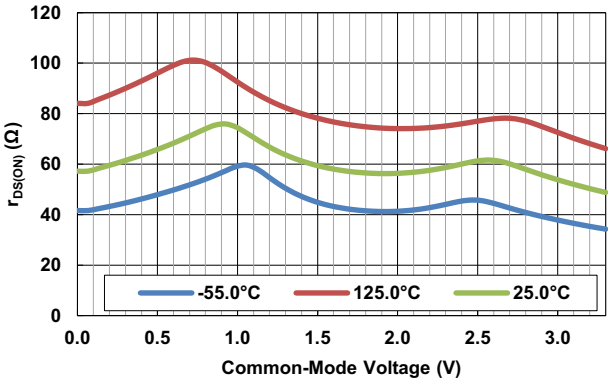


Figure 12. $r_{DS(ON)}$ vs Common-Mode Voltage (V+ = 4.5V)

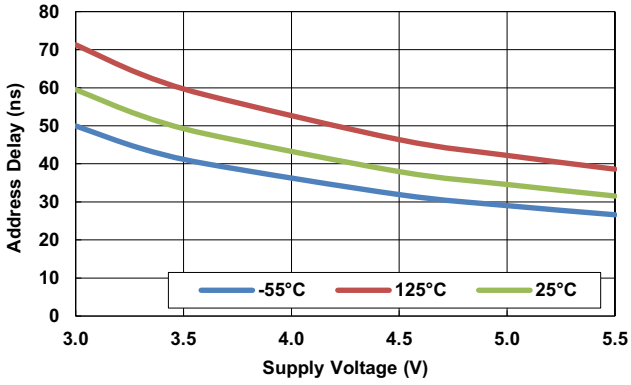


Figure 13. Address Propagation Delay (High to Low)

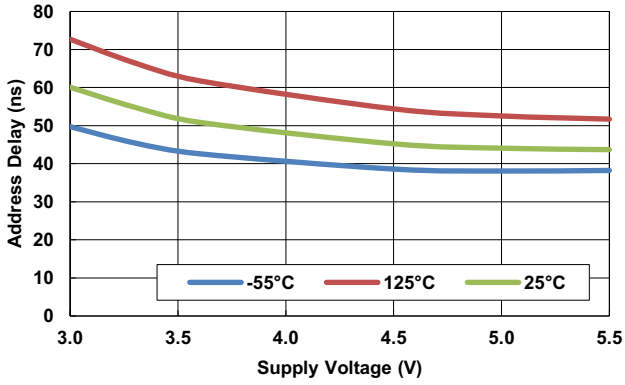


Figure 14. Address Propagation Delay (Low to High)

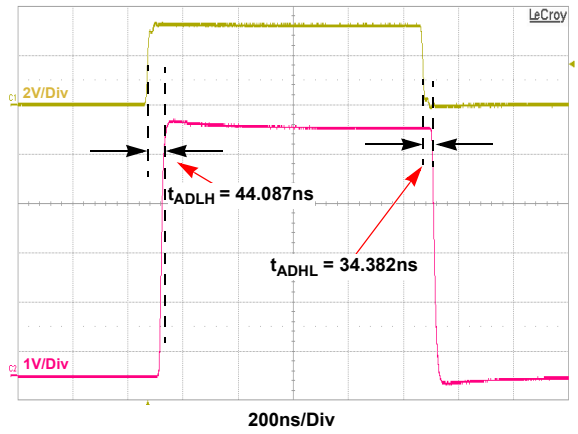


Figure 15. Address Propagation Delay

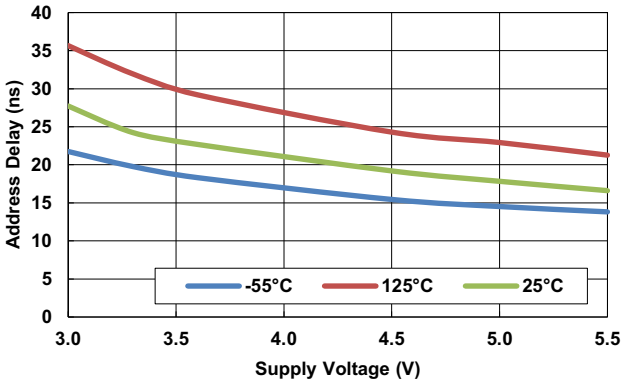


Figure 16. Break-Before-Make Delay

V+ = 5V, V_{REF} = 3.3V, V_{IN} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified **(Continued)**

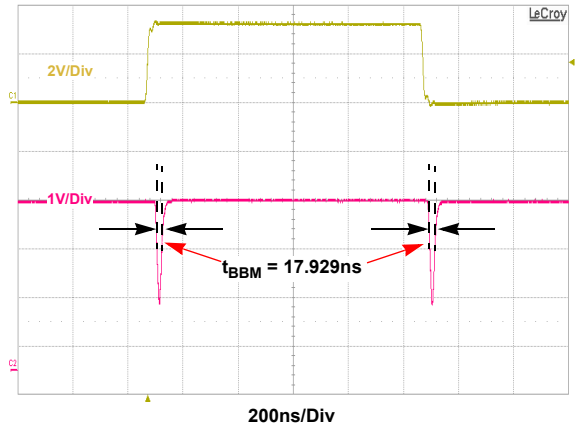


Figure 17. Break-Before-Make Delay

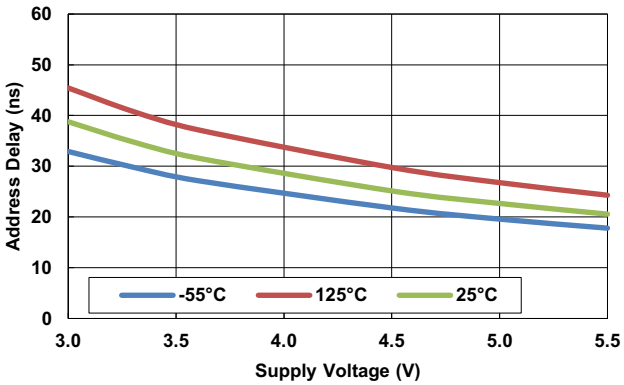


Figure 18. Enable to Output Propagation Delay

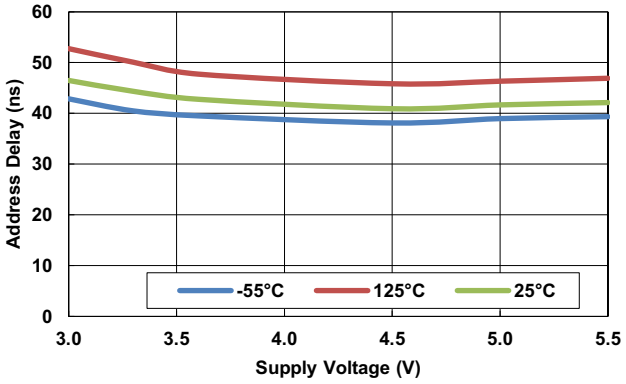


Figure 19. Disable to Output Propagation Delay

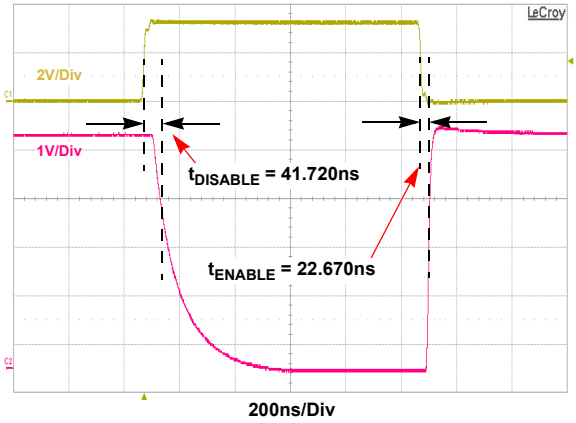


Figure 20. Enable/Disable Propagation Delay

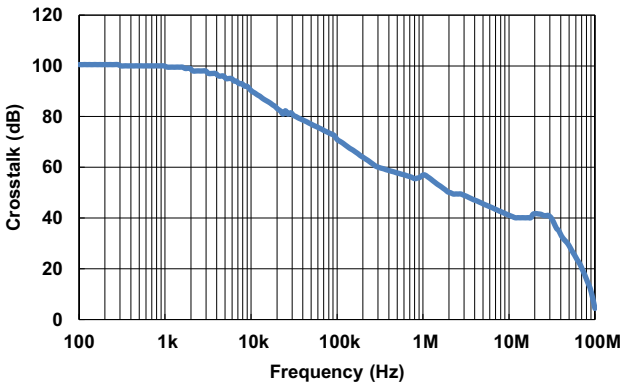


Figure 21. Off Isolation (V+ = 5V, +25°C, R_L = 511Ω)

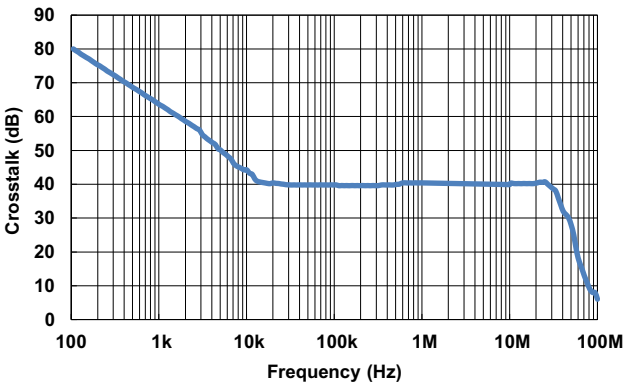


Figure 22. Off Isolation (V+ = 5V, +25°C, R_L= Open)

V+ = 5V, V_{REF} = 3.3V, V_{IN} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified **(Continued)**

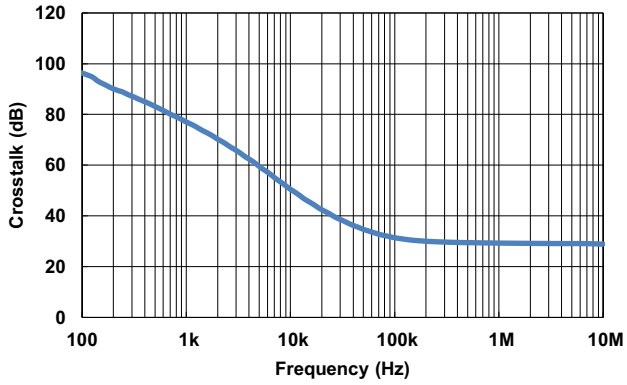


Figure 23. Crosstalk (V+ = 5V, +25°C, R_L = Open)

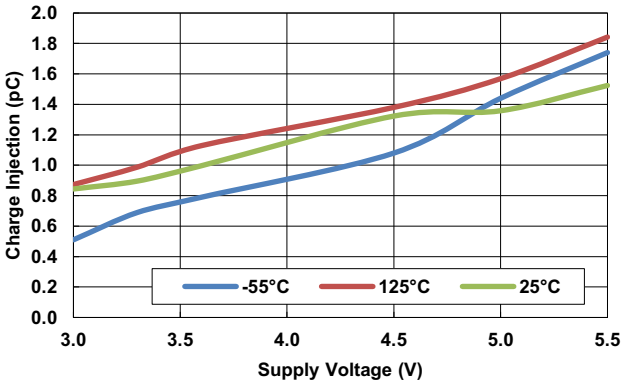


Figure 24. Charge Injection

5. Application Information

5.1 Power-Up Considerations

The circuit is insensitive to any given power-up sequence between V+ and VREF; however, Renesas recommends that all supplies power up relatively close to each other.

5.2 Overvoltage Protection

The ISL71030M has overvoltage protection on both the input and the output. On the output, the voltage is limited to a diode past the rails. Each of the inputs has independent overvoltage protection that works regardless of the switch being selected. If a switch experiences an overvoltage condition, the switch is turned off. As soon as the voltage returns within the rails, the switch returns to normal operation.

5.3 VREF and Logic Functionality

The VREF pin sets the logic threshold for the ISL71030M. The range for VREF is between 3V and 5.5V. The switching point is set to around 50% of the voltage presented to VREF. This switching point allows for both 5V and 3.3V logic control.

5.4 Considerations for Redundant Applications

When using the ISL71030M in a cold sparing application, Renesas recommends keeping the ground pin connected to system ground at all times. Both supply pins (V+ and VREF) should either be grounded or floating together.

If the supply pins are floating, Renesas recommends placing a high value bleed resistor (~1MΩ) in parallel with the decoupling capacitors on each supply pin to ensure that the supply voltage is discharged in a predictable manner. Figures 25 and 26 illustrate the recommended cold sparing setup for both shorted and floating supplies.

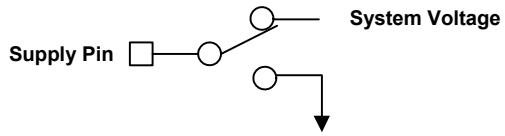


Figure 25. Cold Sparing Setup with Supplies Shorted

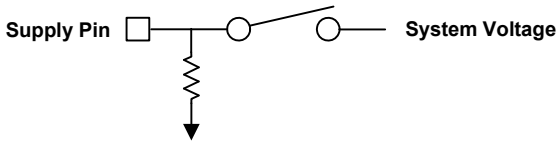


Figure 26. Cold Sparing Setup with Supplies Floating

6. Radiation Tolerance

The ISL71030M is a radiation tolerant device for commercial space applications, Low Earth Orbit (LEO) applications, high altitude avionics, launch vehicles, and other harsh environments. This device's response to Total Ionizing Dose (TID) radiation effects and Single-Event Effects (SEE) has been measured, characterized, and reported in the following sections. However, TID performance is not guaranteed through radiation acceptance testing, nor is the SEE characterized performance guaranteed.

6.1 Total Ionizing Dose (TID) Testing

6.1.1 Introduction

This test was conducted to determine the sensitivity of the part to the total dose environment. Test downpoints were 0krad(Si), 10krad(Si), 20krad(Si), and 30krad(Si). The irradiations were followed by a biased anneal for 168 hours at +100°C. Total dose testing was performed using a Hopewell Designs N40 paronormic 60Co irradiator. The irradiations were performed at 0.00875rad(Si)/s. A PbAl box was used to shield the test fixture and devices under test against low energy secondary gamma radiation. The characterization matrix consisted of 24 samples irradiated under bias and 12 samples irradiated with all pins grounded.

Four control units were used to ensure repeatable data. Two different wafers were used.

6.1.2 Results

Table 1 summarizes the attributes data. "Bin 1" indicates a device that passes all datasheet specification limits.

Table 1. Total Dose Test Attributes Data

Dose Rate	Bias	Sample Size	Downpoint	Bin 1	Rejects
8.75	Biased	16	Pre-rad	16	0
			10krad(Si)	16	0
			20krad(Si)	16	0
			30krad(Si)	16	0
			Anneal	16	0
8.75	Grounded	16	Pre-rad	16	0
			10krad(Si)	16	0
			20krad(Si)	16	0
			30krad(Si)	16	0
		8	Anneal	16	0

Figures 27 through 38 show data for key parameters at all downpoints. The plots show the average as a function of total dose for each of the irradiation conditions; we chose to use the average because of the relatively large sample sizes. All parts showed excellent stability over radiation.

6.1.3 Typical Radiation Performance Graphs

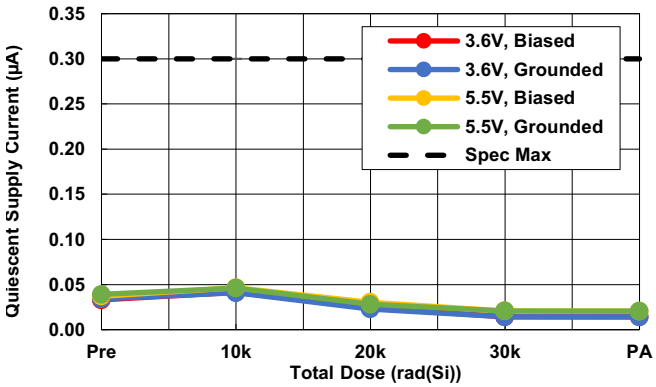


Figure 27. Quiescent Supply Current

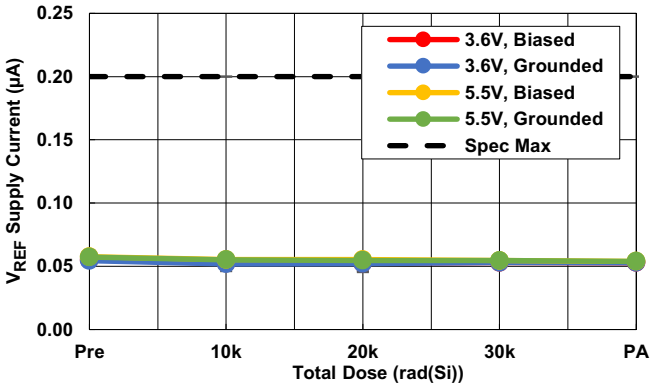


Figure 28. VREF Supply Current vs TID

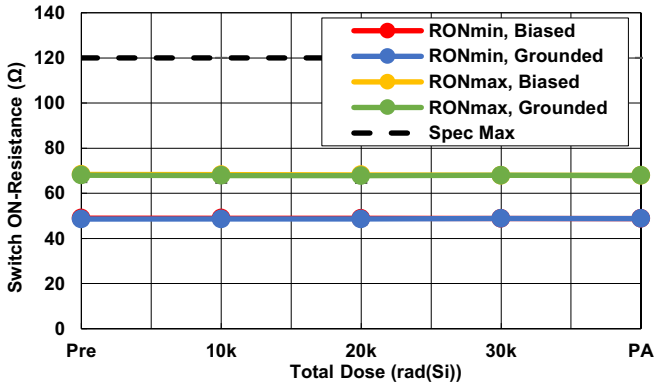


Figure 29. Switch ON Resistance vs TID

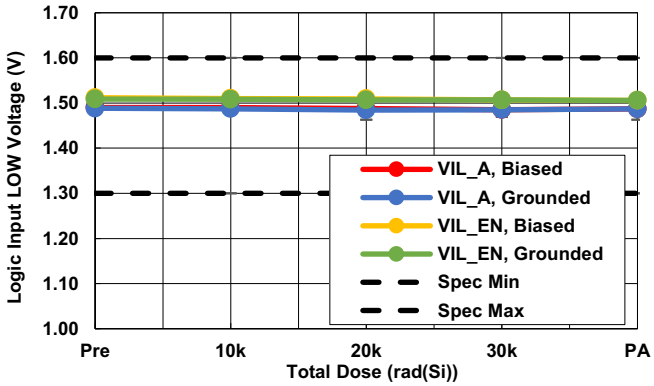


Figure 30. Logic Input LOW Voltage vs TID

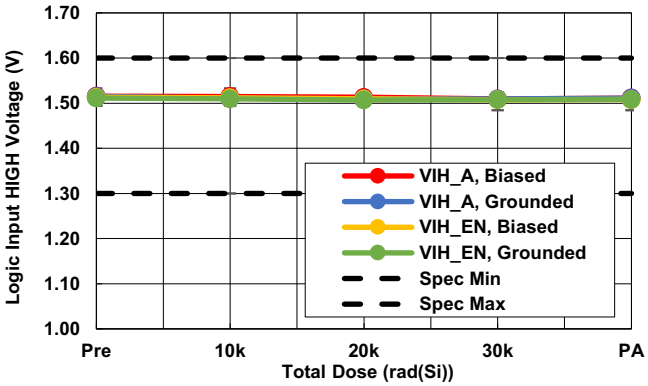


Figure 31. Logic Input HIGH Voltage vs TID

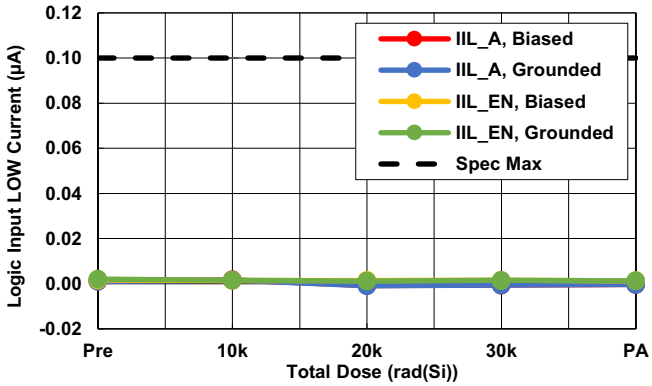


Figure 32. Logic Input LOW Current vs TID

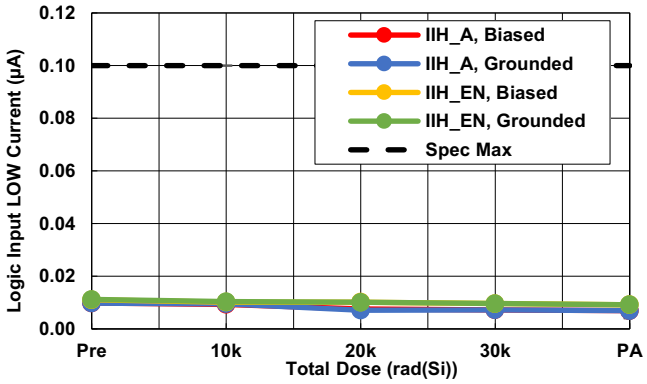


Figure 33. Logic Input HIGH Current vs TID

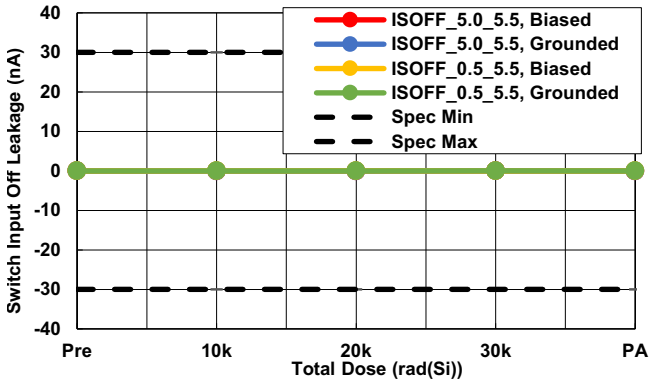


Figure 34. Switch Input Off Leakage vs TID

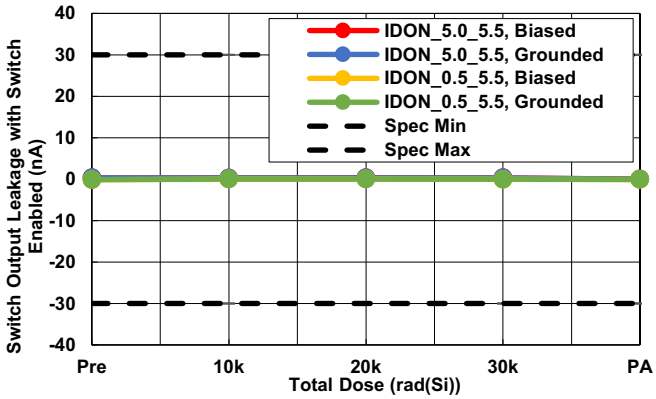


Figure 35. Output Leakage with Switch Enabled vs TID

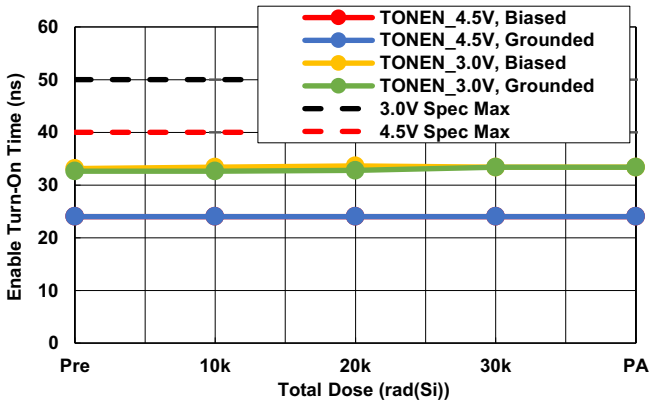


Figure 36. Enable Turn-On Time vs TID

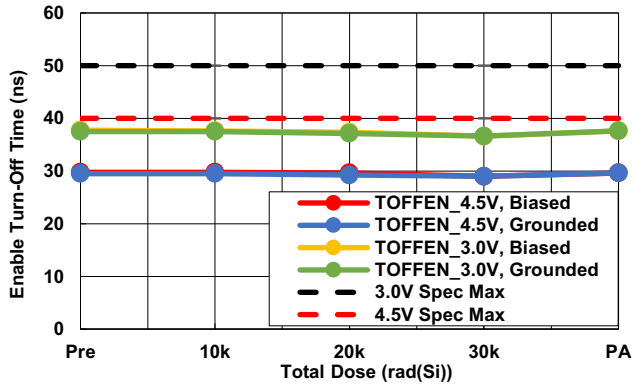


Figure 37. Enable Turn-Off Time vs TID

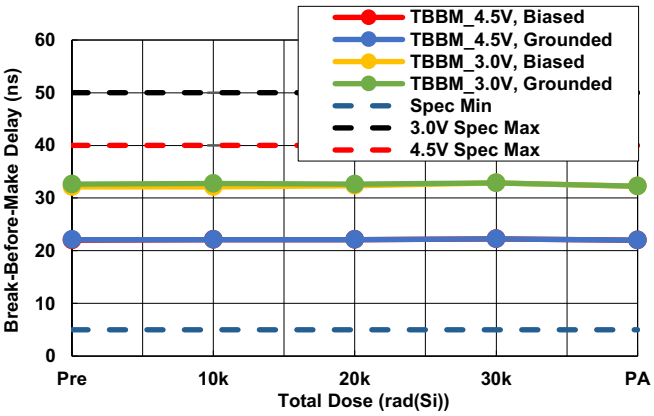


Figure 38. Break-Before-Make Delay vs TID

6.1.4 Conclusion

The ISL71030M 16-channel analog multiplexer was tested at low dose rate under biased and unbiased conditions to 30krad(Si) as outlined in MIL-STD-883 Test Method 1019.7. The samples were also taken through a high temperature biased anneal at 100C for 168 hours. ATE characterization testing at each down-point showed no rejects to the datasheet limits after irradiation or after the high temperature anneal. All parameters showed excellent stability.

Table 2. ISL71030M Response of Key Parameters vs TID

Parameter	Condition	Bias	Pre-Rad Value	10krad(Si)	20krad(Si)	30krad(Si)	Post Anneal	Units
Switch ON-Resistance	Min	Avg (Biased)	48.99	48.98	48.87	48.84	48.80	Ω
		Avg (Unbiased)	48.60	48.62	48.61	48.84	48.80	Ω
	Max	Avg (Biased)	68.36	68.26	68.18	67.95	67.89	Ω
		Avg (Unbiased)	68.01	67.91	67.83	67.95	67.89	Ω
		Limit -	-	-	-	-	-	Ω
		Limit +	120	120	120	120	120	Ω
Switch ON-Resistance Match Between Channels		Avg (Biased)	1.01	1.06	1.14	1.08	1.00	Ω
		Avg (Unbiased)	1.02	1.04	1.04	1.08	1.00	Ω
		Limit -	-	-	-	-	-	Ω
		Limit +	5	5	5	5	5	Ω
Switch ON-Resistance Flatness		Avg (Biased)	19.38	19.28	19.31	19.10	19.10	Ω
		Avg (Unbiased)	19.41	19.29	19.22	19.10	19.10	Ω
		Limit -	-	-	-	-	-	Ω
		Limit +	40	40	40	40	40	Ω
Switch Input Off Leakage		Avg (Biased)	-0.004	-0.111	-0.039	0.006	-0.057	nA
		Avg (Unbiased)	-0.002	-0.098	-0.044	0.006	-0.057	nA
		Limit -	-30	-30	-30	-30	-30	nA
		Limit +	30	30	30	30	30	nA
Switch Input Off Overvoltage Leakage		Avg (Biased)	0.00	-0.11	-0.04	0.01	-0.06	nA
		Avg (Unbiased)	0.00	-0.10	-0.04	0.01	-0.06	nA
		Limit -	-30	-30	-30	-30	-30	nA
		Limit +	30	30	30	30	30	nA
Switch Input Off Leakage with Supply Voltage Grounded		Avg (Biased)	0.08	0.10	0.10	0.22	0.16	nA
		Avg (Unbiased)	0.07	0.12	0.20	0.22	0.16	nA
		Limit -	-20	-20	-20	-20	-20	nA
		Limit +	20	20	20	20	20	nA
Switch Input Off Leakage with Supply Voltage Open		Avg (Biased)	0.27	0.17	0.30	0.25	0.42	nA
		Avg (Unbiased)	0.27	0.35	0.44	0.25	0.42	nA
		Limit -	-20	-20	-20	-20	-20	nA
		Limit +	20	20	20	20	20	nA
Switch On Input Leakage with Overvoltage Applied to the Input		Avg (Biased)	4.12	4.12	4.11	4.10	4.10	µA
		Avg (Unbiased)	4.11	4.12	4.11	4.10	4.10	µA
		Limit -	2.75	2.75	2.75	2.75	2.75	µA
		Limit +	5.50	5.50	5.50	5.50	5.50	µA

Table 2. ISL71030M Response of Key Parameters vs TID (Continued)

Parameter	Condition	Bias	Pre-Rad Value	10krad(Si)	20krad(Si)	30krad(Si)	Post Anneal	Units
Switch Output OFF Leakage		Avg (Biased)	0.08	0.03	0.16	0.07	0.06	nA
		Avg (Unbiased)	0.07	0.03	0.16	0.07	0.06	nA
		Limit -	-30	-30	-30	-30	-30	nA
		Limit +	30	30	30	30	30	nA
Switch Output Leakage with Switch Enabled		Avg (Biased)	0.32	0.28	0.33	0.31	0.28	nA
		Avg (Unbiased)	0.32	0.29	0.32	0.31	0.28	nA
		Limit -	-30	-30	-30	-30	-30	nA
		Limit +	30	30	30	30	30	nA
Logic Input LOW Voltage		Avg (Biased)	1.49	1.49	1.49	1.49	1.49	V
		Avg (Unbiased)	1.49	1.49	1.48	1.49	1.49	V
		Limit -	1.3	1.3	1.3	1.3	1.3	V
		Limit +	1.6	1.6	1.6	1.6	1.6	V
Logic Input HIGH Voltage		Avg (Biased)	1.52	1.51	1.51	1.51	1.51	V
		Avg (Unbiased)	1.51	1.51	1.51	1.51	1.51	V
		Limit -	1.3	1.3	1.3	1.3	1.3	V
		Limit +	1.6	1.6	1.6	1.6	1.6	V
Logic Input LOW Current	ADDR	Avg (Biased)	0.0012	0.0017	-0.0008	-0.0006	-0.0003	µA
		Avg (Unbiased)	0.0010	0.0016	-0.0009	-0.0006	-0.0003	µA
	EN	Avg (Biased)	0.0017	0.0015	0.0014	0.0015	0.0013	µA
		Avg (Unbiased)	0.0020	0.0015	0.0012	0.0015	0.0013	µA
		Limit -	-	-	-	-	-	µA
		Limit +	0.10	0.10	0.10	0.10	0.10	µA
Logic Input HIGH Current	ADDR	Avg (Biased)	0.01	0.01	0.01	0.01	0.01	µA
		Avg (Unbiased)	0.01	0.01	0.01	0.01	0.01	µA
	EN	Avg (Biased)	0.01	0.01	0.01	0.01	0.01	µA
		Avg (Unbiased)	0.01	0.01	0.01	0.01	0.01	µA
		Limit -	-	-	-	-	-	µA
		Limit +	0.10	0.10	0.10	0.10	0.10	µA
Quiescent Supply Current	3.6V	Avg (Biased)	0.033	0.041	0.024	0.014	0.014	µA
		Avg (Unbiased)	0.034	0.041	0.023	0.014	0.014	µA
	5.5V	Avg (Biased)	0.037	0.046	0.030	0.021	0.021	µA
		Avg (Unbiased)	0.039	0.046	0.028	0.021	0.021	µA
		Limit -	-	-	-	-	-	µA
		Limit +	0.3	0.3	0.3	0.3	0.3	µA

Table 2. ISL71030M Response of Key Parameters vs TID (Continued)

Parameter	Condition	Bias	Pre-Rad Value	10krad(Si)	20krad(Si)	30krad(Si)	Post Anneal	Units
VREF Supply Current	3.6V	Avg (Biased)	0.055	0.052	0.052	0.053	0.053	µA
		Avg (Unbiased)	0.054	0.052	0.052	0.053	0.053	µA
	5.5V	Avg (Biased)	0.058	0.055	0.055	0.055	0.054	µA
		Avg (Unbiased)	0.057	0.055	0.055	0.055	0.054	µA
		Limit -	-	-	-	-	-	µA
		Limit +	0.2	0.2	0.2	0.2	0.2	µA
Addressing Transition Time	3.0V	Avg (Biased)	38.13	38.13	38.13	38.25	38.13	ns
		Avg (Unbiased)	38.00	38.00	38.00	38.25	38.13	ns
	4.5V	Avg (Biased)	59.88	59.88	59.88	59.75	59.88	ns
		Avg (Unbiased)	59.63	59.75	59.75	59.75	59.88	ns
		Limit -	10	10	10	10	10	ns
		3.0V Limit +	100	100	100	100	100	ns
		4.5V Limit +	70	70	70	70	70	ns
Break-Before-Make Delay	3.0V	Avg (Biased)	32.13	32.13	32.38	32.88	32.25	ns
		Avg (Unbiased)	32.63	32.75	32.63	32.88	32.25	ns
	4.5V	Avg (Biased)	22.00	22.13	22.13	22.25	22.00	ns
		Avg (Unbiased)	22.13	22.13	22.13	22.25	22.00	ns
		Limit -	5	5	5	5	5	ns
		3.0V Limit +	50	50	50	50	50	ns
		4.5V Limit +	40	40	40	40	40	ns
Enable Turn-On Time	3.0V	Avg (Biased)	33.13	33.38	33.63	33.38	33.38	ns
		Avg (Unbiased)	32.63	32.63	32.75	33.38	33.38	ns
	4.5V	Avg (Biased)	24.00	24.00	24.00	24.00	24.00	ns
		Avg (Unbiased)	24.00	24.00	24.00	24.00	24.00	ns
		Limit -	-	-	-	-	-	ns
		3.0V Limit +	50	50	50	50	50	ns
		4.5V Limit +	40	40	40	40	40	ns
Enable Turn-Off Time	3.0V	Avg (Biased)	37.75	37.63	37.38	36.63	37.63	ns
		Avg (Unbiased)	37.50	37.50	37.13	36.63	37.63	ns
	4.5V	Avg (Biased)	29.75	29.75	29.63	29.00	29.63	ns
		Avg (Unbiased)	29.50	29.50	29.25	29.00	29.63	ns
		Limit -	-	-	-	-	-	ns
		3.0V Limit +	50	50	50	50	50	ns
		4.5V Limit +	40	40	40	40	40	ns

6.2 Single-Event Effects Testing

The intense heavy ion environment encountered in space applications can cause a variety of Single-Event Effects (SEE). SEE can lead to system-level performance issues including disruption, degradation, and destruction. For predictable and reliable space system operation, individual electronic components should be characterized to determine their SEE response. The following is a summary of the ISL71030M SEE testing.

6.2.1 SEE Test Facility

Testing was performed at the Texas A&M University (TAMU) Cyclotron Institute heavy ion facility on April 3, 2019. The overall test setup includes the test jig containing four evaluation boards mounted and wired through a 20ft cable to the data room. The end of the 20ft cable in the data room was connected to a switchboard. The switchboard was wired to the power supplies and monitoring equipment/scopes.

6.2.2 SEE Test Setups

Testing the ISL71030M parts for damaging SEE (Single Event Burnout (SEB) and Single Event Latch-Up (SEL)) had the parts configured to select input 13 by applying the test voltage, VTEST, to address lines A2 and A3 and GND to A0, A1, and EN-bar. This connected IN-13 to the output. The output was loaded with a 10kΩ resistor to GND, and the input (IN-13) had a 10kΩ resistor to the test voltage, VTEST. This created a resistor divider that put the output, OUT, at half of VTEST. The test voltage, VTEST, was also applied to the supply, V+, and to the inputs 9 to 16, excluding 13. The inputs 1 to 8 had GND applied to them. The parts tested for damaging SEE were heated with a thin-film heater on the back of the PCB to attain a case temperature of 125°C.

Single Event Transients (SET) were tested with VTEST at 3.00V and 5.50V, the extremes of the suggested operating range. For SET the parts were not heated and therefore were at the ambient of about 25°C. The definition of a SET was a ±20mV movement of OUT from its nominal value of half VTEST. As with the SEB testing, the part was configured to select input 13. However, unlike the SEB testing, the addressing was done with applied voltages of 70% VREF on A2 and A3, and 30% VREF applied to A0, A1, and EN-bar. This was done to place the addressing at low noise margin states as VREF was set to 3.00V. OUT had a 10kΩ resistor to GND and IN 13 was supplied with VTEST through a 10kΩ resistor to again set OUT to half of VTEST.

6.2.3 Single Event Burnout and Latch-Up (SEB/L) Results

The test voltage, VTEST, was sequentially set to 6.50V, 6.75V, and 7.00V for three independent irradiations on four parts. Before and after each irradiation the total current to V+ and VREF was measured along with the output voltage, OUT. No deviations greater than 3% were registered for the currents, and no deviation of even 1% was seen on OUT. The conclusion was that no permanent damage resulted from the irradiations as done.

6.2.4 SET Results

No SET were captured with the ±20mV criterion in the most recent testing. This result is inconsistent with previous testing on a similar part. In the earlier testing, the ±20mV SET corresponded to cross sections of 419µm^2 at VTEST = 3.0V and 2020µm^2 at VTEST = 5.5V. However, the nature of the SET captures was that a spike transient triggered the capture at ±20mV but the low frequency motion on the OUT node without the spike was less than ±20mV. Examples are presented below from the previous testing. Thus, the captures previously were dependent on the high-frequency coupling. A slight change in this could have dropped the SET below the trigger point for the newer testing. Because there are no SET to examine for the newer testing, this is all supposition. However, the older testing still represents a worst case estimate of the ISL71030M SET behavior. The previous testing did provide evidence that the ±20mV SET vanished at an LET of 20MeV·cm^2/mg. This should also apply to the ISL71030M.

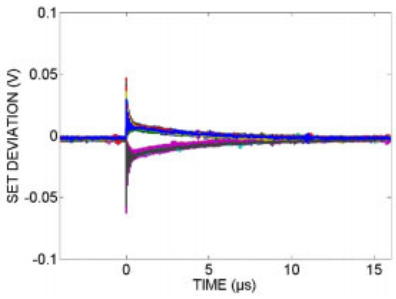


Figure 39. Composite Plot of 20 Largest and Longest SET for Both Positive and Negative Deviations Seen on Previous Testing, DUT 1-4 at LET = 43MeV·cm^2/mg and V+ = 5.5V.

6.2.5 Conclusion

The ISL71030M 5V MUX is immune to damaging SEE when operated at 125°C and V+ voltages up to 7V while being irradiated with normal incidence silver for a surface LET of 43MeV·cm^2/mg. The maximum cross section for damaging events under these conditions is 2.5µm^2 (zero events on four units to 1x10^{7}ions/cm^2).

SET on the ISL71030M for ±20mV on OUT fall somewhere between 2020µm^2 and zero depending on the testing cited. Those SET that were captured were marginal to the ±20mV criterion. The ±20mV SET disappeared completely at 20MeV·cm^2/mg.

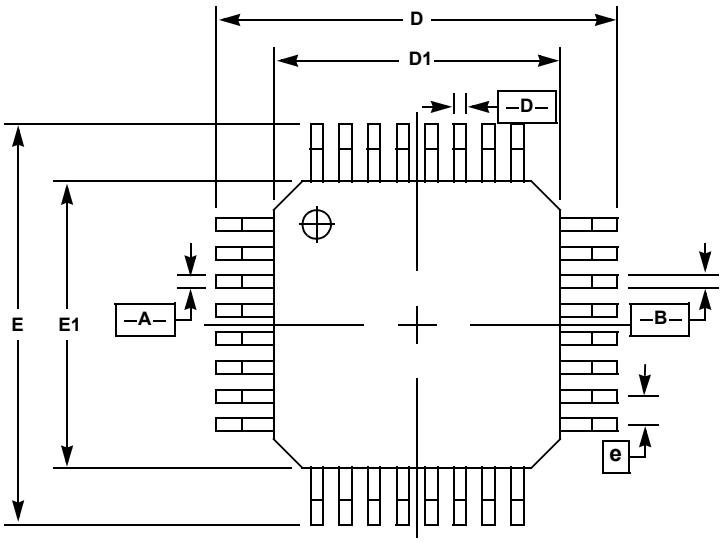
7. Revision History

Rev.	Date	Description
1.01	Apr 12, 2021	Added two features bullets: • Passes NASA low outgassing specifications • NiPdAu lead finish (Pb-free, Sn-free)
1.00	Jul 10, 2019	Initial Release

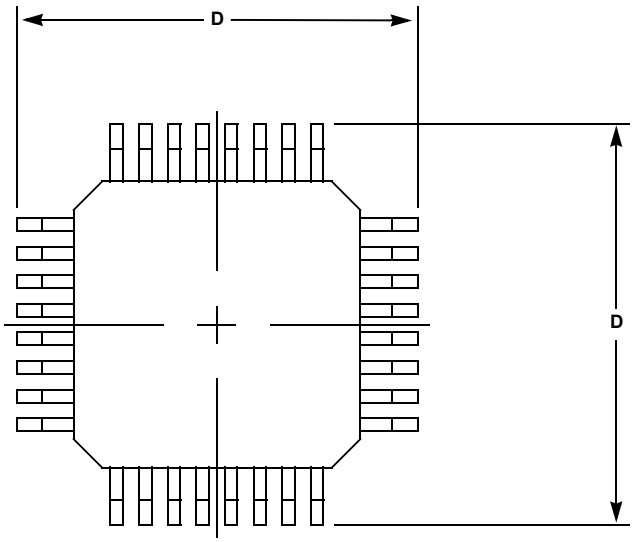
8. Package Outline Drawing

For the most recent package outline drawing, see Q32.5x5A.

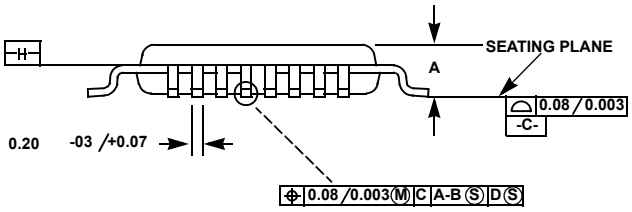
Q32.5X5A
32 Lead Thin Plastic Quad Flatpack Package (TQFP)
Rev 1, 10/11



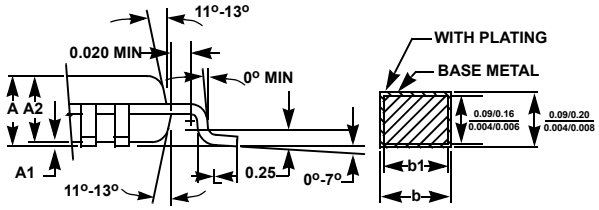
TOP VIEW



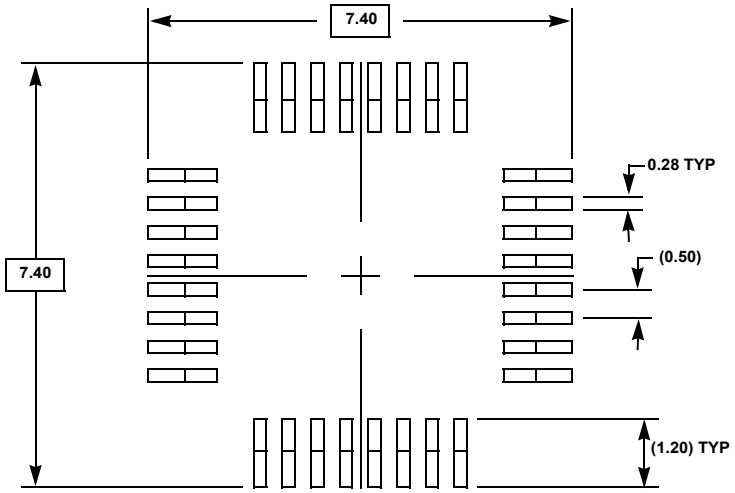
BOTTOM VIEW



SIDE VIEW



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

SCALE NONE

SYMBOL	MIN	MAX	NOTES
A	-	1.13	-
A1	0.039	0.089	-
A2	0.95	1.05	-
b	0.17	0.27	6
b1	0.17	-0.23	-
D	7 BSC		-
E	7 BSC		-
D1	5 BSC		-
E1	5 BSC		-
e	0.5 BSC		-
L	0.45	0.75	-
N	32		6

NOTES:

1. Controlling Dimension; Millimeter, converted inch dimensions are not necessarily exact.
2. All dimensioning and tolerancing conform to ANSI Y14.5-1982.
3. Dimensions D and E to be determined at seating plane -C-
4. Dimensions D1 and E1 to be determined at datum plane -H-
5. Dimensions D1 and E1 do not include mold protusion. Allowable protusion is 0.25mm (0.010 inch) per side.
6. Dimension b does not include dambar protusion. Allowable dambar protusion shall not cause the lead width to exceed the maximum b dimensions by more than 0.08mm (0.0003 inch).
7. “N” is the number of terminal position.

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