VCC Power Off, Brownout, and Power On with the DataFlash® Family

RENESAS

VCC power off, brownout, and power on

Introduction

The AT45DBxxxE serial-interface DataFlash memories have simple requirements on the VCC power supply to guarantee normal operation. The VCC supply needs to be below VPOR MIN in order to reset the device and above VPOR MAX to operate correctly.

If the VCC supply drops below VPOR MAX but above VPOR MIN during a brownout condition, then the device may not reset a previous operation.

Product Details

- **AT45DB021E VPOR MIN is 1.10V, VPOR MAX is 1.60V**
- **AT45DB041E VPOR MIN is 1.10V, VPOR MAX is 1.60V**
- **AT45DB081E VPOR MIN is 1.10V, VPOR MAX is 1.60V**
- **AT45DB161E VPOR MIN is 1.5V, VPOR MAX is 2.2V**
- **AT45DB321E VPOR MIN is 1.5V, VPOR MAX is 2.2V**
- **AT45DB641E VPOR MIN is 1.10V, VPOR MAX is 1.60V**

VCC Conditions

Power off

The AT45DBxxxE DataFlash memories are not sensitive to the power off ramp rate. Once the VCC voltage drops below the minimum operating voltage (see individual data sheets for the operating voltage), then normal operation will cease to work correctly.

Brownout

Care must be taken to avoid a VCC drop below the VPOR MAX or minimum operating voltage (see individual data sheets for the operating voltage).

As system complexity continues to increase, voltage regulation is becoming more important. The supply voltage regulator needs to be able to supply the peak current requirement of all of the devices connected. An under specified regulator can cause current starvation. Besides increasing system noise, current starvation during programming or erasing can lead to improper operation and possible data corruption.

Power on

When power is first applied to the device, the device will default to SPI mode 3. In addition, the output pin (SO) will be in a high impedance state, and a high-to-low transition

on the CS pin will be required to start a valid instruction. The SPI mode (Mode 3 or Mode 0) will be automatically selected on every falling edge of CS by sampling the inactive clock state.

Bringing the CS pin high will guarantee an idle state, which will put the output pin (SO) in high impedance and draw very low VCC current.

During power-on, the device must not be accessed for at least the minimum tVCSL time (see data sheet for specific timing) after the VCC voltage reaches the minimum operating VCC level. While the device is being powered-on, the internal Power-On Reset (POR) circuitry keeps the device in a reset mode until the supply voltage rises above the POR maximum threshold (VPOR MAX). During this time, all operations are disabled and the device will not respond to any commands. After power-on, the device will be in the standby mode.

If the first operation to the device after power-on will be a program or erase operation, then the operation cannot be started until the supply voltage reaches the minimum VCC level and an internal delay of tPUW (see data sheet for specific timing) has elapsed.