

General Description

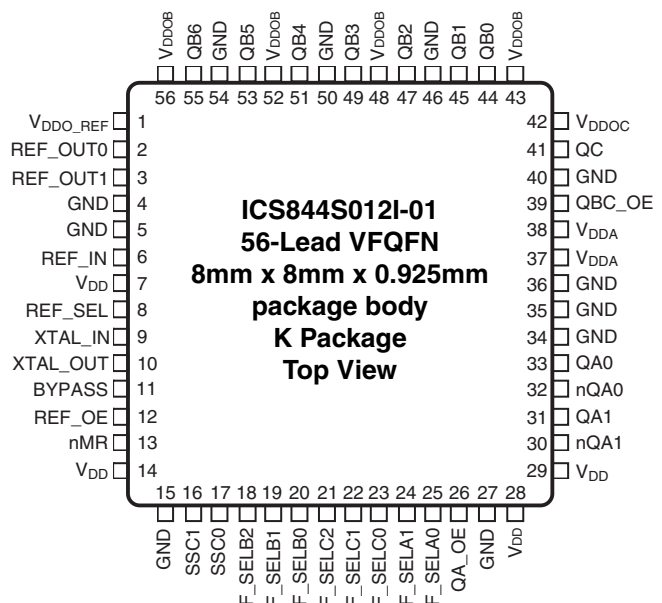
The 844S012I-01 is an optimized PCIe, sRIO and Gigabit Ethernet Frequency Synthesizer. The 844S012I-01 uses a 25MHz parallel resonant crystal to generate 33.33MHz - 200MHz clock signals, replacing solutions requiring multiple oscillator and fanout buffer solution. The device supports $\pm 0.25\%$ center-spread, and -0.6% down-spread clocking with two spread select pins (SSC[1:0]). The VCO operates at frequency of 2GHz. The device has three output banks: Bank A with two LVDS outputs, 100MHz – 250MHz; Bank B with seven 33.33MHz – 200MHz LVCMOS/ LVTTTL outputs; and Bank C with one 33.33MHz – 200MHz LVCMOS/LVTTTL output.

All Banks A, B and C have their own dedicated frequency select pins and can be independently set for the frequencies mentioned above. The low jitter characteristic of the 844S012I-01 makes it an ideal clock source for PCIe, sRIO and Gigabit Ethernet applications. Designed for networking and industrial applications, the 844S012I-01 can also drive the high-speed clock inputs of communication processors, DSPs, switches and bridges.

Features

- Two differential LVDS outputs (Bank A), configurable for PCIe (100MHz or 250MHz) and sRIO (100MHz or 125MHz) clock signals
- Eight LVCMOS/LVTTTL outputs (Bank B/C), 18 Ω typical output impedance
- Two REF_OUT LVCMOS/LVTTTL clock outputs 23 Ω typical output impedance
- Selectable crystal oscillator interface, 25MHz, 18pF parallel resonant crystal or one LVCMOS/LVTTTL single-ended reference clock input
- Supports the following output frequencies:
LVDS Bank A: 100MHz, 125MHz, 200MHz and 250MHz
LVCMOS/LVTTTL Bank B/C: 33.33MHz, 50MHz, 66.67MHz, 100MHz, 125MHz, 133.33MHz, 166.67MHz and 200MHz
- VCO: 2GHz
- Spread spectrum clock: $\pm 0.25\%$ center-spread, and -0.6% down-spread
- PLL bypass and output enable
- RMS period jitter: 23ps (maximum), QB outputs
- Full 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Available in a lead-free (RoHS 6) compliant package

Pin Assignment



Block Diagram

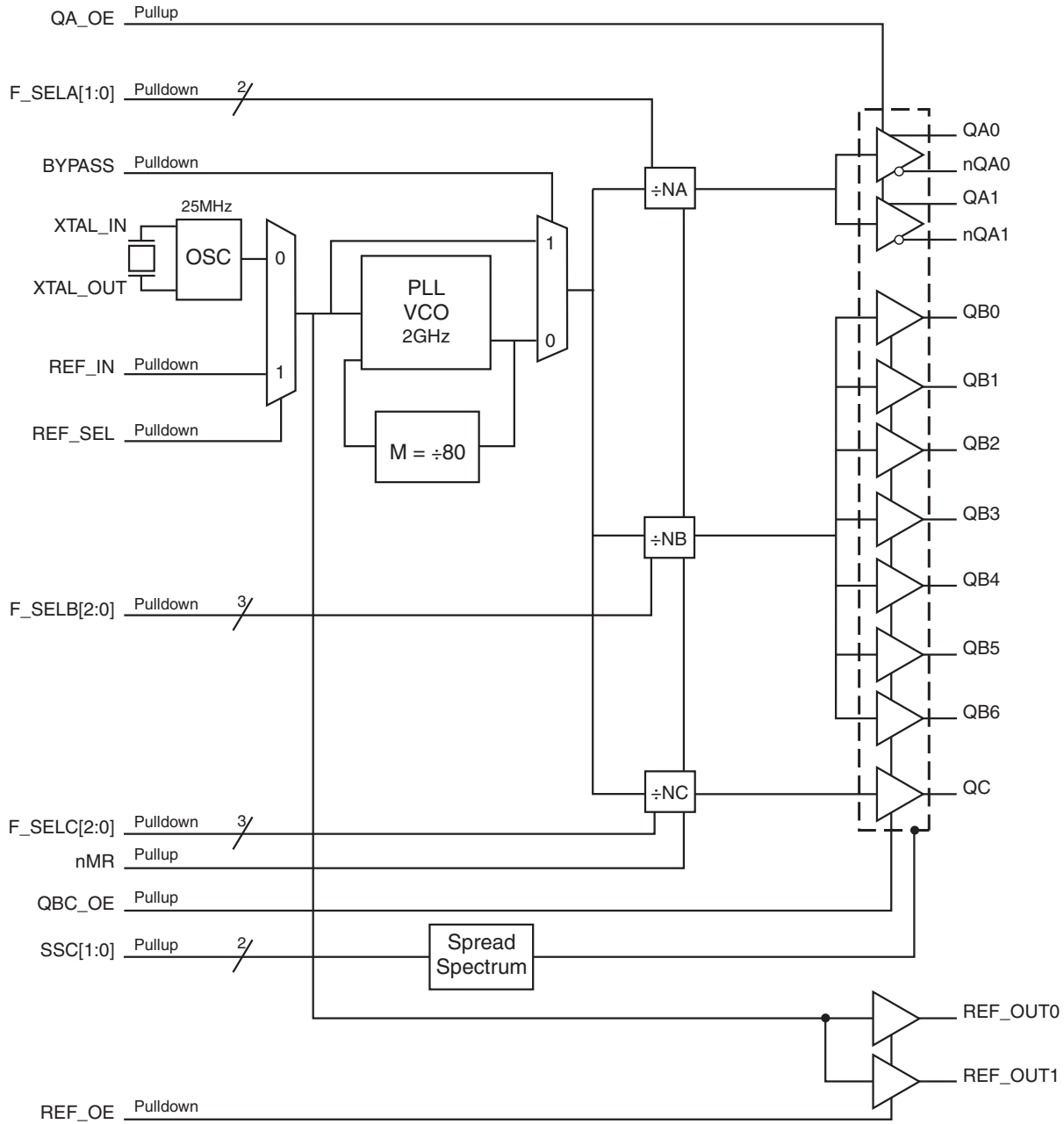


Table 1. Pin Descriptions

Number	Name	Type		Description
1	V _{DDO_REF}	Power		Output supply pin for REF_OUT outputs.
2, 3	REF_OUT0, REF_OUT1	Output		Single-ended reference clock outputs. 23Ω typical output impedance. LVCMOS/LVTTL interface levels.
4, 5, 15, 27, 34, 35, 36, 40, 46, 50, 54	GND	Power		Power supply ground.
6	REF_IN	Input	Pulldown	Single-ended reference clock input. LVCMOS/LVTTL interface levels.
7, 14, 28, 29	V _{DD}	Power		Core supply pins.
8	REF_SEL	Input	Pulldown	Reference select pin. When HIGH selects REF_IN. When LOW, selects crystal. See Table 3E. LVCMOS/LVTTL interface levels.
9, 10	XTAL_IN XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
11	BYPASS	Input	Pulldown	PLL bypass. When HIGH, bypasses PLL. When LOW, selects PLL. See Table 3J. LVCMOS/LVTTL interface levels..
12	REF_OE	Input	Pulldown	Active HIGH REF_OUT enable/disable pin. See Table 3F. LVCMOS/LVTTL interface levels.
13	nMR	Input	Pullup	Active LOW Master Reset. When logic LOW, the internal dividers are reset. When logic HIGH, the internal dividers are enabled. This device requires a reset signal after powerup. See Table 3G. LVCMOS/LVTTL interface levels.
16, 17	SSC1, SSC0	Input	Pullup	SSC control pins. See Table 3D. LVCMOS/LVTTL interface levels.
18, 19, 20	F_SELB2, F_SELB1, F_SELB0	Input	Pulldown	Frequency select pins for QBx outputs. See Table 3B. LVCMOS/LVTTL interface levels.
21, 22, 23	F_SEL2, F_SEL1, F_SEL0	Input	Pulldown	Frequency select pins for QC output. See Table 3C. LVCMOS/LVTTL interface levels.
24, 25	F_SELA1, F_SELA0	Input	Pulldown	Frequency select pins for QAx, nQAx outputs. See Table 3A. LVCMOS/LVTTL interface levels.
26	QA_OE	Input	Pullup	Output enable pin for Bank A outputs. See Table 3H. LVCMOS/LVTTL interface levels.
30, 31 32, 33	nQA1, QA1 nQA0, QA0	Output		Differential Bank A clock output pairs. LVDS interface levels.
37, 38	V _{DDA}	Power		Analog supply pins.
39	QBC_OE	Input	Pullup	Output enable pin for Bank B and Bank C outputs. See Table 3I. LVCMOS/LVTTL interface levels.
41	QC	Output		Single-ended Bank C clock output. LVCMOS/LVTTL interface levels. 18Ω typical output impedance.
42	V _{DDOC}	Power		Output supply pin for QC LVCMOS output.
43, 48, 52, 56	V _{DDOB}	Power		Output supply pins for QBx LVCMOS outputs.
44, 45, 47, 49, 51, 53, 55	QB0, QB1, QB2, QB3, QB4, QB5, QB6	Output		Single-ended Bank B clock outputs. LVCMOS/LVTTL interface levels. 18Ω typical output impedance.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance				2		pF
C _{PD}	Power Dissipation Capacitance	QB[0:6], QC	V _{DD} = V _{DDOB} , V _{DDOC} = V _{DDO_REF} = 3.465V		19		pF
R _{PULLUP}	Input Pullup Resistor				51		kΩ
R _{PULLDOWN}	Input Pulldown Resistor				51		kΩ
R _{OUT}	Output Impedance	QB[0:6], QC	V _{DDOB} , V _{DDOC} = 3.3V		18		Ω
		REF_OUT[0:1]	V _{DDO_REF} = 3.3V		23		Ω

Function Tables

Table 3A. F_SEL A[1:0] Frequency Select Function Table

Inputs				Output Frequency (25MHz Reference)
F_SEL A1	F_SEL A0	M Divider Value	NA Divider Value	QA[0:1], nQA[0:1] – (MHz)
0	0	80	20	100 (default)
0	1	80	16	125
1	0	80	10	200
1	1	80	8	250

Table 3B. F_SEL B[2:0] Frequency Select Function Table

Inputs					Output Frequency (25MHz Reference)
F_SEL B2	F_SEL B1	F_SEL B0	M Divider Value	NB Divider Value	QB[0:6] – (MHz)
0	0	0	80	60	33.33 (default)
0	0	1	80	40	50
0	1	0	80	30	66.67
0	1	1	80	20	100
1	0	0	80	16	125
1	0	1	80	15	133.33
1	1	0	80	12	166.67
1	1	1	80	10	200

Table 3C. F_SEL[2:0] Frequency Select Function Table

Inputs					Output Frequency (25MHz Reference)
F_SEL2	F_SEL1	F_SEL0	M Divider Value	NC Divider Value	QC – (MHz)
0	0	0	80	60	33.33 (default)
0	0	1	80	40	50
0	1	0	80	30	66.67
0	1	1	80	20	100
1	0	0	80	16	125
1	0	1	80	15	133.33
1	1	0	80	12	166.67
1	1	1	80	10	200

Table 3D. SSC_SEL[1:0] Function Table

Inputs		Mode
SSC1	SSC0	
0	0	0 to -0.6% Down-spread
0	1	±0.25% Center-spread
1	0	±0.25% Center-spread
1	1	SSC Off (default)

Table 3E. REF_SEL Function Table

Input	
REF_SEL	Input Reference
0 (default)	XTAL
1	REF_IN

Table 3F. REF_OE Function Table

Input	
REF_OE	Function
0 (default)	REF_OUT[0:1] - Disabled (High-Impedance)
1	REF_OUT[0:1] - Enabled

Table 3G. nMR Function Table

Input	
nMR	Function
0	Device reset, output divider - Disabled
1 (default)	Output - Enabled

NOTE: This device requires a reset signal after power-up to function properly.

Table 3H. QA_OE Function Table

Input	
QA_OE	Function
0	QA[0:1], nQA[0:1] - Disabled (High-Impedance)
1 (default)	QA[0:1], nQA[0:1] - Enabled

Table 3I. QBC_OE Function Table

Input	
QBC_OE	Function
0	QB[0:6] and QC - Disabled (High-Impedance)
1 (default)	QB[0:6] and QC - Enabled

Table 3J. BYPASS Function Table

Input	
BYPASS	Function
0 (default)	PLL
1	Bypass (reference ÷N)

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I XTAL_IN Other Inputs	0V to V_{DD} -0.5V to $V_{DDOx} + 0.5V$
Outputs, V_O (LVCMOS)	-0.5V to $V_{DDOx} + 0.5V$
Outputs, I_O (LVDS) Continuous Current Surge Current	10mA 15mA
Package Thermal Impedance, θ_{JA}	31.4°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDOx} = V_{DDOC} = V_{DDO_REF} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		$V_{DD} - 0.20$	3.3	V_{DD}	V
V_{DDOx}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				275	mA
I_{DDA}	Analog Supply Current				20	mA
I_{DDOx}	Output Supply Current				2	mA

NOTE: V_{DDOx} denotes V_{DDOx} , V_{DDOC} and V_{DDO_REF} .

NOTE: I_{DDOx} denotes I_{DDOx} , I_{DDOC} and I_{DDO_REF} .

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDOB} = V_{DDOC} = V_{DDO_REF} = 3.3V \pm 5\%$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2.2		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	nMR, SSC[1:0], QA_OE, QBC_OE	$V_{DD} = V_{IN} = 3.465V$		10	μA
		REF_IN, REF_SEL, BYPASS, REF_OE, F_SELA[1:0], F_SELB[2:0], F_SELC[2:0]	$V_{DD} = V_{IN} = 3.465V$		150	μA
I_{IL}	Input Low Current	nMR, SSC[1:0], QA_OE, QBC_OE	$V_{DD} = 3.465V, V_{IN} = 0V$	-150		μA
		REF_IN, REF_SEL, BYPASS, REF_OE, F_SELA[1:0], F_SELB[2:0], F_SELC[2:0]	$V_{DD} = 3.465V, V_{IN} = 0V$	-10		μA
V_{OH}	Output High Voltage	QBx, QC, REF_OUTx	$V_{DDOB}, V_{DDOC}, V_{DDO_REF} = I_{OH} = -2mA$	2.6		V
V_{OL}	Output Low Voltage	QBx, QC, REF_OUTx	$V_{DDOB}, V_{DDOC}, V_{DDO_REF} = I_{OH} = 2mA$		0.5	V

Table 4C. LVDS DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247		454	V
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.125		1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

AC Electrical Characteristics

Table 6. AC Characteristics, $V_{DD} = V_{DDOB} = V_{DDOC} = V_{DDO_REF} = T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units	
f_{OUT}	Output Frequency	QA[0:1], nQA[0:1]	100		250	MHz	
		QB[0:6]	33.33		200	MHz	
		QC	33.33		200	MHz	
$tsk(b)$	Bank Skew NOTE 1, 2	QB[0:6]			50	ps	
		QA[0:1], nQA[0:1]	LVCMOS Outputs off		10	ps	
$tsk(o)$	Output Skew; NOTE 2, 3	Across Banks B and C at Same Frequency			130	ps	
$t_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 2	QA[0:1], nQA[0:1]	All Outputs at the Same Frequency, REF_OE = 0		35	ps	
		QB[0:6]	All Outputs at the Same Frequency, REF_OE = 0		50	ps	
		QC	All Outputs at the Same Frequency, REF_OE = 0		60	ps	
$t_{jit(per)}$	RMS Period Jitter	QA[0:1], nQA[0:1]	All Outputs at the Same Frequency, REF_OE = 0		6	ps	
		QB[0:6], QC	QBx, QC = 33.33MHz, QAx, nQAx = 100MHz, REF_OE = 0		23	ps	
			All Outputs at the same Frequency REF_OE = 0		11	ps	
F_M	SSC Modulation Frequency	QA[0:1], nQA[0:1] QB[0:6], QC	29		33.33	kHz	
t_L	PLL Lock Time				100	ms	
t_R / t_F	Output Rise/Fall Time	QB[0:6], QC	20% to 80%	0.4	1.3	ns	
		QA[0:1], nQA[0:1]	20% to 80%	65	250	ps	
odc	Output Duty Cycle	QA[0:1], nQA[0:1]	LVCMOS Outputs OFF		48	52	%
		QB[0:6], QC	Output Frequency \leq 66.67MHz		48	52	%
		QB[0:6], QC	Output Frequency $>$ 66.67MHz		45	55	%

NOTE: QBx, QC LVCMOS outputs are characterized up to 125MHz.

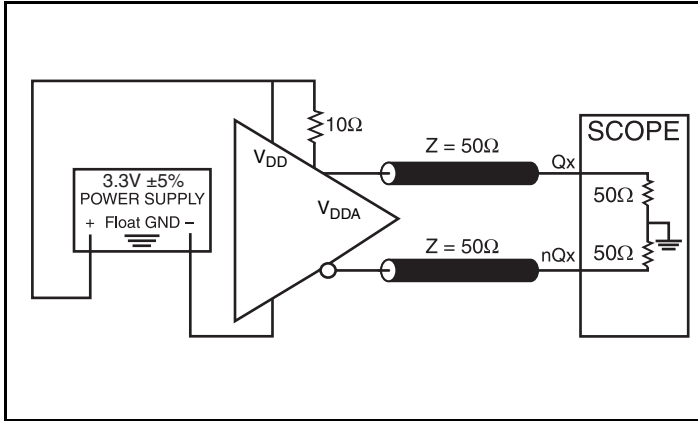
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.

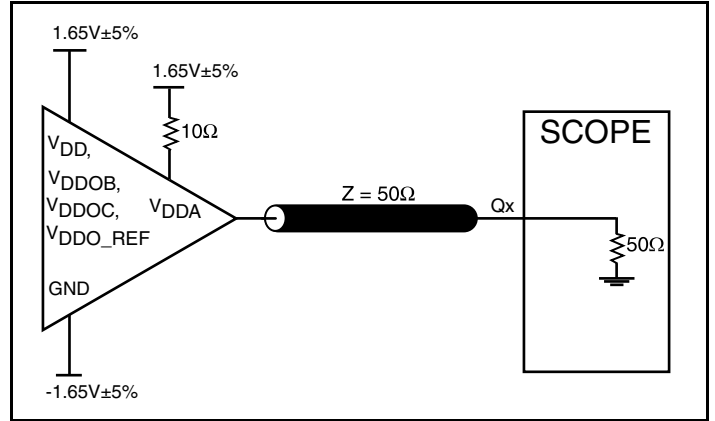
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOB}/2$.

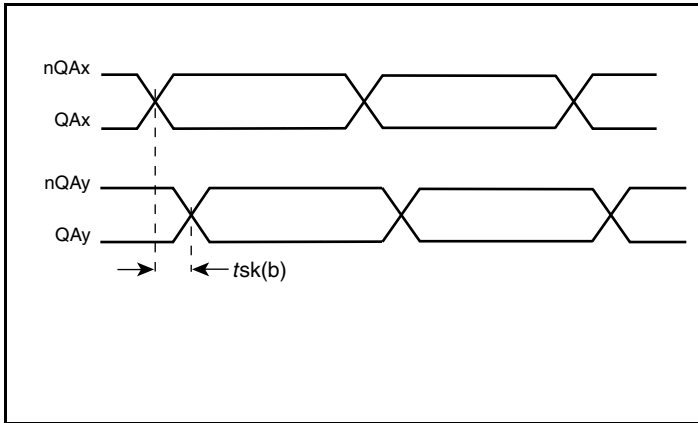
Parameter Measurement Information



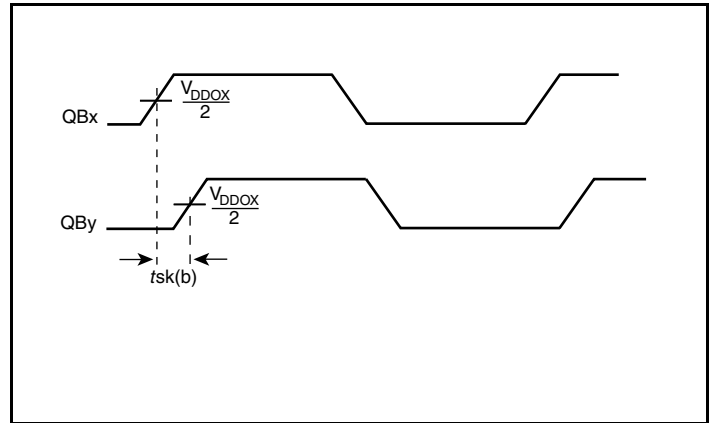
3.3V LVDS Output Load AC Test Circuit



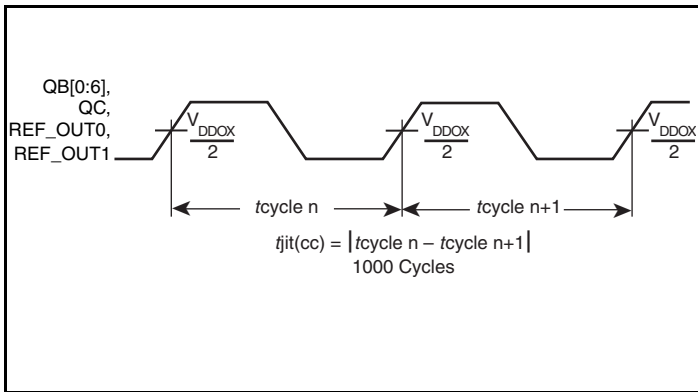
3.3V LVC MOS Output Load AC Test Circuit



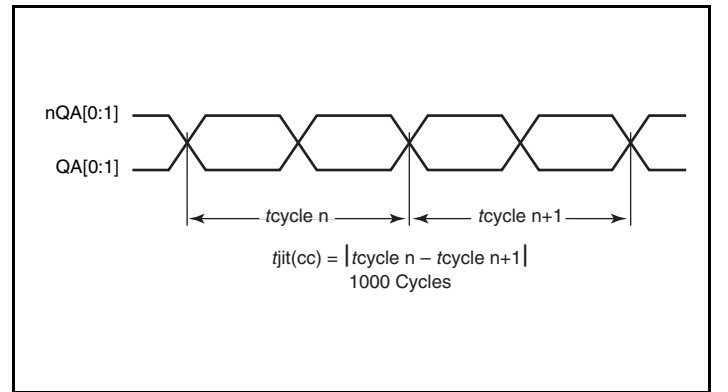
LVDS Bank Skew



LVC MOS Bank Skew

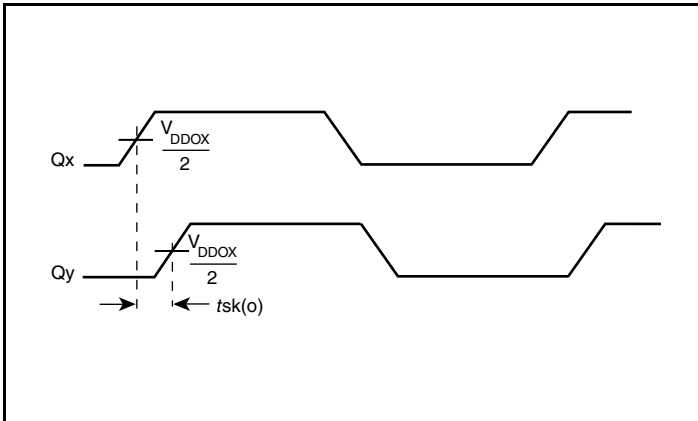


LVC MOS Cycle-to-Cycle Jitter

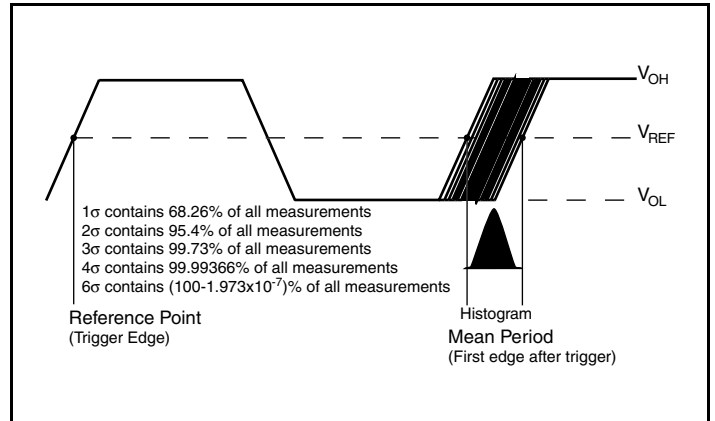


LVDS Cycle-to-Cycle Jitter

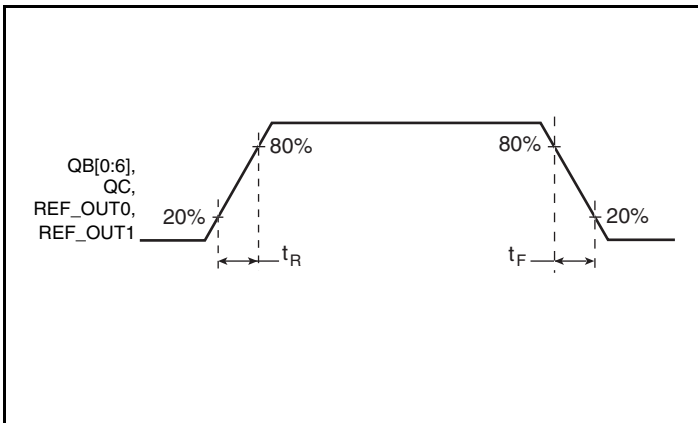
Parameter Measurement Information, continued



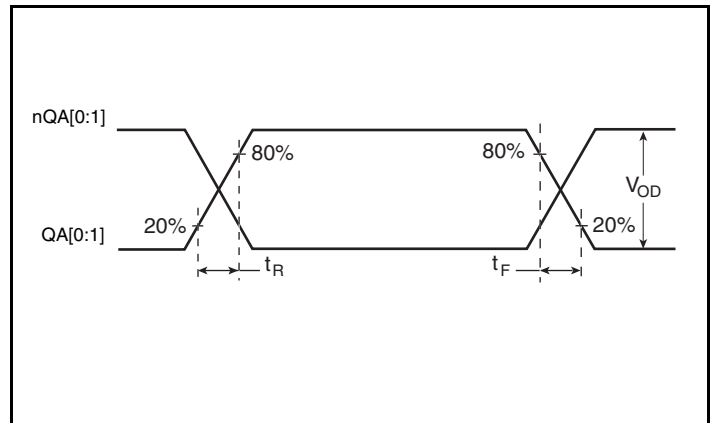
LVCMOS Output Skew



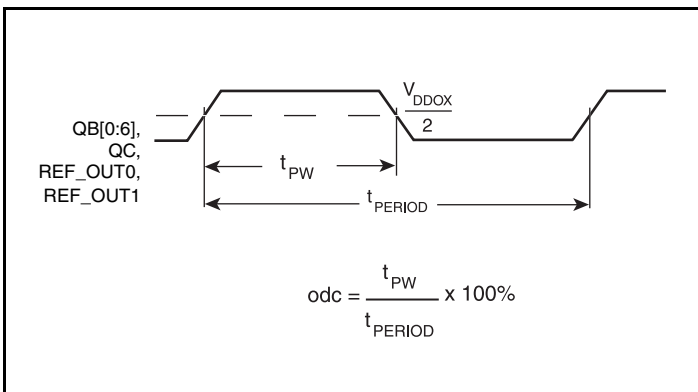
RMS Period Jitter



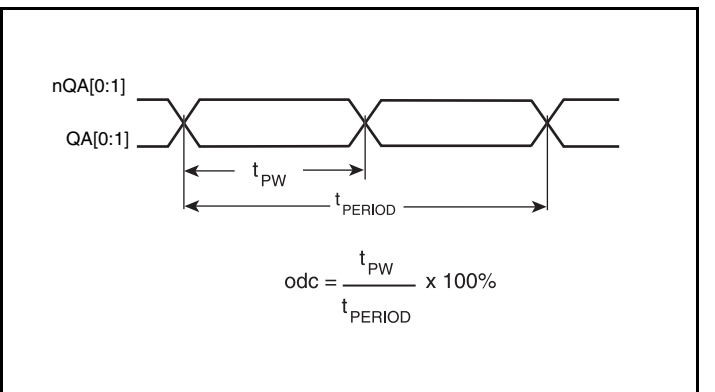
LVCMOS Rise/Fall Time



LVDS Output Rise/Fall Time

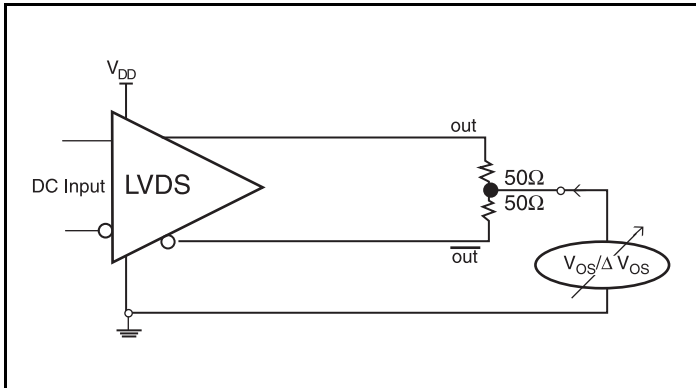


LVCMOS Output Duty Cycle/Pulse Width/Period

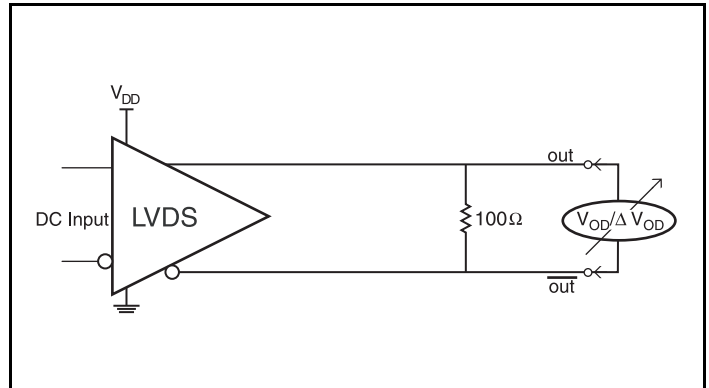


LVDS Output Duty Cycle/Pulse Width/Period

Parameter Measurement Information, continued



Offset Voltage Setup



Differential Output Voltage Setup

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

LVC MOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_IN Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_IN to ground.

Outputs:

LVC MOS Outputs

All unused LVC MOS output can be left floating. We recommend that there is no trace attached.

LVDS Outputs

All unused LVDS outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 844S0121-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} , V_{DDA} , V_{DDOB} and V_{DDO} should be individually connected to the power supply plane through vias, and $0.01\mu\text{F}$ bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a $10\mu\text{F}$ bypass capacitor be connected to the V_{DDA} pin.

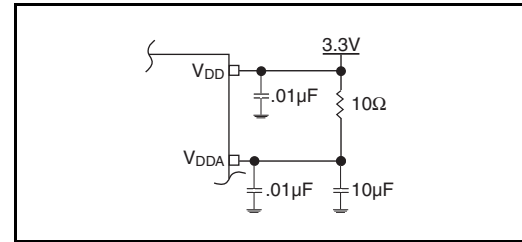


Figure 1. Power Supply Filtering

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 2*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

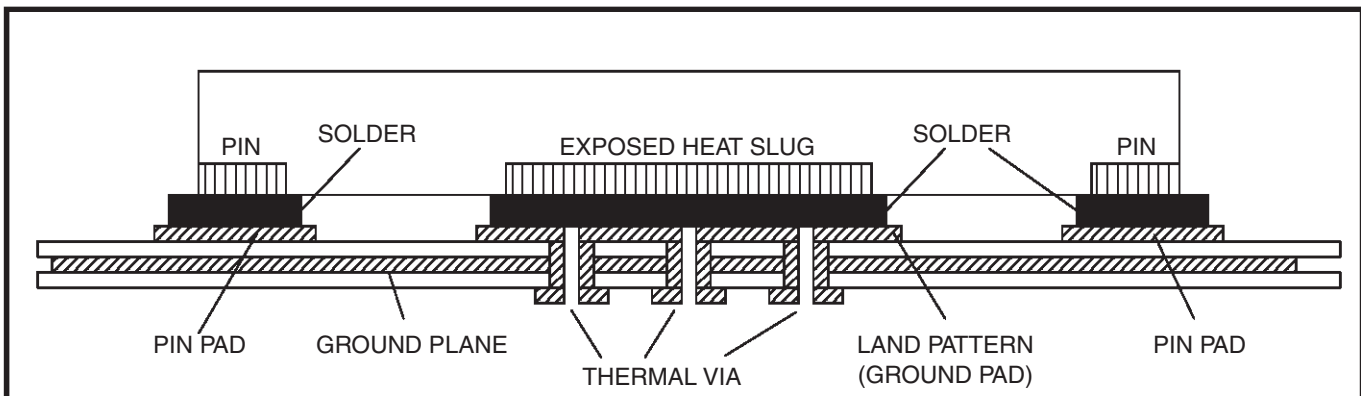


Figure 2. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Crystal Input Interface

The 844S012I-01 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 3* below

were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

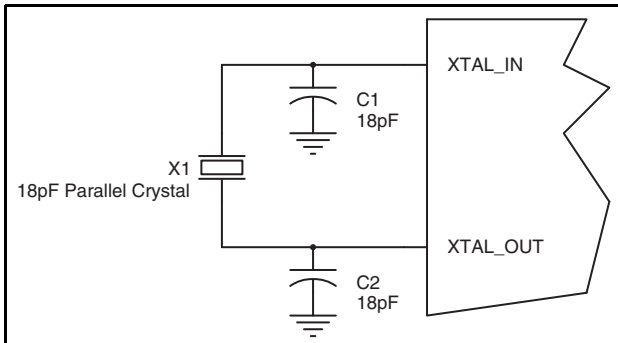


Figure 3. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 4A*. The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (R_o) plus the series resistance (R_s) equals the transmission line impedance. In addition,

matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

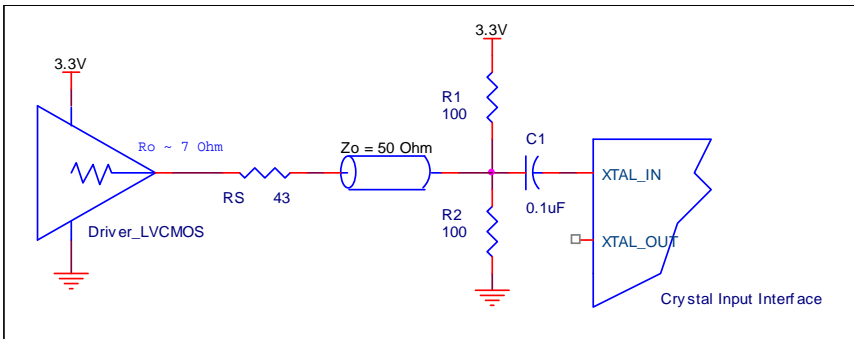


Figure 4A. General Diagram for LVCMOS Driver to XTAL Input Interface

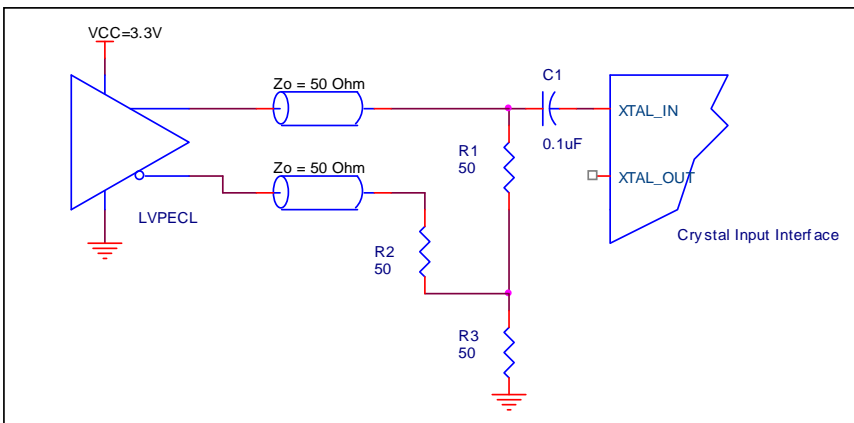


Figure 4B. General Diagram for LVPECL Driver to XTAL Input Interface

LVDS Driver Termination

A general LVDS interface is shown in *Figure 4*. Standard termination for LVDS type output structure requires both a 100Ω parallel resistor at the receiver and a 100Ω differential transmission line environment. In order to avoid any transmission line reflection issues, the 100Ω resistor must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard

termination schematic as shown in *Figure 4* can be used with either type of output structure. If using a non-standard termination, it is recommended to contact IDT and confirm if the output is a current source or a voltage source type structure. In addition, since these outputs are LVDS compatible, the input receivers amplitude and common mode input range should be verified for compatibility with the output.

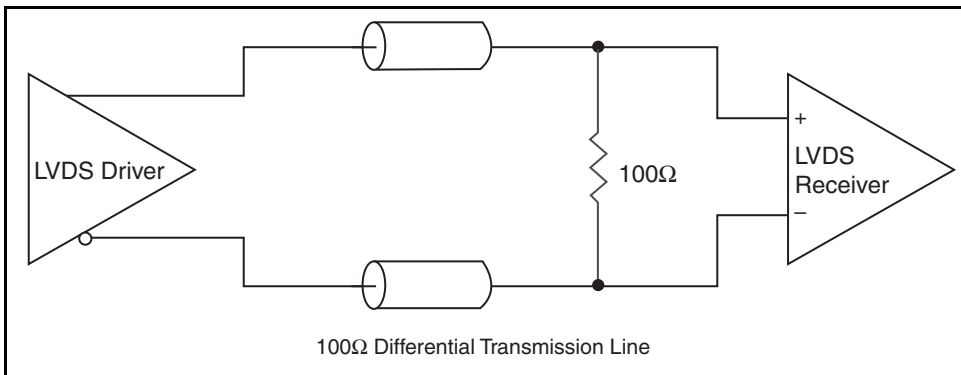


Figure 4. Typical LVDS Driver Termination

Schematic Example

Figure 6 shows an example of 844S012I-01 application schematic. In this example, the device is operated at $V_{DD} = V_{DDOB} = V_{DDOC} = V_{DDO_REF} = 3.3V$. The 18pF parallel resonant 25MHz crystal is used. The C1 and C2 = 18pF and are recommended for frequency accuracy. For different board layouts, the C1 and C2 may be slightly

adjusted for optimizing frequency accuracy. Two examples of LVDS terminations and one example of an LVC MOS termination are shown in this schematic. The decoupling capacitors should be located as close as possible to the power pin.

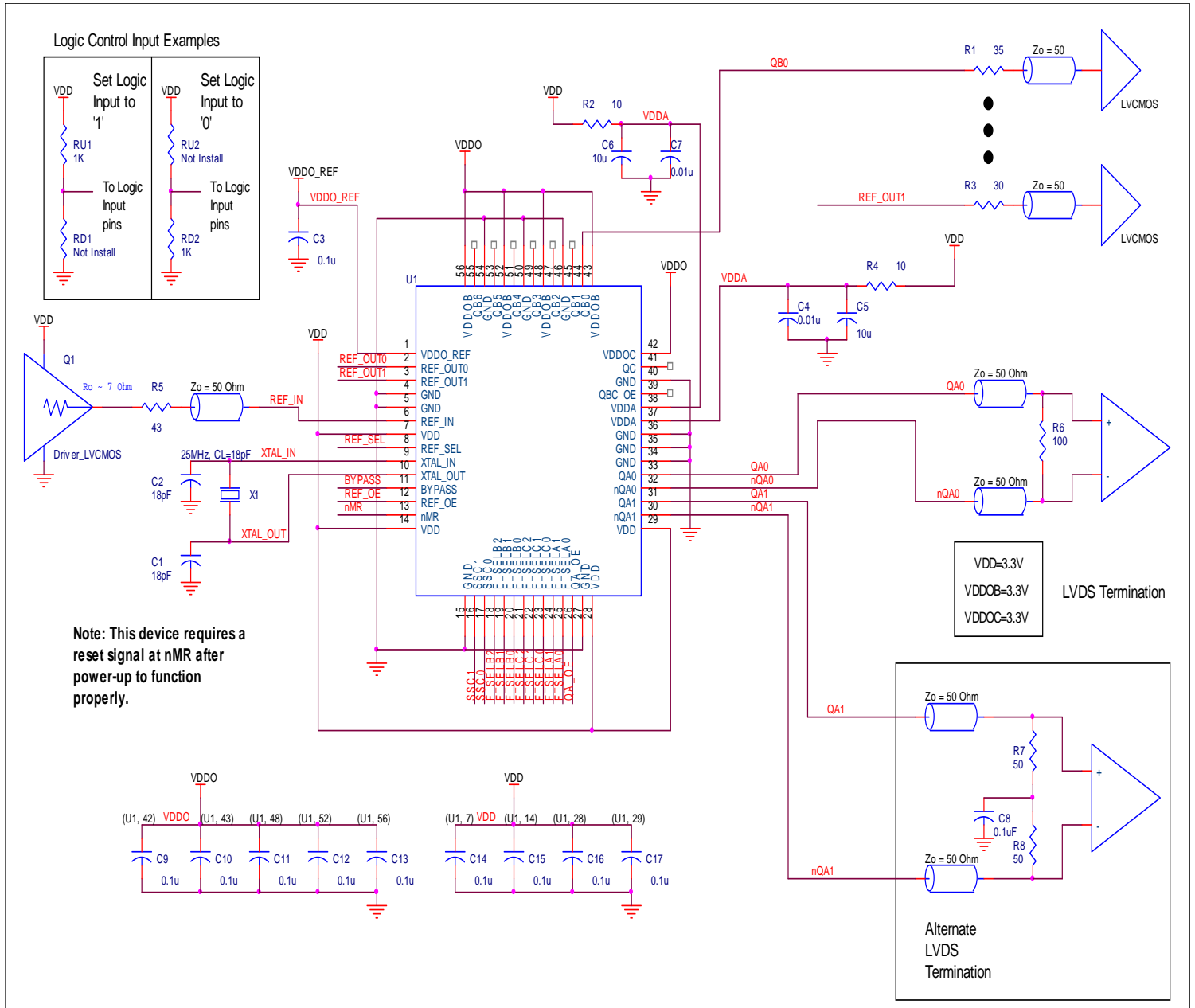


Figure 6. 844S012I-01 Schematic Example

Spread Spectrum

Spread-spectrum clocking is a frequency modulation technique for EMI reduction. When spread-spectrum is enabled, a 32kHz triangle waveform is used with 0.6% down-spread (+0.0% / -0.6%) from the nominal output frequency. An example of a triangle frequency modulation profile is shown in *Figure 7A* below. The ramp profile can be expressed as:

€ F_{nom} = Nominal Clock Frequency in Spread Off mode

€ F_m = Nominal Modulation Frequency (30kHz)

€ δ = Modulation Factor (0.6% down spread)

$$(1 - \delta)F_{nom} + 2F_m \times \delta \times F_{nom} \times t \text{ when } 0 < t < \frac{1}{2F_m},$$

$$(1 - \delta)F_{nom} - 2F_m \times \delta \times F_{nom} \times t \text{ when } \frac{1}{2F_m} < t < \frac{1}{F_m}$$

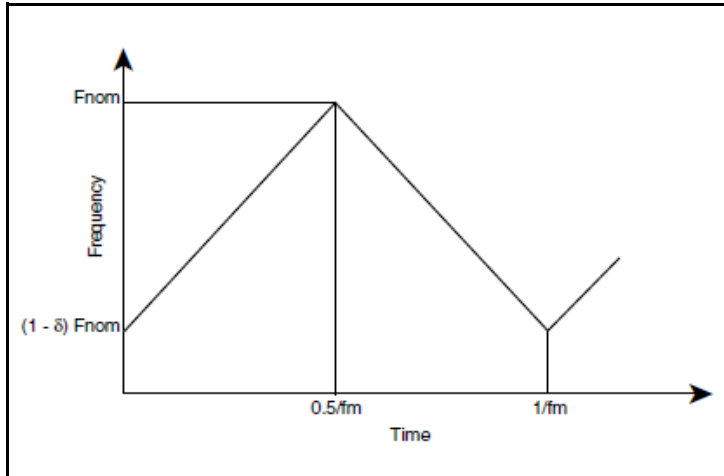


Figure 7A. Triangle Frequency Modulation

The 844S012I-01 triangle modulation frequency deviation will not exceed 0.7% down-spread from the nominal clock frequency (+0.0% / -0.6%). An example of the amount of down spread relative to the nominal clock frequency can be seen in the frequency domain, as shown in *Figure 7B*. The ratio of this width to the fundamental frequency is typically 0.4%, and will not exceed 0.7%. The resulting spectral reduction will be greater than 5dB, as shown in *Figure 7B*. It is important to note the 844S012I-01 5dB minimum spectral reduction is the component-specific EMI reduction, and will not necessarily be the same as the system EMI reduction.

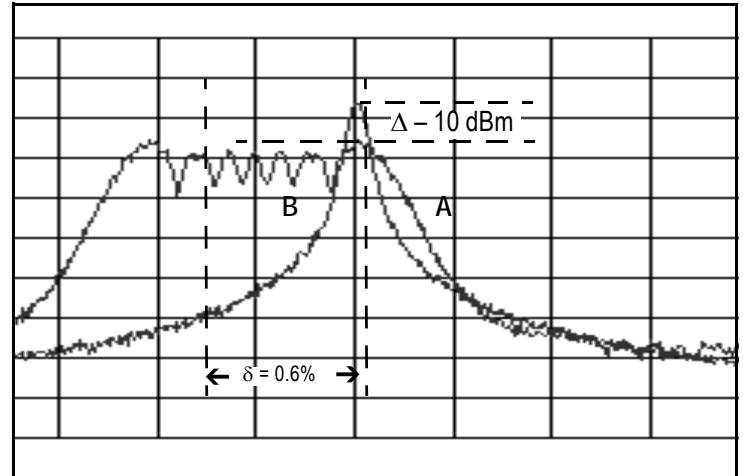


Figure 7B. 200MHz Clock Output In Frequency Domain
 (A) Spread-Spectrum OFF
 (B) Spread-Spectrum ON

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS44S012I. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS44S012I is the sum of the core power plus the power dissipation in the load(s). The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

The maximum current at 85° is as follows:

$$I_{DD_MAX} = 260mA$$

$$I_{DDA_MAX} = 18mA$$

$$I_{DDO_MAX} = 2mA$$

Core and LVDS Output Power Dissipation

- Power (core, LVDS) = $V_{DD_MAX} * (I_{DD} + I_{DDA} + I_{DDO}) = 3.465V * (260mA + 18mA + 2mA) = 970.20mW$

LVC MOS Output Power Dissipation

- Dynamic Power Dissipation at 200MHz, (QB, QC)
 $Power (200MHz) = C_{PD} * Frequency * (V_{DDO})^2 = 19pF * 200MHz * (3.465V)^2 = 45mW \text{ per output}$
Total Power (200MHz) = 45mW * 8 = 360mW
- Dynamic Power Dissipation at 25MHz
 $Power (25MHz) = C_{PD} * Frequency * (V_{DDO})^2 = 19pF * 25MHz * (3.465V)^2 = 5.6mW \text{ per output}$
Total Power (25MHz) = 5.6mW * 2 = 11.2mW

Total Power Dissipation

- Total Power**
 $= Power (core, LVDS) + Total Power (200MHz) + Total Power (25MHz)$
 $= 970.20mW + 360mW + 11.2mW$
 $= 1,341.4mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_j , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_{total} + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_{total} = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 27.5°C/W per Table 7 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 1.341\text{W} * 27.5^\circ\text{C/W} = 121.9^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 56 Lead VFQFN, Forced Convection

Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	31.4°C/W	27.5°C/W	24.6°C/W

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 56 Lead VFQFN

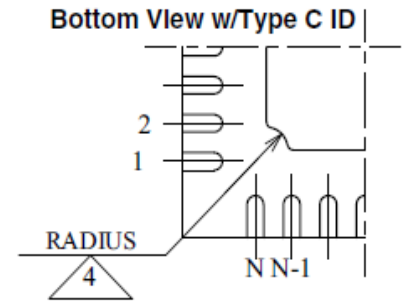
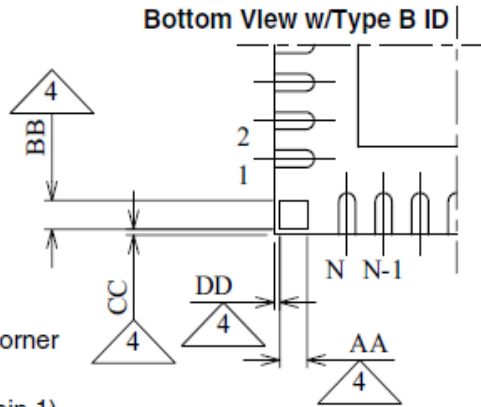
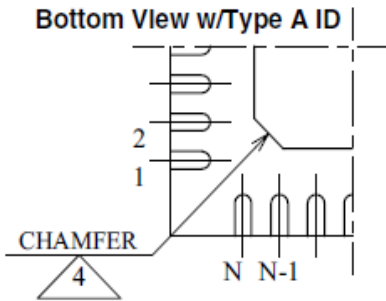
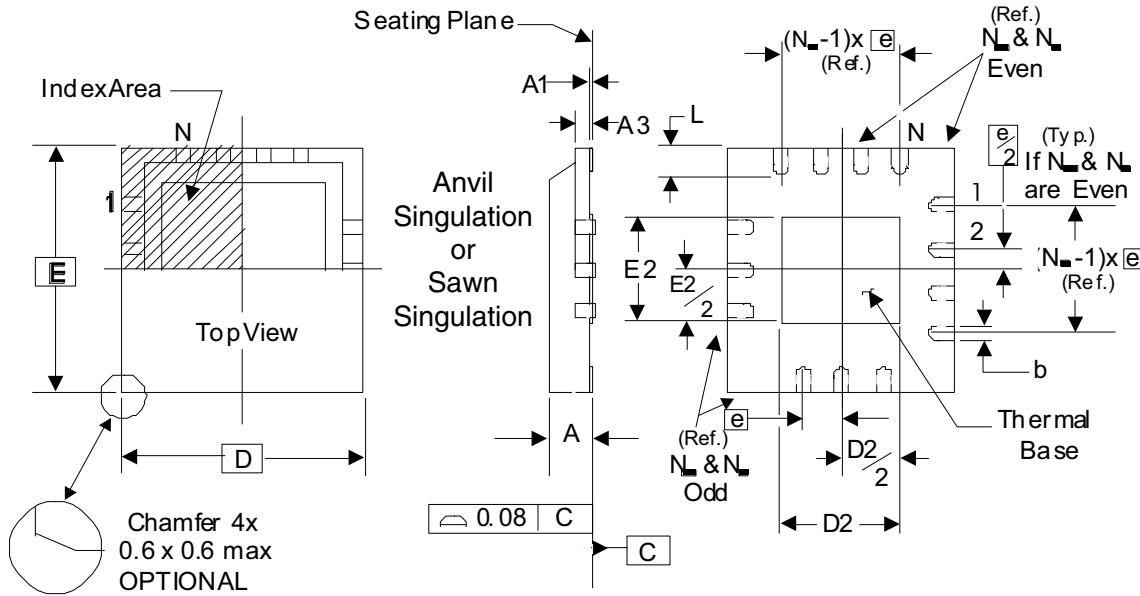
θ_{JA} vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	31.4°C/W	27.5°C/W	24.6°C/W

Transistor Count

The transistor count for 844S012I-01 is: 11,509

Package Outline and Package Dimensions

Package Outline - K Suffix for 56 Lead VFQFN



There are 3 methods of indicating pin 1 corner at the back of the VFQFN package are:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type B: Dummy pad between pin 1 and N.
3. Type C: Mouse bite on the paddle (near pin 1)

Table 9. Package Dimensions

SPEC NON JEDEC: VLLD-2/-5 All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	56	
A	0.80	1.00
A1	0	0.05
A3	0.25 Ref.	
b	0.18	0.30
N_D & N_E	14	
D & E	8.00 Basic	
D2	4.35	4.65
E2	5.05	5.35
e	0.50 Basic	
L	0.30	0.50

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 9.

Reference Document: JEDEC Publication 95, MO-220

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844S012BKI-01LF	ICS4S012BI01L	"Lead-Free" 56 Lead VFQFN	Tray	-40°C to +85°C
844S012BKI-01LFT	ICS4S012BI01L	"Lead-Free" 56 Lead VFQFN	Tape & Reel	-40°C to +85°C

Revision History

Revision Date	Description of Change
January 5, 2016	<ul style="list-style-type: none">▪ General Description - removed the ICS chip.▪ Removed ICS from the part number.▪ Ordering Information - removed 1000 from Tape and Reel and the LF note below the table.▪ Updated the header and footer.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.