64-bit RISC-V Microprocessor Delivers New Options for IoT Edge Development

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Introduction

Global and rapidly expanding IoT edge devices are becoming increasingly important for connecting various sensors to the cloud via networks. IoT edge devices are progressively integrating 64-bit microprocessors capable of running Linux and similar high-performance operating systems. Moreover, recent import and export regulation changes have produced a need for choices in CPU architecture for microprocessors to generate a stable supply of IoT devices. The RZ/Five boasts multiple features which help resolve these issues.

Expanded, High-performance CPU Options

As a microprocessor equipped with a 64-bit RISC-V CPU, the RZ/Five offers customers expanded CPU options as well as superior CPU performance within its class.

Uses RISC-V Open-source ISA

The RISC-V CPU is open-source architecture, greatly differentiating it from other CPUs, which utilize proprietary architectures. As the CPU architecture technology is open source, geopolitical, proprietary, and non-neutral risks are minimized, rendering it suitable for long-term microprocessor supply.

Built Around RISC-V ISA-compatible Andes AX45MP

Renesas adopted the IP from a founding member of RISC-V International, Andes Technology, which enabled swifter provision of a RISC-V ISA-compatible general-purpose microprocessors to the marketplace. This allowed for an early release of RZ/Five with an embedded RISC-V ISA-compliant 64-bit RISC-V CPU.

Excellent CPU performance within its class

The AX45MP has superior CPU performance within its class and is expected to offer a performance measuring approximately 1.3 times that of the Arm® Cortex®-A53.

Reducing Obstacles to RISC-V Adoption

A scalable development environment that enables mutual migration from Arm to RISC-V and RISC-V to Arm broadens CPU choices while improving product development efficiency. Moreover, as microprocessors RZ/Five (RISC-V) and RZ/G2UL (Arm) are pin-compatible and can use the same PCB design, customers enjoy reduced development costs and faster time to market.

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Scalable SMARC-compliant Development Environment

The evaluation kit includes a SMARC-compliant module board incorporating the RZ/Five and DDR memory, as well as a carrier board equipped with connectors for Ethernet, USB, CAN, etc. Both the RZ/Five (RISC-V) and the RZ/G2UL (Arm) can be evaluated by merely switching the module board. As each Board Support Package (CIP Linux) is provided by Renesas, customers can utilize standard APIs, allowing their efforts to focus solely on application software development.

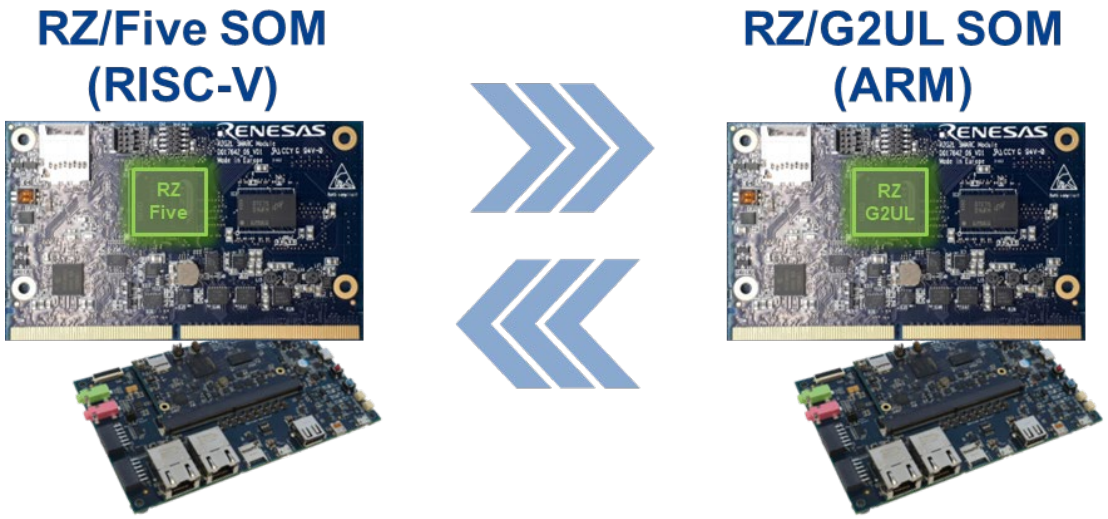


Figure 1. SMARC 2.1-compliant Development Environment

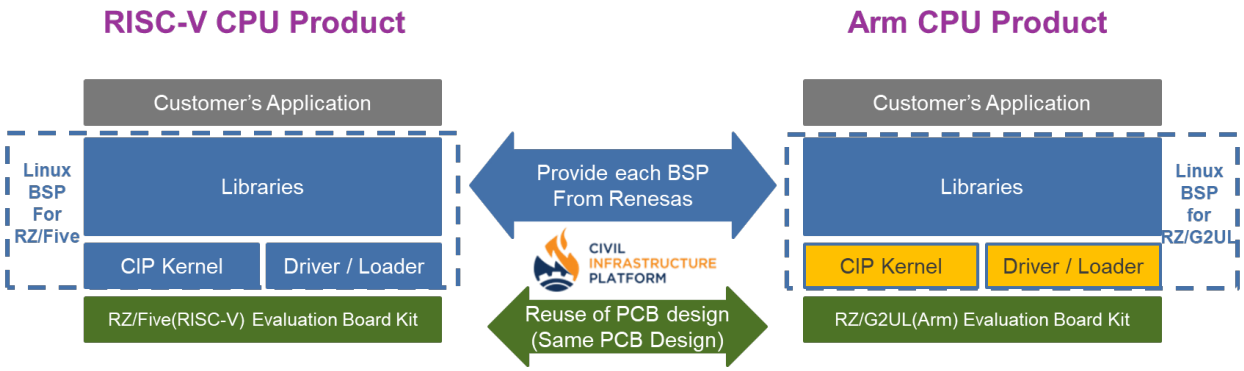


Figure 2. Linux BSP and Application Compatibility

RZ/Five (RISC-V) and RZ/G2UL (Arm) pin compatibility

Pin compatibility between the RZ/Five and RZ/G2UL lowers the hurdle in choosing a CPU architecture, reduces development time and saves costs, as the same PCB design can be used.

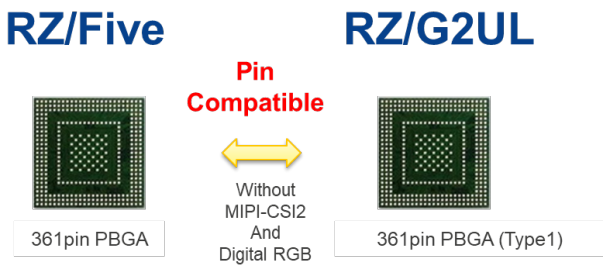


Figure 3. RZ/Five (RISC-V) and RZ/G2UL (Arm) Pin Compatibility

Specialized Features for IoT Edge Devices

RZ/Five further enhances development efficiency with features specific to IoT edge devices integrated on a single chip.

- The 1GHz CPU frequency aids sensor data collection and analysis in addition to network protocol processing.
- Standard with 2 channels of Gbit Ether and CAN-FD enables multiple network processing options.
- Two 12-bit AD converters are included for acquiring data from analog sensors.

Function	RZ/Five
CPU	AX45MP Single Core RISC-V 64-bit @1.0GHz
Internal RAM	128KB w/ECC
DRAM I/F	16-bit x1ch DDR3L (1.3Gbps)/DDR4 (1.6Gbps) w/ECC
USB	USB2.0 Host 1ch, USB2.0 Host/Function 1ch
Ether	Gbit 2ch (361 pin package), Gbit 1ch (266 pin package)
SDHI	2 x SDHI (UHS-I)/MMC
SPI	1 x SPI Multi I/O (4-bit DDR)
CAN	2x CAN-FD
Serial	4x I2C, 2x SCI, 5x UART, 3x RSPI
Timer	8x 16-bit MTU, 1x WDT
ADC	2x 12-bit ADC
Package	361 pin, 13x13mm PBGA (0.5mm Pitch) 266 pin, 11x11mm PBGA (0.5mm Pitch)

Table 1: RZ/Five Functions

Reducing System Costs

RZ/Five has numerous features to reduce system costs required for entry-level products. These include the incorporation of peripheral components, an optimized dedicated power supply, as well as the potential for a lower cost four-layer board design. As shown in figure 4.

Incorporation of two 12-bit ADCs

RZ/Five integrates two AD converters which eliminates the need for external components when acquiring data from analog sensors therefore, reducing costs.

Optimization of power supply system with dedicated PMIC

The DA9062 PMIC (Power Management IC) optimized for RZ/Five simplifies the power supply peripheral design, decreasing the number of components while alleviating design complexity leading to improved time-to-market.

Realizing four-layer PCB

A 4-layer board for RZ/Five is realized by integrating DDR4-SDRAM and standard interfaces. The DDR signal wiring of the 4-layer PCB design has been verified to satisfy JEDEC standards. Renesas additionally offers a 4-layer PCB board design which serves as a reference to shorten board design time.

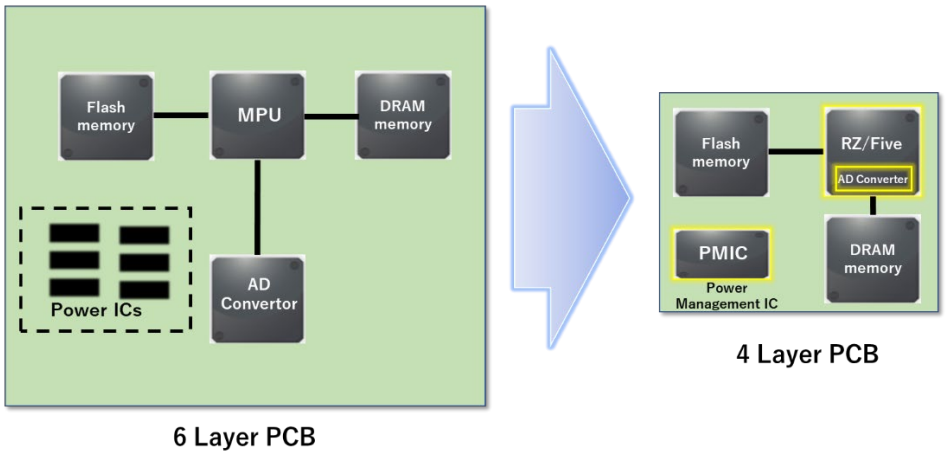


Figure 4. Reducing System Costs

CIP Linux Kernel Eases Long-Term Product Maintenance Burden

Solar inverters, secure home gateways, EV chargers, and other IoT edge devices have extremely long product development-to-release and operation periods, therefore requiring maintenance during their extensive life cycles. The CIP Linux Kernel and VLP of the RZ/G and RZ/Five help to alleviate the burden, extensive man-hours and high cost of customer performed maintenance through the following initiatives:

- Adopting Linux kernel provided by the CIP (Civil Infrastructure Platform); maintaining industrial-grade Linux for over 10 years
- Providing a VLP (Verified Linux Package) based on the CIP's Linux kernel; reducing the user's Linux maintenance man-hours

What is the Civil Infrastructure Platform (CIP)?

- The CIP is a platform providing the base layer required to build Linux-based embedded systems meeting the needs of today's civil infrastructure. It is spearheaded by The Linux Foundation and promoted by leading global infrastructure system manufacturers. Please click here for more information.

Summary

The RZ/Five is a general-purpose microprocessor based on the open-source RISC-V ISA.

RZ/Five features required by IoT edge devices also contribute to our system cost reduction for developers, including:

- Expanded options for CPU architectures and reduced risk of long-term product usage
- Scalable development environment facilitating mutual migration between RISC-V and Arm and improved development efficiency
- System cost-reduction mechanisms contributing to a lower overall development costs.

Renesas enhances product development for customers by offering a wider choice of CPU architectures as well as a scalable development environment.

References

- RZ/Five — General-purpose microprocessors with RISC-V CPU Core (Andes AX45MP Single) (1.0 GHz) with 2ch gigabit Ethernet
- RZ/Five Evaluation Board Kit — Evaluation board kit for RZ/FIVE microprocessors
- RZ/G2UL — General-purpose microprocessors with Single-core Arm® Cortex®-A55 (1.0 GHz) CPU and Single-core Arm® Cortex®-M33 (200 MHz) CPU with 2ch gigabit Ethernet

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