

[Notes]

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Rev.1.00

Nov. 01, 2022

RX Family AES/RSA/SHA Library

Firmware Integration Technology

Outline

When using any of the products below, note the following point.

RX Family AES Library Firmware Integration Technology

RX Family RSA Library Firmware Integration Technology

RX Family SHA Library Firmware Integration Technology

- Using the software in RXv3 CPU products

1. Using the Software in RXv3 CPU Products

1.1 Applicable Products

Table 1: RX AES/RSA/SHA Library FIT Module applicable products

Product name	Version	Document No.
RX Family AES Library Firmware Integration Technology	1.06	R20AN0044EJ0106
RX Family RSA Library Firmware Integration Technology	1.03	R20AN0292EJ0103
RX Family SHA Library Firmware Integration Technology	1.04	R20AN0157EJ0104

1.2 Applicable Devices

RXv3 CPU products

RX660, RX66N, RX66T, RX671, RX72M, RX72N, RX72T

1.3 Details and Condition

If RXv3 is specified for the instruction set architecture for compiler options, the following build error occurs.

```
#error "None-support combination of CPU and endian"
```

The compiler options for the instruction set architecture that cause the build error are as follows:

CCRX: -isa=rxv3

GCC: -misa=v3

IAR: --core rxv3

1.4 Workaround

Modify the information as follows in the files in which the error might occur.

- AES library
 - r_aes_version.c
 - r_gcm_version.c
- RSA library
 - r_rsa_version.c
- SHA library
 - r_sha_version.c

[Before modification]

```
#if (defined (__RXV2) && defined (__BIG))
    #define __TARGET_CPU__ "RXV2 BIG endian"
    #define __COMPILER_VER__ (__RENESAS_VERSION__)
#elif (defined (__RXV2) && defined (__LIT))
    #define __TARGET_CPU__ "RXV2 LITTLE endian"
    #define __COMPILER_VER__ (__RENESAS_VERSION__)
#elif (defined (__RXV1) && defined (__BIG))
    #define __TARGET_CPU__ "RXV1 BIG endian"
    #define __COMPILER_VER__ (__RENESAS_VERSION__)
#elif (defined (__RXV1) && defined (__LIT))
    #define __TARGET_CPU__ "RXV1 LITTLE endian"
    #define __COMPILER_VER__ (__RENESAS_VERSION__)
#elif (defined (__RX600) && defined (__BIG))
    #define __TARGET_CPU__ "RX600 BIG endian"
    #define __COMPILER_VER__ (__RENESAS_VERSION__)
#elif (defined (__RX600) && defined (__LIT))
    #define __TARGET_CPU__ "RX600 LITTLE endian"
    #define __COMPILER_VER__ (__RENESAS_VERSION__)
#elif (defined (__RX200) && defined (__BIG))
    #define __TARGET_CPU__ "RX200 BIG endian"
    #define __COMPILER_VER__ (__RENESAS_VERSION__)
#elif (defined (__RX200) && defined (__LIT))
    #define __TARGET_CPU__ "RX200 LITTLE endian"
    #define __COMPILER_VER__ (__RENESAS_VERSION__)
```

[After modification]

```
#if (defined (__RX) && defined (__BIG))
    #define __TARGET_CPU__ "RX BIG endian"
    #define __COMPILER_VER__ (__RENESAS_VERSION__)
#elif (defined (__RX) && defined (__LIT))
    #define __TARGET_CPU__ "RX LITTLE endian"
    #define __COMPILER_VER__ (__RENESAS_VERSION__)
```

1.5 Schedule for Fixing the Problem

This problem will be fixed in the next version (scheduled to be released in November 2022).

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Nov.01.22	-	First edition issued

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