

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A891A/E	Rev.	1.00
Title	Usage Notes on WDT		Information Category	Technical Notification		
Applicable Product	See below.	Lot No.	Reference Document	See below.		
		All lots				

Usage notes on the watchdog timer mode (WDT) for the products listed below are as follows.

1. WTCNT Setting Value

If the timer is stopped and WTCNT is set to H'FF in interval timer mode, an overflow does not occur when WTCNT changes from H'FF to H'00 after one cycle of the count clock, but an overflow does occur when WTCNT changes from H'FE to H'FF after 256 cycles of the count clock. If the timer is operating and WTCNT is set to H'FF, an interval timer interrupt is generated immediately.

Do not set WTCNT to H'FF in watchdog timer mode. If WTCNT is set to H'FF, a WDT reset is generated immediately regardless of the clock selected by bits CKS[2:0]. In this case, the assertion periods of the $\overline{\text{WDTOVF}}$ signal and internal reset signal are shortened.

2. Timer Variation

After timer operation has started, the period from the power-on reset point to the first count up timing of WTCNT varies depending on the time period that is set by the TME bit of WTCSR. The shortest such time period is thus one cycle of the peripheral clock, $P\phi$, while the longest is the result of frequency division according to the value in the CKS[2:0] bits. The timing of subsequent incrementation is in accord with the selected frequency division ratio. Accordingly, this time difference is referred to as timer variation.

This also applies to the timing of the first incrementation after WTCNT has been written to during timer operation.

3. System Reset by $\overline{\text{WDTOVF}}$ Signal

If the $\overline{\text{WDTOVF}}$ signal is input to the $\overline{\text{RES}}$ pin of this LSI, this LSI cannot be initialized correctly.

Avoid input of the $\overline{\text{WDTOVF}}$ signal to the $\overline{\text{RES}}$ pin of this LSI through glue logic circuits. To reset the entire system with the $\overline{\text{WDTOVF}}$ signal, use the circuit shown in figure 1.

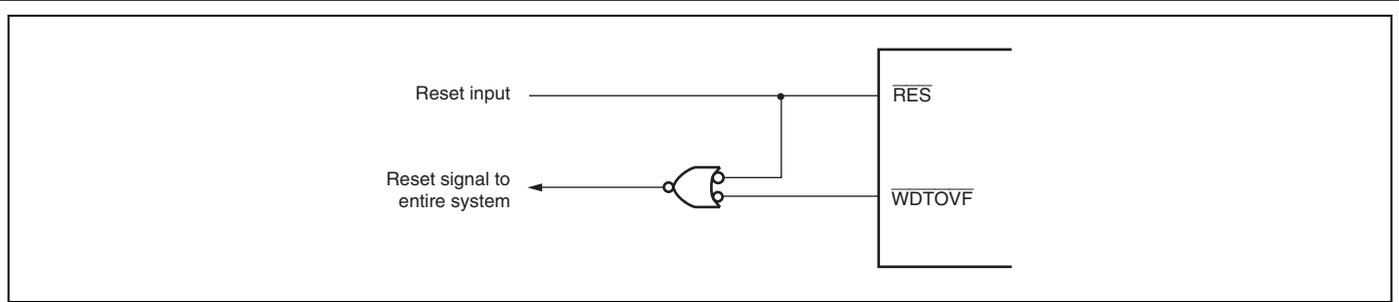


Figure 1 Example of System Reset Circuit Using WDTOVF Signal

4. Manual Reset in Watchdog Timer Mode*

When a manual reset occurs in watchdog timer mode, the current bus cycle is continued. If a manual reset occurs while the bus is released or during DMAC burst transfer, manual reset exception handling will be pended until the CPU acquires the bus mastership.

Note: * Except SH/Tiny series

[Corrections in User's Manual]

Corrections of the User's Manual are described below using the SH7080 Group User's Manual: Hardware as an example.

14.6.1 WTCNT Setting Value

[Before correction (p.726)]

If WTCNT is set to H'FF in interval timer mode, an overflow does not occur when WTCNT changes from H'FF to H'00 after one cycle of count clock, but an overflow occurs when WTCNT changes from H'FF to H'00 after 257 cycles of count clock.

If WTCNT is set to H'FF in watchdog timer mode, overflow occurs when WTCNT changes from H'FF to H'00 after one cycle of count clock.

[After correction (p.726)]

If the timer is stopped and WTCNT is set to H'FF in interval timer mode, an overflow does not occur when WTCNT changes from H'FF to H'00 after one cycle of the count clock, but an overflow does occur when WTCNT changes **from H'FE to H'FF after 256 cycles of the count clock. If the timer is operating and WTCNT is set to H'FF, an interval timer interrupt is generated immediately.**

Do not set WTCNT to H'FF in watchdog timer mode. If WTCNT is set to H'FF, a WDT reset is generated immediately, regardless of the clock selected by bits CKS[2:0]. In this case, the assertion periods of the $\overline{\text{WDTOVF}}$ signal and internal reset signal are shortened.

[Addition (p.726)]

14.6.2 Timer Variation

After timer operation has started, the period from the power-on reset point to the first count up timing of WTCNT varies depending on the time period that is set by the TME bit of WTCSR. The shortest such time period is thus one cycle of the peripheral clock, Pφ, while the longest is the result of frequency division according to the value in the CKS[2:0] bits. The timing of subsequent incrementation is in accord with the selected frequency division ratio. Accordingly, this time difference is referred to as timer variation.

This also applies to the timing of the first incrementation after WTCNT has been written to during timer operation.

[Addition (p.726)]

14.6.3 System Reset by WDTOVF Signal

If the $\overline{\text{WDTOVF}}$ signal is input to the $\overline{\text{RES}}$ pin of this LSI, this LSI cannot be initialized correctly.

Avoid input of the $\overline{\text{WDTOVF}}$ signal to the $\overline{\text{RES}}$ pin of this LSI through glue logic circuits. To reset the entire system with the $\overline{\text{WDTOVF}}$ signal, use the circuit shown in figure 14.4.

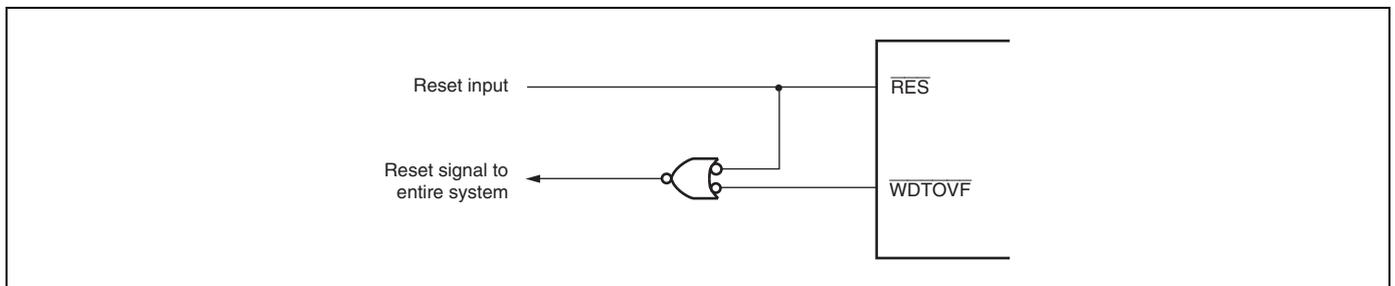


Figure 14.4 Example of System Reset Circuit Using $\overline{\text{WDTOVF}}$ Signal

[Addition (p.726)]

14.6.4 Manual Reset in Watchdog Timer Mode*

When a manual reset occurs in watchdog timer mode, the current bus cycle is continued. If a manual reset occurs while the bus is released or during DMAC burst transfer, manual reset exception handling will be pended until the CPU acquires the bus mastership.

Note: * Except SH/Tiny series

[Addition (p.726)]

14.6.5 Internal Reset in Watchdog Timer Mode

When an internal reset is generated by an overflow of the watchdog timer counter (WTCNT) in watchdog timer mode, the watchdog timer control/status register (WTCSR) is not initialized and its value is maintained.

[Applicable Products and Reference Documents]

Series	Group	Reference Document	Rev.	Ref. No.
SH7080	SH7083, SH7084, SH7085, SH7086	SH7080 Group User's Manual: Hardware	5.00	R01UH0198EJ0500
SH7137	SH7131, SH7132, SH7136, SH7137	SH7137 Group Hardware Manual	3.00	REJ09B0402-0300
SH7146	SH7146, SH7149	SH7146 Group User's Manual: Hardware	4.00	R01UH0049EJ0400
SH/Tiny	SH7124, SH7125	SH7125 Group, SH7124 Group Hardware Manual	5.00	REJ09B0243-0500

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