Date: August 22, 2014

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A890A/E	Rev.	1.00
Title	Usage Notes on WDT		Information Category	Technical Notification		
Applicable Product	See below.	Lot No. All lots	Reference Document	See below.		

Usage notes on the watchdog timer for the products listed below are as follows.

[Notes]

1. Interval Timer Overflow Flag

When the value of WTCNT is H'FF, clearing of the IOVF flag is not possible. Clear the IOVF flag after the value of WTCNT has become H'00 or after writing a value other than H'FF to WTCNT.

2. Manual Reset in Watchdog Timer Mode

When a manual reset occurs in watchdog timer mode, the current bus cycle is continued. If a manual reset occurs while the bus is released or during DMAC burst transfer, manual reset exception handling will be pended until the CPU acquires the bus mastership.

However, if the interval from generation of the manual reset until the end of the bus cycle is equal to or longer than 128 cycles of Pφ (the internal manual reset interval cycles), the internal manual reset source is ignored instead of being deferred, and manual reset exception handling is not executed.

3. Internal Reset in Watchdog Timer Mode

When an internal reset is generated by an overflow of the watchdog timer counter (WTCNT) in watchdog timer mode, the watchdog reset control/status register (WRCSR) is not initialized and the WOVF bit is set to 1. When the value of the WOVF bit is 1, no internal reset is generated when a WTCNT overflow occurs.

[Corrections in the User's Manual]

Corrections of the User's Manual are described below using the SH7211 Group Hardware Manual as an example.

14.5.4 Manual Reset in Watchdog Timer Mode

[Before correction (p.664)]

When a manual reset occurs in watchdog timer mode, the bus cycle is continued. If a manual reset occurs while the bus is released or during DMAC burst transfer, manual reset exception handling will be pended until the CPU acquires the bus mastership.

However, if the duration from generation of the manual reset to the bus cycle end is equal to or longer than the duration of the internal manual reset activated, the occurrence of the internal manual reset source is ignored instead of being pended, and the manual reset exception handling is not executed.

[After correction]

When a manual reset occurs in watchdog timer mode, the bus cycle is continued. If a manual reset occurs while the bus is released or during DMAC burst transfer, manual reset exception handling will be pended until the CPU acquires the bus mastership.

However, if the interval from generation of the manual reset until the end of the bus cycle is equal to or longer than 128 cycles of Pφ (the internal manual reset interval cycles), the internal manual reset source is ignored instead of being pended, and the manual reset exception handling is not executed.

[Addition]

14.5.5 Interval Timer Overflow Flag

When the value of WTCNT is H'FF, clearing of the IOVF flag is not possible. Clear the IOVF flag after the value of WTCNT has become H'00 or after writing a value other than H'FF to WTCNT.

[Addition]

14.5.6 Internal Reset in Watchdog Timer Mode

When an internal reset is generated by an overflow of the watchdog timer counter (WTCNT) in watchdog timer mode, the watchdog reset control/status register (WRCSR) is not initialized and the WOVF bit is set to 1. When the value of the WOVF bit is 1, no internal reset is generated when a WTCNT overflow occurs.

[Applicable Products and Reference Documents]

Series	Group	Reference Document	Rev.	Ref. No.
SH7210	SH7211	SH7211 Group Hardware Manual	3.00	REJ09B0344-0300
SH7216	SH7214, SH7216	SH7214 Group, SH7216 Group User's Manual: Hardware	4.00	R01UH0230EJ0400
SH7231	SH7231	SH7231 Group User's Manual: Hardware	2.00	R01UH0073EJ0200
SH7239	SH7237, SH7239	SH7239 Group, SH7237 Group User's Manual: Hardware	2.00	R01UH0086EJ0200
SH7243	SH7243	SH7280 Group, SH7243 Group User's Manual: Hardware	3.00	R01UH0229EJ0300
SH7280	SH7285, SH7286	SH7280 Group, SH7243 Group User's Manual: Hardware	3.00	R01UH0229EJ0300

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