To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-SH7-A702A/E	Rev.	1.00
Title	SH7211 Series: Correction of error in the Electrical Characteristics in the hardware manual		Information Category	Technical Notification		
Applicable Product	SH7211 Group	Lot No. All lots	Reference Document	SH7211 Group Hardware Manual Rev. 2.00 (REJ09B0344-0200)		

We would like to inform you of correction to an error in the SH7211 Group hardware manual, specifically to the description regarding the Section 17,19 and the Electrical Characteristics. Please take this information into consideration when using this product.

Revised Description

The description of the Section 17,19 and the Section 27 Electrical Characteristics in the SH7211 Group hardware manual Rev. 2.00 has been revised as follows.

1. Descriptions in Section 17 A/D Converter (ADC)

[Before]

- 12-bit resolution
- Input channels

  Eight channels (two independent A/D conversion modules)
- High-speed conversion

  When Aφ = 40 MHz: Minimum 1.25 μs per channel

  AD clock = 40 MHz, 50 conversion states
- Two operating modes
- Single-cycle scan mode: Continuous A/D conversion on one to eight channels
- Continuous scan mode: Repetitive A/D conversion on one to eight channels
- A/D data registers

  Eight A/D data registers (ADDR) are provided. A/D conversion results are stored in A/D data registers (ADDR) that correspond to the input channels.
- Sample-and-hold function

  A sample-and-hold circuit is built into the A/D converter of this LSI, simplifying the configuration of the external analog input circuitry. Multiple channels can be sampled simultaneously because sample-and-hold circuits can be dedicated for channels 0 to 2 and 8 to10.

  - Group A (GrA): Analog input pins selected from channels 0, 1, and 2 can be simultaneously sampled.

[After]

- 12-bit resolution
- Input channels

  Eight channels
- High-speed conversion

  When Aφ = 40 MHz: Minimum 1.25 µs per channel

  AD clock = 40 MHz, 50 conversion states
- Two operating modes
- Single-cycle scan mode: Continuous A/D conversion on one to eight channels
- Continuous scan mode: Repetitive A/D conversion on one to eight channels
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  Eight A/D data registers (ADDR) are provided. A/D conversion results are stored in A/D data registers (ADDR) that correspond to the input channels.
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  A sample-and-hold circuit is built into the A/D converter of this LSI, simplifying the configuration of the external analog input circuitry. Multiple channels can be sampled simultaneously because sample-and-hold circuits can be dedicated for channels 0 to 2.

  - Group A (GrA): Analog input pins selected from channels 0, 1, and 2 can be simultaneously sampled.

2. Description in the Section 17.7 Usage Notes

[Before]

17.7.1 Analog Input Voltage Range

The voltage applied to analog input pin (ANn) during A/D conversion should be in the range AVss ≤ ANn (n = 0 to 7) ≤ AVcc.

17.7.2 Relationship between AVcc, AVss and Vcc, Vss

When using the A/D converter, set AVcc = 5.0 V ±0.5 V and AVss = Vss. When the A/D converter is not used, set Vcc ≤ AVcc ≤ 5.0V ±0.5V, AVss = Vss, and do not leave the AVcc pin open.

17.7.3 Range of AVREF Pin Settings

Set AVREF = AVcc ±0.3 V and AVREFVss = AVss ±0.3 V. If these conditions are not met, the reliability of the LSI may be adversely affected.

[After]

17.7.1 Relationship between AVcc, AVss and VccQ, VssQ

When using the A/D converter or D/A converter, set AVcc = 5.0 V ±0.5 V and AVss = Vss.
When the A/D converter or D/A converter are not used, set AVcc=VccQ, AVss=VssQ,
and do not leave the AVcc,AVss pin open.

17.7.2 Range of AVREF Pin Settings

When using the A/D converter or D/A converter, set AVREF=4.5V～AVcc.
When the A/D converter or D/A converter are not used, set AVREF=AVcc,
and do not leave the AVREF pin open.
AVREFVss is always AVREFVss=AVss, and do not leave the AVREFVss pin open.
If these conditions are not met, the reliability of the LSI may be adversely affected.

3. Descriptions in Section 19 Pin Function Controller(PFC)

[Before]

Bit	Bit Name	Initial Value	R/W	Description
6 to 4	PB29MD[2:0]	000	R/W	PB29 Mode Select the function of the PB29/DREQ0/TIOC1B pin. 000:PB29 I/O(port) 001:Setting prohibited 010:DREQ0 input(DMAC) 011: Setting prohibited 100:TIOC1B I/O(MTU2) 101:RXD3 input(SCIF) 110: Setting prohibited 111: Setting prohibited
3	-	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	PB28MD[2:0]	000	R/W	PB28 Mode Select the function of the PB28/DACK0/TIOC1A/RXD3 pin. 000:PB28 I/O(port) 001:Setting prohibited 010:Dack0 output(DMAC) 011: Setting prohibited 100:Setting prohibited 101:TIOC1A I/O(MTU2) 110: Setting prohibited 111: Setting prohibited

[After]

Bit	Bit Name	Initial Value	R/W	Description
6 to 4	PB29MD[2:0]	000	R/W	PB29 Mode Select the function of the PB29/DREQ0/TIOC1B pin. 000:PB29 I/O(port) 001:Setting prohibited 010:DREQ0 input(DMAC) 011: Setting prohibited 100:TIOC1B I/O(MTU2) 101:Setting prohibited 110: Setting prohibited 111: Setting prohibited
3	-	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	PB28MD[2:0]	000	R/W	PB28 Mode Select the function of the PB28/DACK0/TIOC1A/RXD3 pin. 000:PB28 I/O(port) 001:Setting prohibited 010:Dack0 output(DMAC) 011: Setting prohibited 100:TIOC1A I/O(MTU2) 101:RXD3 input(SCIF) 110: Setting prohibited 111: Setting prohibited

4. Line 7 in the Figure 27.2 Recommended Time for Power-on/Power-off Sequence

[Before]

This undefined period can be eliminated by turning on/off the power supplies in the order shown in figure 27.2.

[After]

This undefined period can be eliminated by turning on the power supplies in the order shown in figure 27.2.

5. Notes in the Figure 27.2 Power-On Sequence

[Before]

Figure 27.2 Power-On/Off Sequence

Notes: 1. AVcc = AVREF > Vcc = PLLVcc is recommended. Either AVcc or VccQ power supply can be turned on or off first. However, note that the equation AVcc ± 0.3 V = AVREF should always be true. Using the LSI under the following conditions may result in decreased reliability or permanent damage to the LSI.
AVREF > AVcc ± 0.3 V

2. To prevent the pin and internal states from being undefined, VccQ and AVcc should be kept GND voltage level (0 V) and they should not be placed in floating state until Vcc reaches the Min. voltage. In addition, the /RES pin should be input low to place poweron reset state. In this case, care must be taken for the power consumption increase caused by sink current because each pin is placed in low-impedance state until VccQ reaches the Min. voltage.

[After]

Figure 27.2 Power-On Sequence

Notes: To prevent the pin and internal states from being undefined, VccQ and AVcc should be kept GND voltage level (0 V) and they should not be placed in floating state until Vcc reaches the Min. voltage. In addition, the /RES pin should be input low to place poweron reset state. In this case, care must be taken for the power consumption increase caused by sink current because each pin is placed in low-impedance state until VccQ reaches the Min. voltage.

6. Caution in the Table 27.3 DC Characteristics (1)

[Before]

Caution: When neither the A/D converter nor the D/A converter is in use, set Vcc ≤ AVcc ≤ 5.0 V ± 0.5 V and AVss = Vss, and do not leave the AVcc, AVss, AVREF, and AVREFVss pins open.

[After]

Caution: When neither the A/D converter nor the D/A converter is in use, do not leave the AVcc, AVss, AVREF, and AVREFVss pins open.

7. Table 27.8 Bus Timing

[Before]

Item	Symbol	Min.	Max.	Unit	Figure
Read data setup time 1	tRDS1	1/2tCYC + 20	-	ns	Figures 27.12 to 27.18
Write data hold time 1	tWDH1	1	-	ns	Figures 27.12 to 27.18

[After]

Item	Symbol	Min.	Max.	Unit	Figure
Read data setup time 1	tRDS1	1/2tCYC + 13	-	ns	Figures 27.12 to 27.18
/CS setup time	tCSS	0	-	ns	Figures 27.12 to 27.15
/CS hold time	tCSH	0	-	ns	Figures 27.12 to 27.15
Read data access time	tACC*2	tCYC x (n + 1.5) – 31 *1	-	ns	Figures 27.12 to 27.15 Figures 27.17 to 27.18
Access time from read strobe	tOE*2	tCYC x (n + 1) – 31 *1	-	ns	Figures 27.12 to 27.15 Figures 27.17 to 27.18
Write data hold time 1	tWDH1	1	15	ns	Figures 27.12 to 27.18

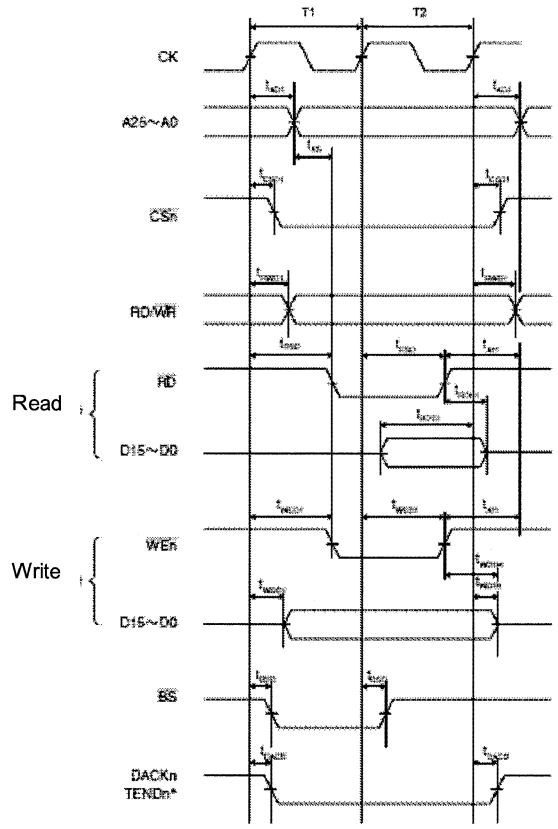
Note.

*1: "n" means wait cycles.

*2: "tRDS1" is not required to be satisfied if access time is satisfied.

8. Figure 27.12 Basic Bus Timing for Normal Space (No Wait)

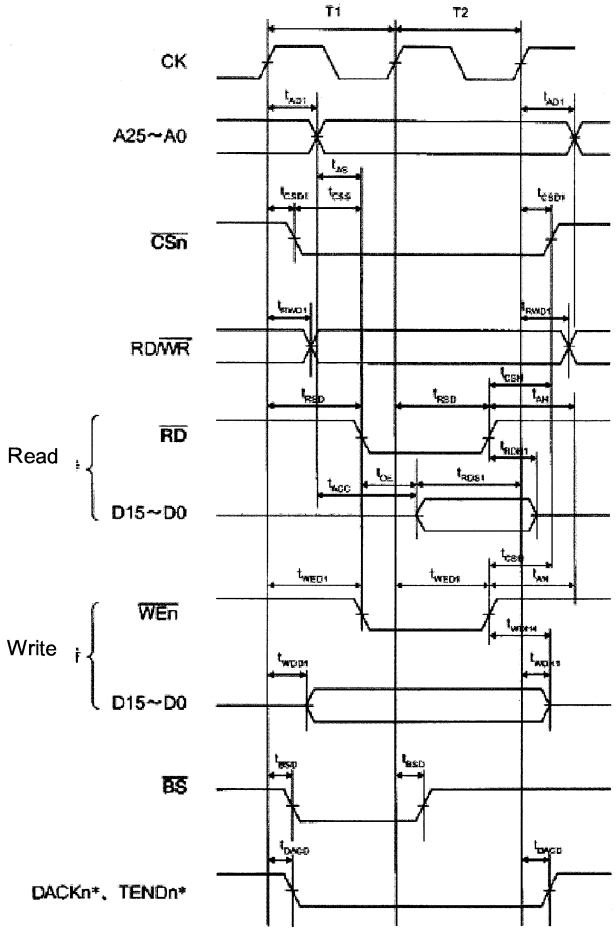
[Before] (Hardware Manual Rev. 2.00 Figure 27.12)



Note: * The waveform for DACKn and TENDn is when active low is specified.

Figure 27.12 Basic Bus Timing for Normal Space (No Wait)

[After]



Note: * The waveform for DACKn and TENDn is when active low is specified.

Figure 27.12 Basic Bus Timing for Normal Space (No Wait)

9. Figure 27.13 Basic Bus Timing for Normal Space (One Software Wait Cycle)

[Before] (Hardware Manual Rev. 2.00 Figure 27.13)

(Figure is omitted)

[After]

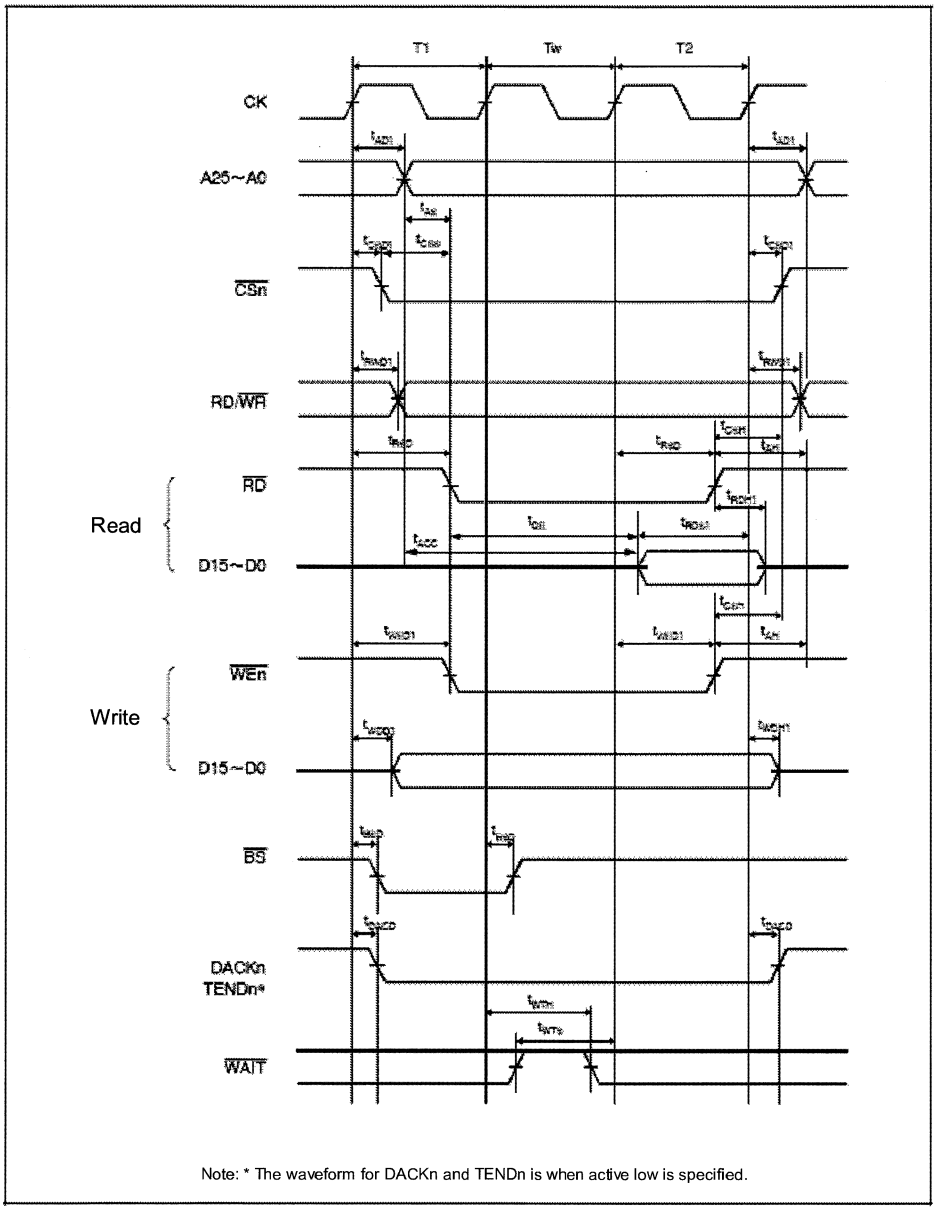


Figure 27.13 Basic Bus Timing for Normal Space (One Software Wait Cycle)

10. Figure 27.14 Basic Bus Timing for Normal Space (One External Wait Cycle)

[Before] (Hardware Manual Rev. 2.00 Figure 27.14)

(Figure is omitted)

[After]

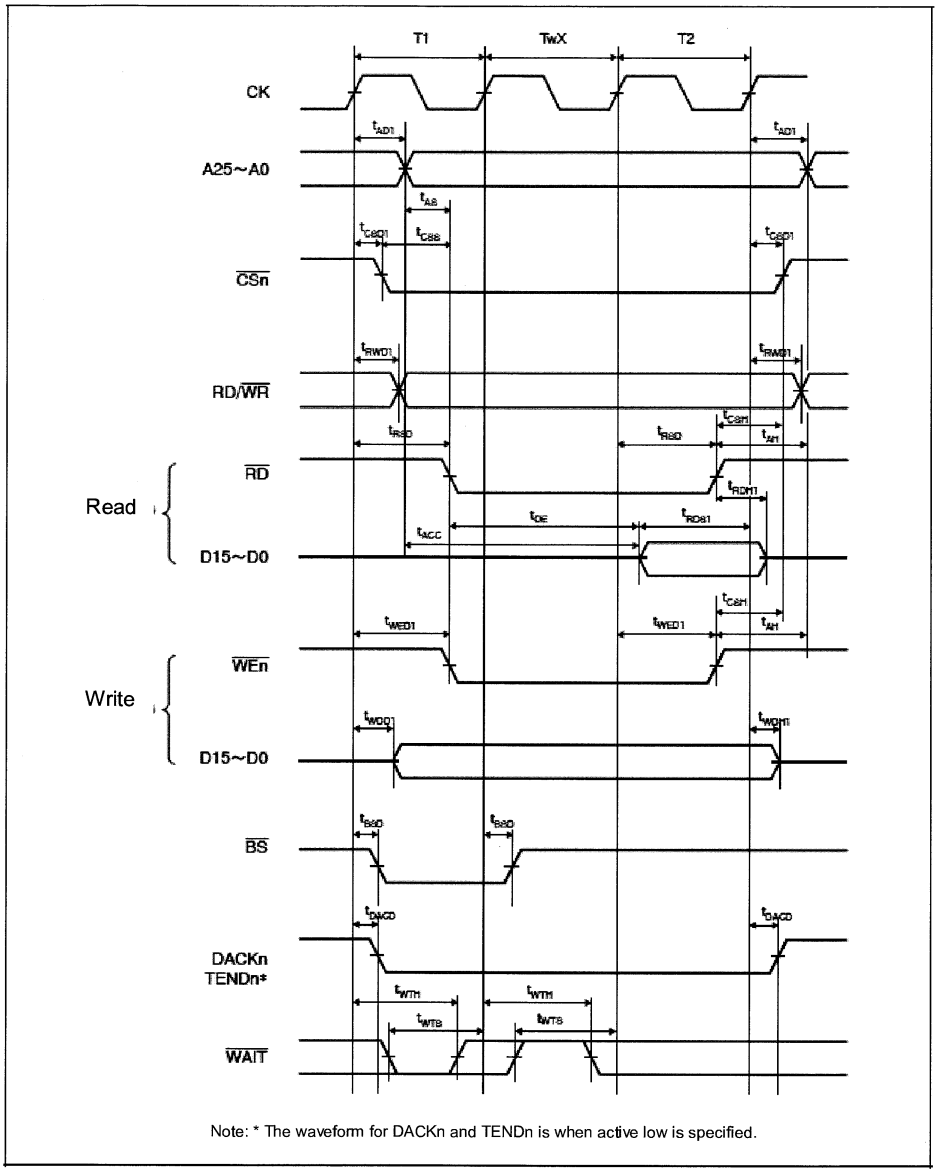


Figure 27.14 Basic Bus Timing for Normal Space (One External Wait Cycle)

11. Figure 27.15 Basic Bus Timing for Normal Space

[Before] (Hardware Manual Rev. 2.00 Figure 27.15)

(Figure is omitted)

[After]

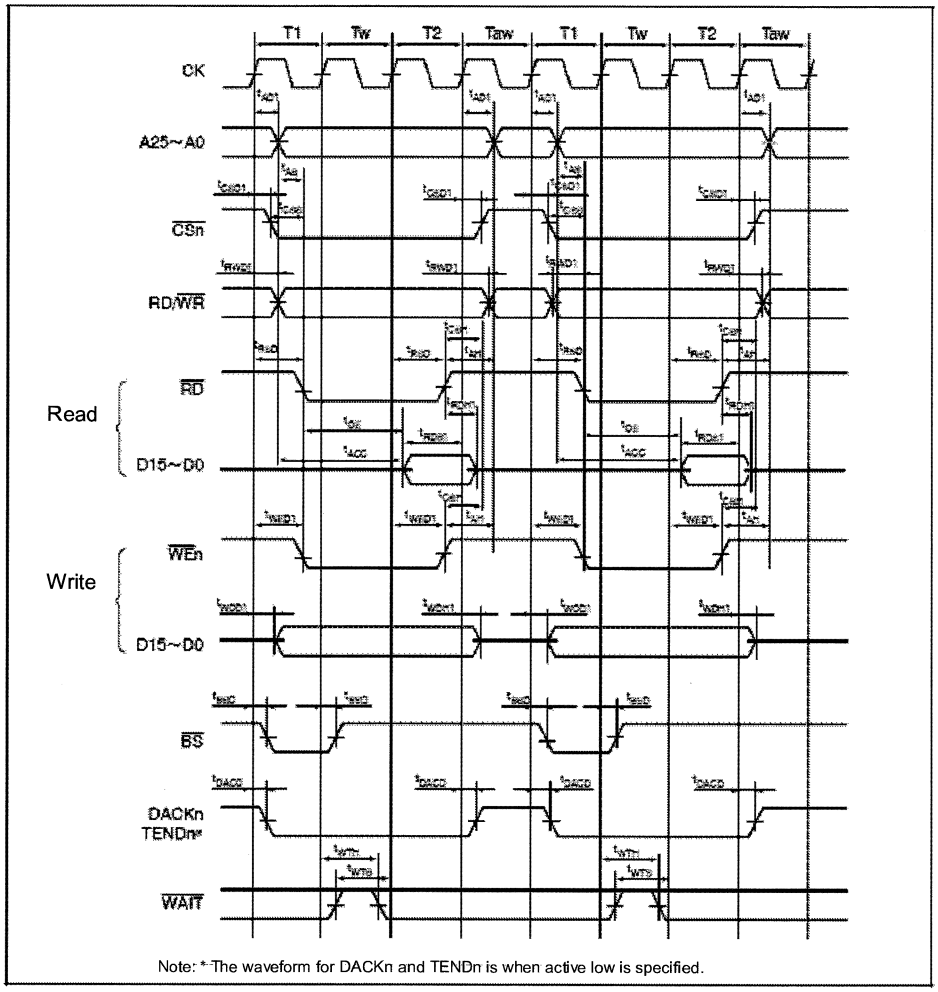


Figure 27.15 Basic Bus Timing for Normal Space

(One Software Wait Cycle, External Wait Cycle Valid (WM Bit = 0), No Idle Cycle)

12. Figure 27.17 Bus Cycle of SRAM with Byte Selection

[Before] (Hardware Manual Rev. 2.00 Figure 27.17)

(Figure is omitted)

[After]

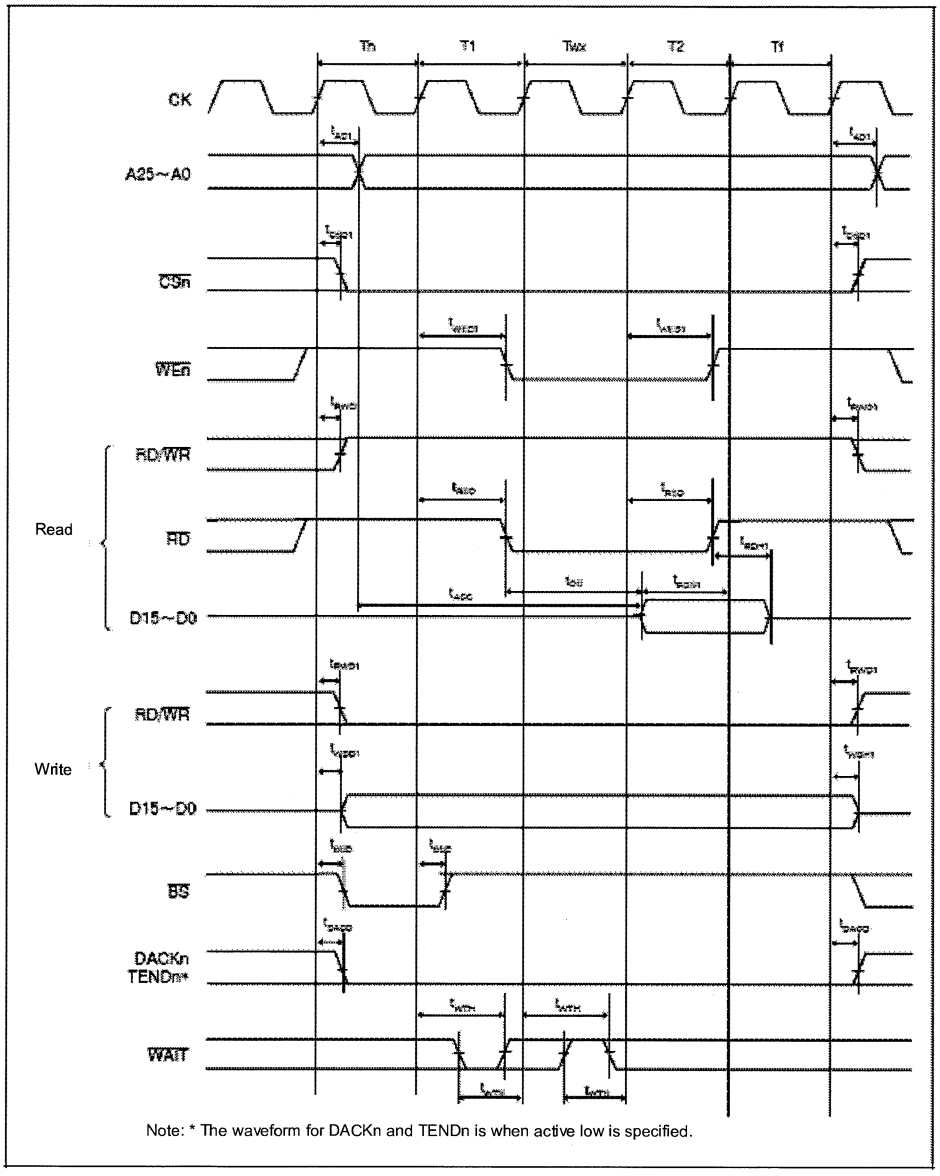


Figure 27.17 Bus Cycle of SRAM with Byte Selection (SW = 1 Cycle, HW = 1 Cycle, One Asynchronous External Wait Cycle, BAS = 0 (Write Cycle UB/LB Control))

13. Figure 27.18 Bus Cycle of SRAM with Byte Selection

[Before] (Hardware Manual Rev. 2.00 Figure 27.18)

(Figure is omitted)

[After]

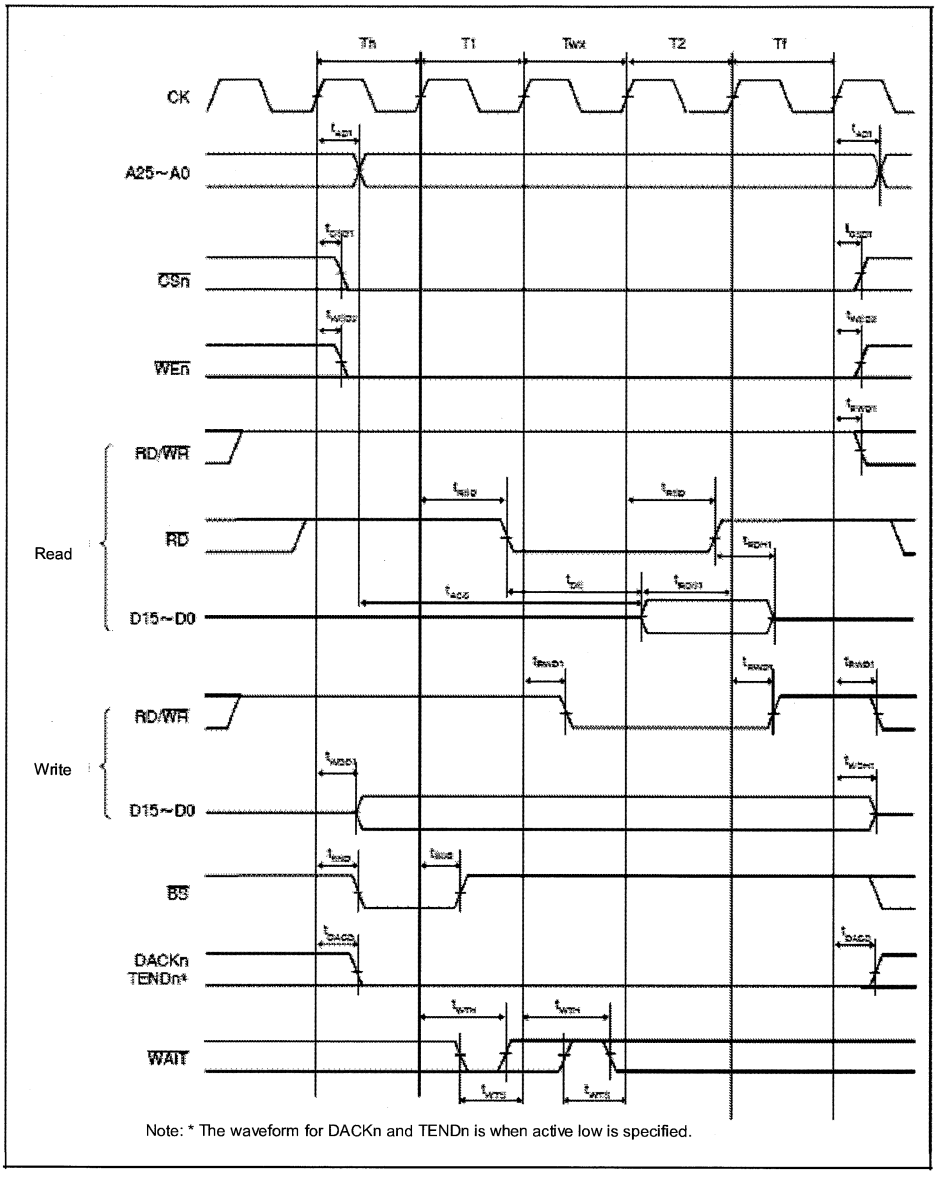


Figure 27.18 Bus Cycle of SRAM with Byte Selection (SW = 1 Cycle, HW = 1 Cycle, One Asynchronous External Wait Cycle, BAS = 1 (Write Cycle WE Control))

14. Table 27.15 I2C Bus Interface 3 Timing in the 27.4.10 IIC3 Module Timing

[Before]

Item	Symbol	Test Conditions	Specifications Min.	Typ.	Max.	Unit	Figure
SCL,SDA input rise time	t_{Sr}		—	—	300	t_{pcyc} *1	Figure 27.48
SCL,SDA input fall time	t_{Sf}		—	—	$1t_{pcyc}$	ns	

[After]

Item	Symbol	Test Conditions	Specifications Min.	Typ.	Max.	Unit	Figure
SCL,SDA input rise time	t_{Sr}		—	—	300	ns	Figure 27.48
SCL,SDA input fall time	t_{Sf}		—	—	300	ns	

15. Table 27.19 A/D Converter Characteristics in the 27.5 A/D Converter Characteristics

[Before]

Conditions: Vcc = PLLVcc = 1.4 V to 1.6 V, VccQ = 3.0 V to 3.6 V, AVcc = AV_{ref} = 4.5 V to 5.5 V,
Vss = PLLVss = VssQ = AVss = AVREFVss = 0 V, Ta = -40°C to +85°C,
V_{AN0-2} = 0.25 to AVcc -0.25 V, V_{AN3-7} = 0 V to AVcc

[After]

Conditions: Vcc = PLLVcc = 1.4 V to 1.6 V, VccQ = 3.0 V to 3.6 V, AVcc = 4.5V to 5.5V, AV_{ref} = 4.5 V to AVcc,
Vss = PLLVss = VssQ = AVss = AVREFVss = 0 V, Ta = -40°C to +85°C,
V_{AN0-2} = 0.25 to AVcc -0.25 V, V_{AN3-7} = 0 V to AVcc

16. Table 27.20 D/A Converter Characteristics in the 27.6 D/A Converter Characteristics

[Before]

Conditions: Vcc = PLLVcc = 1.4 V to 1.6 V, VccQ = 3.0 V to 3.6 V, AVcc = 4.5 V to 5.5 V,
Vss = PLLVss = VssQ = AVss = AVREFVss = 0 V, Ta = -40°C to +85°C

[After]

Conditions: Vcc = PLLVcc = 1.4 V to 1.6 V, VccQ = 3.0 V to 3.6 V, AVcc = 4.5 V to 5.5 V, AVREF=4.5V to AVCC,
Vss = PLLVss = VssQ = AVss = AVREFVss = 0 V, Ta = -40°C to +85°C