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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-R8C-A042A/E	Rev.	1.00
Title	Serial Interface (UART2) Special Mode1 (I2C Mode) Conditions		Information Category	Technical Notification		
Applicable Product	Described below	Lot No.	Reference Document			

Several conditions are added to the following applied product in the User's Manual.

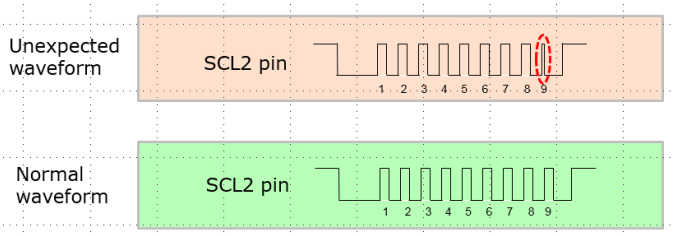
1-1. Applied Product

R8C/34E group, R8C/34F group, R8C/34G group, R8C/34H group,
R8C/36E group, R8C/36F group, R8C/36G group, R8C/36H group,
R8C/38E group, R8C/38F group, R8C/38G group, R8C/38H group,
R8C/34W group, R8C/34X group, R8C/34Y group, R8C/34Z group,
R8C/36W group, R8C/36X group, R8C/36Y group, R8C/36Z group,
R8C/38W group, R8C/38X group, R8C/38Y group, R8C/38Z group

1-2. Condition when using master

When using serial interface (UART2) Special Mode 1 (I2C mode) as master in the following condition, the 9th clock pulse of SCL2 output possibly be shorter than the normal width.

- Internal/External clock select bit (CKDIR) of UART2 Transmit /Receive mode Register (U2MR) as "0" (Internal clock).
- Clock synchronization bit (CSC) of UART2 Special Mode Register 2 (U2SMR2) as "1" (Approved).
- U2BRG count source select bit (CLK1/0) of UART2 Transmit /Receive Control Register 0 (U2C0) as 00:f1/01:f8 select



1-3. Countermeasure

In order to prevent such phenomenon, if that clock synchronization is not needed, Clock synchronization bit (CSC) shall be set to "0".

Also, there is a case that selecting 10:f32 at CLK 1/0 bit able to prevent, please contact Renesas sales.