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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A046A/E	Rev.	1.00
Title	RZ/T1 Group User's Manual: Hardware Restriction about 57th interrupt of Cortex-R4 vector interrupt controller		Information Category	Technical Notification		
Applicable Product	RZ/T1 Group	Lot No. All lots	Reference Document	RZ/T1 Group User's Manual: Hardware Rev.1.30 R01UH0483EJ0130 Rev.1.30		

There is a restriction about the 57th interrupt (TGID6) behavior of Cortex-R4 vector interrupt controller when it is used with DMA controller. The following describes restriction, workaround and correction of User's Manual Hardware.

1. Condition:

   In case of setting the 57th interrupt "MTU3a ch6 input capture/compare match D interrupt (TGID6)" of Cortex-R4 vector interrupt controller as DMA transfer completion interrupt.

2. Phenomenon

   An interrupt is generated when DMA transfer starts.

   DMA transfer completion interrupt is not generated.

3. Workaround

   The 57th interrupt cannot be used as DMA transfer completion interrupt. To confirm DMA transfer completion, check END bit of CHSTAT_n register.

4. Correction

Page	Description
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Vector Number	Request Source	Source		Detection Type	DMAC	DMAC setting vector Number
57	MTU3a	TGID6	ch6 input capture/compare match D interrupt	Edge	Y	Y

[Correct description]
Table 12.3 Cortex-R4F/DMAC Interrupt Vector Table (2/9)

Vector Number	Request Source	Source		Detection Type	DMAC	DMAC setting vector Number
57	MTU3a	TGID6	ch6 input capture/compare match D interrupt	Edge	Y	Y ***5**

Note 5. DMA transfer completion interrupt is not generated and an interrupt is generated at the same time as DMA request. Check CHSTAT_n.END register for DMA transfer completion.