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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A047A/E	Rev.	1.00
Title	RZ/T1 Group User's Manual: Hardware Correction and adding notifications about EtherMAC and EtherCAT Slave Controller		Information Category	Technical Notification		
Applicable Product	RZ/T1 Group	Lot No. All lots	Reference Document	RZ/T1 Group User's Manual: Hardware Rev.1.30 R01UH0483EJ0130 Rev.1.30		

Correction and adding notification about EtherMAC and EtherCAT Slave Controller.

Correction of manual are below.

■ **Correction of EtherMAC:**

No.	Page	Current description	Correct description
1	1324	28.2.2.5 RX Mode Register (GMAC_RXMODE) Function description of b31 AFILLTEREN 1 : Enables address filtering	28.2.2.5 RX Mode Register (GMAC_RXMODE) Function description of b31 AFILLTEREN 1 : Enables address filtering Note **[Note]** **Even though Address filtering is enabled, MAC Control Frames (ex. Pause Packet) are always received regardless contents of MAC Address Register. MAC Control Frame is the frame that the destination address is 01-80-C2-00-00-01.**
2	1352	[Current description] 28.3.1.3 (2) (e) Table 28.6 HWFNC_LongBuffer_Get Argument registers R4[15:0] / Buffer Length / Required buffer length. Unit: bytes. 1 to 2048 R4[23:16] / Reserved / Always 0 R4[31:24] / Unused R5[31:0] / Unused R6[31:0] / Unused R7[31:0] / Unused Return value registers R0[1:0] / Result / 0xb and R0[29] = 1: Success 10b: Invalid system call 11b: The buffer is insufficient R0[28:2] / Unused / All 0 R0[29] / Complete / 0: Hardware function call not completed 1: Hardware function call completed R0[31:30] / Unused / All 0 R1[31:0] / First logical address of the buffer / [31:27] 00001b [26] 1 [25:18] LLID [17:0] 0	

[Correct description]
28.3.1.3 (2) (e)
Table 28.6 HWFNC_LongBuffer_Get
Argument registers

R4	[15:0] Buffer Length	Required buffer length. Unit: bytes. 1 to 2048.
	[23:16]	Reserved bits. Always set to 0
	[31:24]	Not used in this Function call. Settings are ignored.
R5	[31:0]	Not used in this Function call. Settings are ignored.
R6	[31:0]	Not used in this Function call. Settings are ignored.
R7	[31:0]	Not used in this Function call. Settings are ignored.

Return value registers

R0	[1:0] Result	0xb and R0[29] = 1: Success 10b: Invalid system call 11b: The buffer is insufficient
	[28:2]	Reserved bits. Always set to 0
	[29] Complete	0: Hardware function call not completed 1: Hardware function call completed
	[31:30]	Reserved bits. Always set to 0
R1	[31:0] First logical address of the buffer	[31:27] 00001b [26] 1 [25:18] LLID [17:0] 0

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[Current description]
28.3.1.3 (2) (e)
Table 28.7 HWFNC_Short_Buffer_Get
Argument registers

R4[15:0]	Buffer Length	Required buffer length. Unit: bytes. 1 to 512.
R4[31:16]	Unused	
R5[31:0]	Unused	
R6[31:0]	Unused	
R7[31:0]	Unused	

Return value registers

R0[1:0]	Result	0xb: Success 10b: Invalid system call 11b: The buffer is insufficient
R0[28:2]	Unused	All 0
R0[29]	Complete	0: Hardware function call not completed 1: Hardware function call completed
R0[31:30]	Unused	All 0
R1[31:0]	First logical address of the buffer	[31:27] 00001b [26] 0 [25:18] SBID [18:0] 0

[Correct description]
28.3.1.3 (2) (e)
Table 28.7 HWFNC_Short_Buffer_Get
Argument registers

R4	[15:0] Buffer Length	Required buffer length. Unit: bytes. 1 to 512.
	[31:16]	Not used in this Function call. Settings are ignored.
R5	[31:0]	Not used in this Function call. Settings are ignored.
R6	[31:0]	Not used in this Function call. Settings are ignored.
R7	[31:0]	Not used in this Function call. Settings are ignored.

Return value registers

R0	[1:0] Result	0xb: Success 10b: Invalid system call 11b: The buffer is insufficient
	[28:2]	Reserved bits. Always set to 0
	[29] Complete	0: Hardware function call not completed 1: Hardware function call completed
	[31:30]	Reserved bits. Always set to 0
R1	[31:0] First logical address of the buffer	[31:27] 00001b [26] 0 [25:18] SBID [17:0] 0

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[Current description]
28.3.1.3 (2) (e)
Table 28.8 HWFNC_ Buffer_Release
Argument registers

R4[31:0]	First logical address of the buffer	First logical address of the buffer to be released The value is returned in R1 following a call of HWFNC_LongBuffer_Get or HWFNC_ShortBuffer_Get.
R5[31:0]	Unused	
R6[31:0]	Unused	
R7[31:0]	Unused	

Return value registers

R0[1:0]	Result	0xb: Success 10b: Invalid system call 11b: A buffer is not definable at the given address.
R0[28:2]	Unused	All 0
R0[29]	Complete	0: Hardware function call not completed 1: Hardware function call completed
R0[31:30]	Unused	All 0
R1[31:0]	Unused	All 0

[Correct description]
28.3.1.3 (2) (e)
Table 28.8 HWFNC_ Buffer_Release
Argument registers

R4	[31:0] First logical address of the buffer	0xb: Success 10b: Invalid system call 11b: A buffer is not definable at the given address.
R5	[31:0]	Not used in this Function call. Settings are ignored.
R6	[31:0]	Not used in this Function call. Settings are ignored.
R7	[31:0]	Not used in this Function call. Settings are ignored.

Return value registers

R0	[1:0] Result	0xb: Success 10b: Invalid system call 11b: The buffer is insufficient
	[28:2]	Reserved bits. Always set to 0
	[29] Complete	0: Hardware function call not completed 1: Hardware function call completed
	[31:30]	Reserved bits. Always set to 0
R1	[31:0]	Reserved bits. Always set to 0

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[Current description]
28.3.1.3 (2) (e)
Table 28.9 HWFNC_ Buffer_Return
Argument registers

R4[31:0]	First logical address of the buffer	First logical address of the buffer to be released The value is returned in R1 following a call of HWFNC_LongBuffer_Get or HWFNC_ShortBuffer_Get.
R5[31:0]	First logical address of the part for release	First address of the part for release (the part of the buffer at addresses beginning from this address is released)
R6[31:0]	Unused	
R7[31:0]	Unused	

Return value registers

R0[2:0]	Result	00xb: Success 010b: Invalid system call 011b: A buffer has not been defined at the address specified by R4. 100b: The buffer at the address specified by R5 has already been released.
R0[28:3]	Unused	All 0
R0[29]	Complete	0: Hardware function call not completed 1: Hardware function call completed
R0[31:30]	Unused	All 0
R1[31:0]	Unused	All 0

[Correct description]
28.3.1.3 (2) (e)
Table 28.9 HWFNC_ Buffer_Return
Argument registers

R4	[31:0] First logical address of the buffer	First logical address of the buffer to be released The value is returned in R1 following a call of HWFNC_LongBuffer_Get or HWFNC_ShortBuffer_Get.
R5	[31:0] First logical address of the part for release	First address of the part for release (the part of the buffer at addresses beginning from this address is released)
R6	[31:0]	Not used in this Function call. Settings are ignored.
R7	[31:0]	Not used in this Function call. Settings are ignored.

Return value registers

R0	[2:0] Result	00xb: Success 010b: Invalid system call 011b: A buffer has not been defined at the address specified by R4. 100b: The buffer at the address specified by R5 has already been released.
	[28:3]	Reserved bits. Always set to 0
	[29] Complete	0: Hardware function call not completed 1: Hardware function call completed
	[31:30]	Reserved bits. Always set to 0
R1	[31:0]	Reserved bits. Always set to 0

<table>
<tr><td>6</td><td>1359</td><td>28.3.1.4 (2) (b), 2-1)
[Example of reading and releasing a buffer]
(3) The bits [15:0] read from the BUFID are bits [26:11] of the address where the acquired buffer starts.
The individual bits of the address where the acquired buffer starts are configured as follows.
[31:27]: 00001b
[26:19]: Equivalent to the bits [15:8] in the BUFID ([26] of the start address is always 1; [25:19] are LBID[6:0])</td><td>28.3.1.4 (2) (b), 2-1)
[Example of reading and releasing a buffer]
(3) The bits [15:0] read from the BUFID are bits [26:11] of the address where the acquired buffer starts.
The individual bits of the address where the acquired buffer starts are configured as follows.
[31:27]: 00001b
[26:19]: Equivalent to the bits [15:8] in the BUFID ([26] of the start address is always 1; [25:19] are LLID[6:0])</td></tr>
<tr><td>7</td><td>1360</td><td colspan="2">[Current description]
28.3.1.4 (2) (c)
Table 28.10 HWFNC_ MACDMA_RX_Enable
Argument registers
<table>
<tr><td>R4[31:0]</td><td>Unused</td><td></td></tr>
<tr><td>R5[31:0]</td><td>Unused</td><td></td></tr>
<tr><td>R6[31:0]</td><td>Unused</td><td></td></tr>
<tr><td>R7[6:0]</td><td>Reserved</td><td>Always 0</td></tr>
<tr><td>R7[31:8]</td><td>Unused</td><td></td></tr>
</table>
Return value registers
<table>
<tr><td>R0[0]</td><td>Result</td><td>0: Success
1: Invalid system call*1</td></tr>
<tr><td>R0[28:1]</td><td>Unused</td><td>All 0</td></tr>
<tr><td>R0[29]</td><td>Complete</td><td>0: Hardware function call not completed
1: Hardware function call completed</td></tr>
<tr><td>R0[31:30]</td><td>Unused</td><td>All 0</td></tr>
<tr><td>R1[31:0]</td><td>Unused</td><td>All 0</td></tr>
</table>
[Correct description]
28.3.1.4 (2) (c)
Table 28.10 HWFNC_ MACDMA_RX_Enable
Argument registers
<table>
<tr><td>R4</td><td>[31:0]</td><td>Not used in this Function call. Settings are ignored.</td></tr>
<tr><td>R5</td><td>[31:0]</td><td>Not used in this Function call. Settings are ignored.</td></tr>
<tr><td>R6</td><td>[31:0]</td><td>Not used in this Function call. Settings are ignored.</td></tr>
<tr><td>R7</td><td>[31:0]</td><td>Not used in this Function call. Settings are ignored.</td></tr>
</table>
Return value registers
<table>
<tr><td rowspan="4">R0</td><td>[0] Result</td><td>0: Success
1: Invalid system call*1</td></tr>
<tr><td>[28:1]</td><td>Reserved bits. Always set to 0</td></tr>
<tr><td>[29] Complete</td><td>0: Hardware function call not completed
1: Hardware function call completed</td></tr>
<tr><td>[31:30]</td><td>Reserved bits. Always set to 0</td></tr>
<tr><td>R1</td><td>[31:0]</td><td>Reserved bits. Always set to 0</td></tr>
</table></td></tr>
</table>

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[Current description]
28.3.1.4 (2) (c)
Table 28.11 HWFNC_ MACDMA_RX_Disable
Argument registers

R4[0]	Forced reset	0: This function is disabled while reception is in progress. 1: If the reception DMAC is enabled, it is disabled even if reception is in progress (the reception DMAC is forcibly reset). Nothing is done if the reception DMAC is already disabled.
R4[31:1]	Unused	
R5[31:0]	Unused	
R6[31:0]	Unused	
R7[6:0]	Reserved	Always 0
R7[31:8]	Unused	

Return value registers

R0[0]	Result when R4[0] = 0	00b: Success 01b: Invalid system call (the buffer is in use or reception is suspended) 10b: The function cannot be disabled since reception is in progress. 11b: The function has already been disabled.
	Result when R4[0] = 1	00b: Success 01b: Invalid system call (the buffer is in use or reception is suspended)
R0[28:1]	Unused	All 0
R0[29]	Complete	0: Hardware function call not completed 1: Hardware function call completed
R0[31:30]	Unused	All 0
R1[31:0]	Unused	All 0

[Correct description]
28.3.1.4 (2) (c)
Table 28.11 HWFNC_ MACDMA_RX_Disable
Argument registers

R4	[0] Forced reset	0: This function is disabled while reception is in progress. 1: If the reception DMAC is enabled, it is disabled even if reception is in progress (the reception DMAC is forcibly reset). Nothing is done if the reception DMAC is already disabled.
	[31:1]	
R5	[31:0]	Not used in this Function call. Settings are ignored.
R6	[31:0]	Not used in this Function call. Settings are ignored.
R7	**[31:0]**	**Not used in this Function call. Settings are ignored.**

Return value registers

R0	[**1**:0] Result	Result when R4[0] = 0	00b: Success 01b: Invalid system call (the buffer is in use or reception is suspended) 10b: The function cannot be disabled since reception is in progress. 11b: The function has already been disabled.
		Result when R4[0] = 1	00b: Success 01b: Invalid system call (the buffer is in use or reception is suspended)
	[28:**2**]		Reserved bits. Always set to 0
	[29] Complete		0: Hardware function call not completed 1: Hardware function call completed
	[31:30]		Reserved bits. Always set to 0
R1	[31:0]		Reserved bits. Always set to 0

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[Current description]
28.3.1.4 (2) (c)
Table 28.12 HWFNC_MACDMA_RX_Control
Argument registers

R4[8:0]	Interrupt source	Controls enabling or disabling of the interrupt source corresponding to each bit. 0: Interrupts disabled 1: Interrupts enabled (initial value)
R4[31:9]	Unused	
R5[31:0]	Unused	
R6[31:0]	Unused	
R7[31:0]	Unused	

Return value registers

R0[0]	Result	0: Success 1: Invalid system call
R0[28:1]	Unused	All 0
R0[29]	Complete	0: Hardware function call not completed 1: Hardware function call completed
R0[31:30]	Unused	All 0
R1[31:0]	Unused	All 0

[Correct description]
28.3.1.4 (2) (c)
Table 28.12 HWFNC_MACDMA_RX_Control
Argument registers

R4	[8:0] Interrupt source	Controls enabling or disabling of the interrupt source corresponding to each bit. 0: Interrupts disabled 1: Interrupts enabled (initial value)
	[31:9]	Not used in this Function call. Settings are ignored.
R5	[31:0]	Not used in this Function call. Settings are ignored.
R6	[31:0]	Not used in this Function call. Settings are ignored.
R7	[31:0]	Not used in this Function call. Settings are ignored.

Return value registers

R0	[0] Result	0: Success 1: Invalid system call
	[28:1]	Reserved bits. Always set to 0
	[29] Complete	0: Hardware function call not completed 1: Hardware function call completed
	[31:30]	Reserved bits. Always set to 0
R1	[31:0]	Reserved bits. Always set to 0

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[Current description]
28.3.1.4 (2) (c)
Table 28.13 HWFNC_MACDMA_RX_Errstat
Argument registers

R4[31:0]	Unused	
R5[31:0]	Unused	
R6[31:0]	Unused	
R7[31:0]	Unused	

Return value registers

R0[3:0]	Result	[0]: Buffer Get fails [1]: Always 0 [2]: Rx data size over 4096 words (16 KB) [3]: HWFNC_MACDMA_Rx_Disable is issued when forced reset is enabled.
R0[28:4]	Unused	All 0
R0[29]	Complete	0: Hardware function call not completed 1: Hardware function call completed
R0[31:30]	Unused	All 0
R1[31:0]	Unused	All 0

[Correct description]
28.3.1.4 (2) (c)
Table 28.13 HWFNC_MACDMA_RX_Errstat
Argument registers

R4	[31:0]	Not used in this Function call. Settings are ignored.
R5	[31:0]	Not used in this Function call. Settings are ignored.
R6	[31:0]	Not used in this Function call. Settings are ignored.
R7	[31:0]	Not used in this Function call. Settings are ignored.

Return value registers

R0	[3:0] Result	[0]: Buffer Get fails [1]: Always 0 [2]: Rx data size over 4096 words (16 KB) [3]: HWFNC_MACDMA_Rx_Disable is issued when forced reset is enabled.
	[28:4]	Reserved bits. Always set to 0
	[29] Complete	0: Hardware function call not completed 1: Hardware function call completed
	[31:30]	Reserved bits. Always set to 0
R1	[31:0]	Reserved bits. Always set to 0

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[Current description]
28.3.1.4 (3) (d)
Table 28.14 HWFNC_MACDMA_TX_Start
Argument registers

R4[31:0]	Address of the descriptor	Address of the transmission descriptor
R5[31:0]	Unused	
R6[31:0]	Unused	
R7[6:0]	Reserved	Always 0
R7[31:7]	Unused	

Return value registers

R0[1:0]	Result	0: Success 1: Invalid system call
R0[28:2]	Unused	All 0
R0[29]	Complete	0: Hardware function call not completed 1: Hardware function call completed
R0[31:30]	Unused	All 0
R1[31:0]	Unused	All 0

[Correct description]
28.3.1.4 (3) (d)
Table 28.14 HWFNC_MACDMA_ TX_Start
Argument registers

R4	[31:0] Address of the descriptor	Address of the transmission descriptor
R5	[31:0]	Not used in this Function call. Settings are ignored.
R6	[31:0]	Not used in this Function call. Settings are ignored.
R7	[6:0]	Reserved bits. Always set to 0
	[31:7]	Not used in this Function call. Settings are ignored.

Return value registers

R0	[~~1.~~0] Result	0: Success 1: Invalid system call
	[28:1]	Reserved bits. Always set to 0
	[29] Complete	0: Hardware function call not completed 1: Hardware function call completed
	[31:30]	Reserved bits. Always set to 0
R1	[31:0]	Reserved bits. Always set to 0

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[Current description]
28.3.1.4 (3) (d)
Table 28.15 HWFNC_MACDMA_TX_Errstat
Argument registers

R4[31:0]	Unused	
R5[31:0]	Unused	
R6[31:0]	Unused	
R7[31:0]	Unused	

Return value registers

R0[1:0]	Result	[0]: Memory Access Violation [1]: Memory Access Timeout
R0[28:2]	Unused	All 0
R0[29]	Complete	0: Hardware function call not completed 1: Hardware function call completed
R0[31:30]	Unused	All 0
R1[31:0]	Unused	All 0

[Correct description]
28.3.1.4 (3) (d)
Table 28.15 HWFNC_MACDMA_TX_Errstat
Argument registers

R4	[31:0]	Not used in this Function call. Settings are ignored.
R5	[31:0]	Not used in this Function call. Settings are ignored.
R6	[31:0]	Not used in this Function call. Settings are ignored.
R7	[31:0]	Not used in this Function call. Settings are ignored.

Return value registers

R0	[1:0] Result	[0]: Memory Access Violation [1]: Memory Access Timeout
	[28:2]	Reserved bits. Always set to 0
	[29] Complete	0: Hardware function call not completed 1: Hardware function call completed
	[31:30]	Reserved bits. Always set to 0
R1	[31:0]	Reserved bits. Always set to 0

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[Current description]
28.3.1.5 (2) (c)
Table 28.16 HWFNC_Direct_Memory_Transfer

Name	HWFNC_Direct_Memory_Transfer
Function	Transfers data from the data RAM to the buffer RAM or from the buffer RAM to the data RAM. Data cannot be transferred from the buffer RAM to the buffer RAM. For transfer from the buffer RAM to the buffer RAM, use HWFNC_INT_BUF (however, data transfer from the data RAM to the data RAM is possible).

Argument registers

R4[31:0]	Address where the source area for transfer starts	Specifies the address where the source area for transfer starts.
R5[31:0]	Address where the destination area for transfer starts	Specifies the address where the destination area for transfer starts.
R6[31:0]	Number of bytes for transfer	Specifies the number of bytes for transfer.
R7[31:0]	Unused	

Return value registers

R0[1:0]	Result	00b: Success 01b: Invalid system call (transfer from the buffer RAM to the buffer RAM has been specified) 10b: An exception has occurred
R0[28:2]	Unused	All 0
R0[29]	Complete	0: Hardware function call not completed 1: Hardware function call completed
R0[31:30]	Unused	All 0
R1[31:0]	Address where the exception occurred	When an exception has occurred, this is the address where it occurred. In other cases, all 0s.

[Correct description]
28.3.1.5 (2) (c)
Table 28.16 HWFNC_Direct_Memory_Transfer

Name	HWFNC_Direct_Memory_Transfer
Function	Transfers data from the data RAM to the buffer RAM or from the buffer RAM to the data RAM. ~~**Data cannot be transferred from the buffer RAM to the buffer RAM. For transfer from the buffer RAM to the buffer RAM, use HWFNC_INT_BUF (however, data transfer from the data RAM to the data RAM is possible).**~~

Argument registers

R4	[31:0] Address where the source area for transfer starts	Specifies the address where the source area for transfer starts.
R5	[31:0] Address where the destination area for transfer starts	Specifies the address where the destination area for transfer starts.
R6	[31:0] Number of bytes for transfer	Specifies the number of bytes for transfer.
R7	[31:0]	Not used in this Function call. Settings are ignored.

Return value registers

R0	[1:0] Result	00b: Success 01b: Invalid system call (transfer from the buffer RAM to the buffer RAM has been specified) 10b: An exception has occurred
	[28:2]	Reserved bits. Always set to 0
	[29] Complete	0: Hardware function call not completed 1: Hardware function call completed
	[31:30]	Reserved bits. Always set to 0
R1	[31:0] Address where the exception occurred	When an exception has occurred, this is the address where it occurred. In other cases, all 0s.

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[Current description]
28.3.1.5 (2) (c)
Table 28.17 HWFNC_Direct_Memory_Replace

Name	HWFNC_Direct_Memory_ Replace
Function	Replaces the specified memory area in the data RAM or buffer RAM with a defined data pattern. The number of words to be written must be at least four.

Argument registers

R4[31:0]	Pattern	Specifies the data pattern for writing.
R5[31:0]	Start address	Specifies the address where the destination area for writing starts.
R6[31:0]	Number of words	Specifies the number of words to be written.
R7[31:0]	Unused	

Return value registers

R0[1:0]	Result	00b: Success 01b: Invalid system call The set address was specified in byte units or the setting for the number of words to be transferred is three or fewer. 10b: An exception has occurred.
R0[28:2]	Unused	All 0
R0[29]	Complete	0: Hardware function call not completed 1: Hardware function call completed
R0[31:30]	Unused	All 0
R1[31:0]	Address where the exception occurred	When an exception has occurred, this is the address where it occurred. In other cases, all 0s.

[Correct description]
28.3.1.5 (2) (c)
Table 28.17 HWFNC_Direct_Memory_Replace

Name	HWFNC_Direct_Memory_ Replace
Function	Replaces the specified memory area in the data RAM or buffer RAM with a defined data pattern. The number of words to be written must be at least four. **(A words unit is 32 bits)**

Argument registers

R4	[31:0] Pattern	Specifies the data pattern for writing.
R5	[31:0] Start address	Specifies the address where the destination area for writing starts.
R6	[31:0] Number of words	Specifies the number of words to be written.
R7	[31:0]	Not used in this Function call. Settings are ignored.

Return value registers

R0	[1:0] Result	00b: Success 01b: Invalid system call The set address was specified in byte units or the setting for the number of words to be transferred is three or fewer. 10b: An exception has occurred.
	[28:2]	Reserved bits. Always set to 0
	[29] Complete	0: Hardware function call not completed 1: Hardware function call completed
	[31:30]	Reserved bits. Always set to 0
R1	[31:0] Address where the exception occurred	When an exception has occurred, this is the address where it occurred. In other cases, all 0s.

<table>
<tr><td>15</td><td>1369</td><td>28.3.2 Table 28.18 Interrupt related Operations for Transmission

Conditions for Asserting and De-asserting Interrupts of TX FIFO error interrupt

This interrupt is generated when information is further updated while the GMAC_TXID/GMAC_TXRESULT register is holding the maximum number of items of information (four). Take care, since the oldest of the retained information will have been overwritten when this error occurs.
Reading the GMAC_TXID/GMAC_TXRESULT register leads to clearing of the retained information and restoring normal operation.</td><td>28.3.2 Table 28.18 Interrupt related Operations for Transmission

Conditions for Asserting and De-asserting Interrupts of TX FIFO error interrupt

This interrupt is generated when information is further updated while the GMAC_TXID/GMAC_TXRESULT register is holding the maximum number of items of information (four). Take care, since the oldest of the retained information will have been overwritten when this error occurs.
Reading the GMAC_TXID/GMAC_TXRESULT register repeatedly until the value of the GMAC_TXFIFO.TRBFR bit becomes 0 leads to clearing of the retained information and restoring normal operation.</td></tr>
<tr><td>16</td><td>1373</td><td>28.3.3.2 (1) Tx frame control information<table><tr><td>Item</td><td>Explanation</td></tr><tr><td>TX_WORD[12:0]</td><td>Specifies the number of words in the Ethernet frame to be transmitted. The number of valid bytes in the last word is specified by using TX_EOB[1:0].</td></tr><tr><td>TCPIP ACC OFF</td><td>1: Disables the TCPIP accelerator.
0: Enables the TCPIP accelerator.</td></tr><tr><td>APAD</td><td>Padding is inserted because the frame length is less than 64 octets.</td></tr></table></td><td>28.3.3.2 (1) Tx frame control information<table><tr><td>Item</td><td>Explanation</td></tr><tr><td>TX_WORD[12:0]</td><td>Specifies the number of words in the Ethernet frame to be transmitted (A word unit is 32 bits). The number of valid bytes in the last word is specified by using TX_EOB[1:0].</td></tr><tr><td>TCPIP ACC OFF*2</td><td>1: Disables the TCPIP accelerator.
0: Enables the TCPIP accelerator.</td></tr><tr><td>APAD</td><td>Padding is automatically inserted if the frame length is less than 64 octets.</td></tr></table>Note2: Disable the TCPIP accelerator if the following frames are sent;
● IPv6 frames without UDP or TCP packet
● iEEE802.3 + IEEE802.2 (LLC) frames</td></tr>
<tr><td>17</td><td>1374</td><td>28.3.3.2 (2) (a)
Figure 28.16 Format for Transmission Data (TCPIP Accelerator Enabled, VLAN Tag included)<table><tr><td colspan="2">Destination MAC address(6bytes)</td></tr><tr><td colspan="2">Source MAC address(6bytes)</td></tr><tr><td>Padding(2bytes)</td><td>VLAN tag(2bytes)</td></tr><tr><td>Type/Length(2bytes)</td><td>VLAN tag(2bytes)</td></tr><tr><td colspan="2">Frame payload(Max. 1500bytes)</td></tr></table></td><td>28.3.3.2 (2) (a)
Figure 28.16 Format for Transmission Data (TCPIP Accelerator Enabled, VLAN Tag included)<table><tr><td colspan="2">Destination MAC address(6bytes)</td></tr><tr><td colspan="2">Source MAC address(6bytes)</td></tr><tr><td>Padding(2bytes)</td><td>VLAN tag(2bytes)</td></tr><tr><td>Type/Length(2bytes)</td><td>VLAN Info(2bytes)</td></tr><tr><td colspan="2">Frame payload(Max. 1500bytes)</td></tr></table></td></tr>
<tr><td>18</td><td>1376</td><td>28.3.3.3 Creating transmit descriptors
Note that this function is subject to the following restrictions:
• If Linked Long Buffer is specified as a descriptor with Release Bit = 1
• Only the buffer that includes the address specified by the descriptor is released.
• The buffer linked with the released buffer is not released.</td><td>28.3.3.3 Creating transmit descriptors
~~Note that this function is subject to the following restrictions:~~
~~• If Linked Long Buffer is specified as a descriptor with Release Bit = 1~~
~~• Only the buffer that includes the address specified by the descriptor is released.~~
~~• The buffer linked with the released buffer is not released.~~</td></tr>
<tr><td>19</td><td>1379</td><td>28.3.4.6 Format of receive data
If a frame is received by using Ethernet MAC, 64-bit receive frame information is suffixed to the frame data. The Ethernet frame size, error status, and other information can be obtained from the receive frame information.
Receive frame information begins at a 64-bit boundary. Therefore, the size of padding at the end of Ethernet frames changes according to the frame size.</td><td>28.3.4.6 Format of receive data
If a frame is received by using Ethernet MAC, 64-bit receive frame information is suffixed to the frame data. The Ethernet frame size, error status, and other information can be obtained from the receive frame information.
Receive frame information begins at a 64-bit boundary. Therefore, the size of next padding at the end of Ethernet frames changes according to the frame size.</td></tr>
</table>

<table>
<tr>
<td>20</td>
<td>1380, 1381</td>
<td>28.3.4.6 (1) Reception frame information
<table>
<tr><td>item</td><td>Explanation</td></tr>
<tr><td>IPNG</td><td>If this field is set to ‘1’, it indicates that the checksum of the IPv4 header conflicts with the calculation result of the TCPIP accelerator.</td></tr>
<tr><td>TCPNG</td><td>If this field is set to ‘1’, it indicates that the checksum of the TCP or UDP header conflicts with the calculation result of the TCPIP accelerator.</td></tr>
<tr><td>IPV6NG</td><td>If this field is set to ‘1’, it indicates that the IPv6 extended header is one from among routing, Hopby-Hop, or Destination Opt, and that the value of the header length field is incorrect.</td></tr>
<tr><td>OUT_OF_LIST</td><td>If this field is set to ‘1’, it indicates that a protocol number not listed below was detected in the IPv6 extended header.
06h: TCP header
11h: UDP header
00h: Hop-by-Hop
3Ch: Destination Opt
2Ch: Fragment
2Bh: Routing
3Bh: No next header
32h: ESP header
33h: AH header</td></tr>
<tr><td>TYPEIP</td><td>If this field is set to ‘1’, it indicates that an IP packet was received.</td></tr>
<tr><td>MAACL</td><td>If this field is set to ‘1’, it indicates that an 802.3 (LLC/SNAP) packet was received.</td></tr>
<tr><td>PPPOE</td><td>If this field is set to ‘1’, it indicates that a PPPoE packet was received.</td></tr>
<tr><td>VTAG</td><td>If this field is set to ‘1’, it indicates that the packet included a VLAN tag.</td></tr>
</table></td>
<td>28.3.4.6 (1) Reception frame information
<table>
<tr><td>item</td><td>Explanation</td></tr>
<tr><td>IPNG Note</td><td>If this field is set to ‘1’, it indicates that the checksum of the IPv4 header conflicts with the calculation result of the TCPIP accelerator.</td></tr>
<tr><td>TCPNG Note</td><td>If this field is set to ‘1’, it indicates that the checksum of the TCP or UDP header conflicts with the calculation result of the TCPIP accelerator.</td></tr>
<tr><td>IPV6NG Note</td><td>If this field is set to ‘1’, it indicates that the IPv6 extended header is one from among routing, Hopby-Hop, or Destination Opt, and that the value of the header length field is incorrect.</td></tr>
<tr><td>OUT_OF_LIST Note</td><td>If this field is set to ‘1’, it indicates that a protocol number not listed below was detected in the IPv6 extended header.
06h: TCP header
11h: UDP header
00h: Hop-by-Hop
3Ch: Destination Opt
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<tr><td>TYPEIP Note</td><td>If this field is set to ‘1’, it indicates that an IP packet was received.</td></tr>
<tr><td>MAACL Note</td><td>If this field is set to ‘1’, it indicates that an 802.3 (LLC/SNAP) packet was received.</td></tr>
<tr><td>PPPOE Note</td><td>If this field is set to ‘1’, it indicates that a PPPoE packet was received.</td></tr>
<tr><td>VTAG Note</td><td>If this field is set to ‘1’, it indicates that the packet included a VLAN tag.</td></tr>
</table>
Note: These fields are invalid if TCPIP accelerator is disabled.</td>
</tr>
<tr>
<td>21</td>
<td>1386</td>
<td>28.3.5.1 Transmission with Use of the TCPIP Accelerator

Note: If the result of calculating the UDP checksum of a packet for transmission is 0000h, write FFFFh to the checksum field.</td>
<td>28.3.5.1 Transmission with Use of the TCPIP Accelerator

Note1: If the result of calculating the UDP checksum of a packet for transmission is 0000h, write FFFFh to the checksum field.

Note2: If the value of the header length field of IPv4 does not match with that of actual header length, the transmission may never end.</td>
</tr>
<tr>
<td>22</td>
<td>1387</td>
<td>28.3.5.2 Reception with Use of the TCPIP Accelerator
When TCPIPACC is enabled, two bytes of padding for the TCPIP accelerator are inserted in the MAC headers of received frames.
When the reception TCPIP accelerator is enabled and a received packet includes TCP/UDP, the FCS field is overwritten by the checksum value of TCP/UDP. This checksum value can be used for calculating the total checksum value of fragmented TCP/UDP packets.</td>
<td>28.3.5.2 Reception with Use of the TCPIP Accelerator
When TCPIPACC is enabled, two bytes of padding for the TCPIP accelerator are inserted in the MAC headers of received frames.
When the reception TCPIP accelerator is enabled and a received packet includes TCP/UDP, the FCS field is overwritten by the checksum value of TCP/UDP. This checksum value can be used for calculating the total checksum value of fragmented TCP/UDP packets.
However, the checksum of Pseudo Header needs to be calculated by software because the checksum field is not contained in Pseudo Header for fragment packets.</td>
</tr>
<tr>
<td>23</td>
<td>1387</td>
<td>28.3.5.2 Reception with Use of the TCPIP Accelerator
Note: If the checksum field of the UDP header of the received packet is 0000h, checksum comparison does not proceed.</td>
<td>28.3.5.2 Reception with Use of the TCPIP Accelerator
Note: If the checksum field of the UDP header of the received packet is 0000h, checksum comparison does not proceed. TCPNG bit is set to 0.</td>
</tr>
</table>

24	1389	[Current description] No description.
		[Correct description] Add the description in below. **28.4.4 Erroneous Judgment of Checksum Validation at Reception** **(1) Target: Ethernet Ⅱ frame and IEEE802.3 + IEEE802.2 (LLC+SNAP) frame** **When a frame is received under below conditions listed, IPNG field or TCPNG field of the Reception Frame Information may become "1" even the packet is valid. If these conditions are met, checksum value must be checked by software.** ● **Value of the checksum field in IPv4, TCP header is 0x0000 or 0xFFFF** ● **A frame length that excluded IPv6, FCS is over 60 bytes. Payload of TCP or UDP is 1 byte and the data followed are not 0** ● **The Value of the checksum of Pseudo header used for calculating the checksum of IPv6, TCP or UDP is over 21 bits** **(2) Target: IEEE802.3 + IEEE802.2 (LLC) frame** **If IEEE802.3 + IEEE802.2 (LLC) frame that does not have SNAP is received, TYPEIP field and IPNG field may become "1". In this case, Check the presence of SNAP by software and if SNAP is not present, handle that frame as valid.**

■ **Correction of EtherCAT Slave Controller:**

No.	Page	Current description	Correct description
1	1519	30.8.1 AL Control Register (AL_CONTROL) Description of b5 Value after reset: x Symbol:— Bit Name: Reserved Description : When read, the value returned is undefined. PDI:R(Clear) ECAT:R/(W)	30.8.1 AL Control Register (AL_CONTROL) Description of b5 Value after reset: **0** Symbol:**DEVICEID** Bit Name: **Device ID Request** Description:**Device ID Request** **0: No request** **1: Device ID request** PDI:R(Clear) ECAT:R/(W)
2	1520	30.8.2 AL Status Register (AL_STATUS) Description of b5 Value after reset: x Symbol:— Bit Name: Reserved Description : When read, the value returned is undefined.	30.8.2 AL Status Register (AL_STATUS) Description of b5 Value after reset: **0** Symbol:**DEVICEID** Bit Name: **Device ID Status** Description:**Device ID Status** **0: Device ID not valid** **1: Device ID loaded**
3	1525	30.9.3 PDI Configuration Register (PDI_CONFIG) Description of b7 to b5 Value after reset: 010 Symbol:ONCHIPBUS Bit Name: On-Chip Bus Type Indication Description:Indicate the type of on-chip bus. In this chip, the value is always 100.	30.9.3 PDI Configuration Register (PDI_CONFIG) Description of b7 to b5 Value after reset: 010 Symbol:ONCHIPBUS Bit Name: On-Chip Bus Type Indication Description:Indicate the type of on-chip bus. In this chip, the value is always **010**.
4	1544	30.14.7 PHY Port Status n Register (PHY_STATUSn)	~~**30.14.7 PHY Port Status n Register (PHY_STATUSn)**~~
5	1580	[Current description] No description.	
		[Correct description] Add the description in below. **30.20 Configuration of Reset Circuit** **The configuration of Reset Circuit of ESC is shown in Figure 30.2. When Reset Request (0040h) by ECAT or Reset Request (0041h) by PDI have been received, ESC will stop and RESET pin output from ESC becomes "1". The RESET pin output from ESC will cause the PHYRESETOUT# pin to be low, then it will reset the Ethernet PHY that connected outside. And ETHCRSTI interrupt is generated.** **After ETHCRSTI interrupt is detected, it is necessary to switch the CATRST bit in the ETHSFTRST register from "1" to "0" to "1". To be noted, at the time the ESC reset input goes from "1" to "0", the ESC reset output will be "0". At the time when the ESC reset input goes from "0" to "1", the ESC starts restarting and the loading of the EEPROM will be started. The loading of EEPROM will be completed in about 1 ms. Be sure to set the timing of cancelling the reset of the Ethernet PHY, so that the restart of the Ethernet PHY will be after the start of ESC is completed. The timing chart is shown in Figure 30.3.** **It is also possible to reset the ESC with the CATRST bit in the ETHSFTRST register, not by the ECAT/PDI reset request (0040h/0041h). In this case, since the PHYRESETOUT# pin does not automatically go low, set the Ethernet PHY to the reset state beforehand by the PHYRST bit in the ETHSFTRST register. The timing chart is shown in Figure 30.4.**	

5	1580	

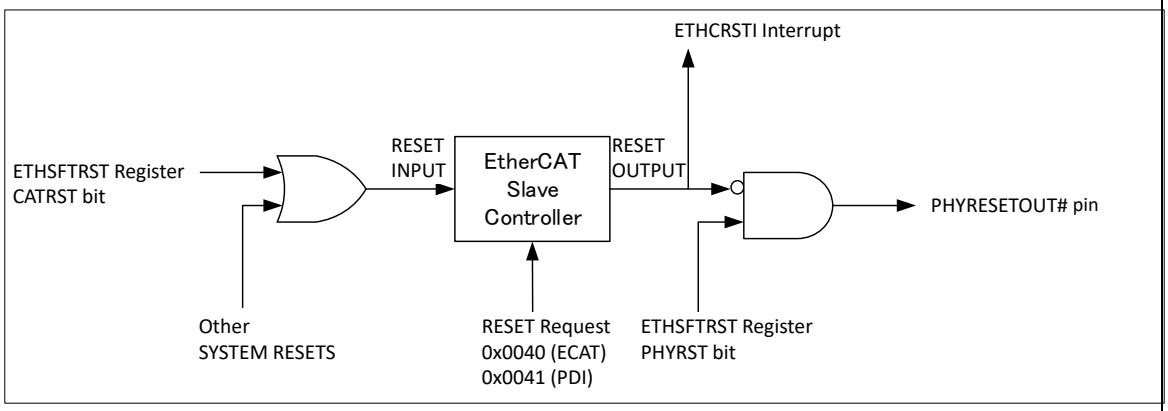

Figure 30.2 Configuration of Reset Circuit of EtherCAT Slave Controller

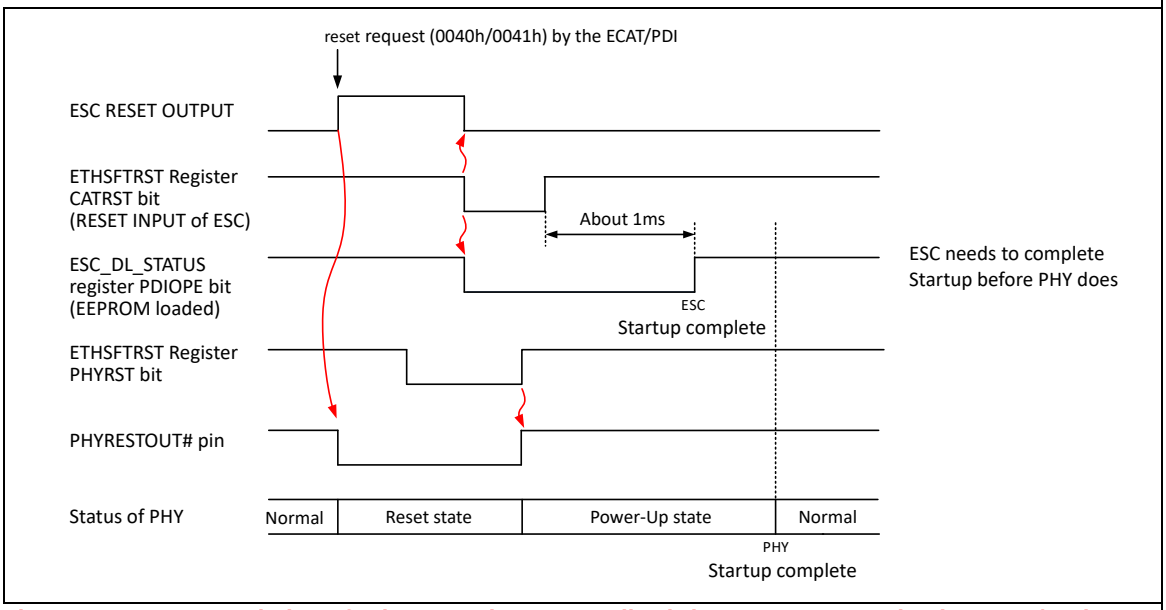

Figure 30.3 Reset timing of EtherCAT Slave Controller (when reset request by the ECAT/PDI)

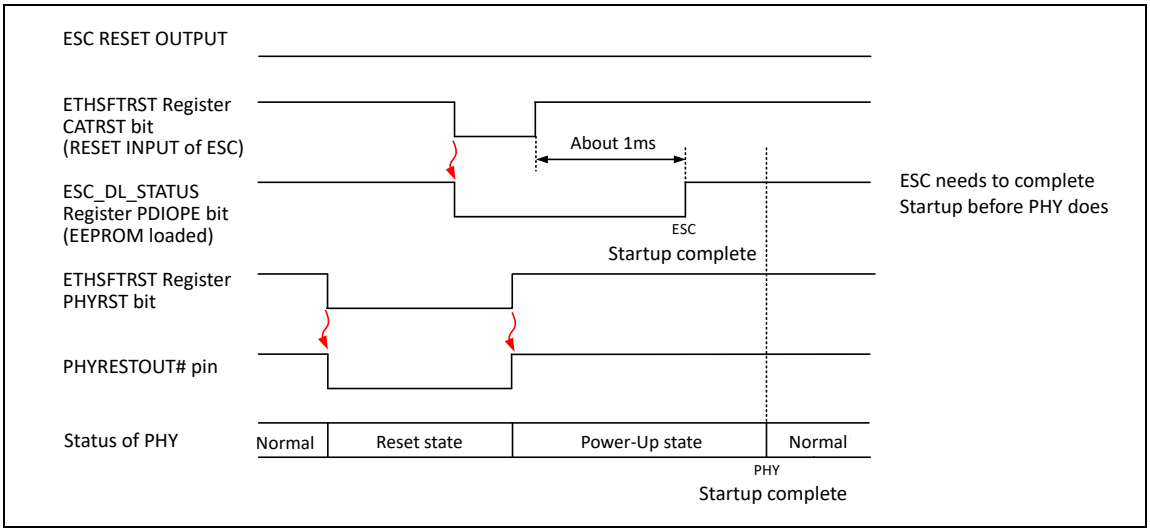

Figure 30.4 Reset timing of EtherCAT Slave Controller (when reset by the CATRST bit of ETHSFTRST)