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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0090A/E	Rev.	1.00
Title	RZ/G2N and G2E Additional Descriptions for SYSC		Information Category	Technical Notification		
Applicable Product	RZ/G Series, 2nd Generation RZ/G2N RZ/G2E	Lot No. All lots	Reference Document	RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.10 (R01UH0808EJ0110)		

This technical update describes document correction of RZ/G Series, 2nd Generation product.

[Summary]

Additional Descriptions for “RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.10”.

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Products]

RZ/G2N

RZ/G2E

[Section number and title]

Section 14. System Controller (SYSC)

“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. Section 14. SYSC, Page 14-73, 14-74, 14.3.2 Initial state of power domains, Table 14.6 Initial state of power domains (RZ/G2E), 3rd Column of Boot is not disclosed. Table 14.7 Initial state of power domains (RZ/G2N) is added.

Current (from):

14.3.2 Initial state of power domains

Table 14.5 and 14.6 shows initial states of each power domain. Initial power state of CPUs depends on the selection of boot CPU, which was specified by mode pins.

Table 14.5 Initial state of power domains (RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0)

Domain name	Cortex-A57 Boot	Cortex-A53 Boot	Remark
Cortex-A57 CPU0	ON	OFF	—
Cortex-A57 CPU1/2/3	OFF	OFF	—
Cortex-A57 SCU	ON	OFF	—
Cortex-A53 CPU0	OFF	ON	—
Cortex-A53 CPU1/2/3	OFF	OFF	—
Cortex-A53 SCU	OFF	ON	—
3DG-A/B/C/D/E	OFF	OFF	—
A3IR/A3VP/A3VC/A2VC0/A2VC1	OFF	OFF	—

Table 14.6 Initial state of power domains (RZ/G2E)

Domain name	Cortex-A53 Boot	Boot	Remark
Cortex-A53 CPU0	ON	OFF	—
Cortex-A53 CPU1	OFF	OFF	—
Cortex-A53 SCU	ON	OFF	—
A3VC/A2VC1	OFF	OFF	—
3DG-A/B	OFF	OFF	—

14.3.3 Power Control of Arm CPUs

The AP system cores (Cortex-A53 and Cortex-A57) can be powered off by executing the WFI instruction. Similarly, power of Arm CPUs can be resumed either by controlling the APMU (Advanced Power Management Unit) registers or by an IRQ or FIQ interrupt.

For detail of power control by APMU registers, see section 13, Advanced Power Management Unit for AP-System Core (APMU).

(1) Power Control by WFI Instruction and Interrupts

The power shutdown by the WFI instruction is performed only when Cortex-A57/ Cortex-A53 CPUn power status control register (CA57CPUnCR, CA53CPUnCR) are in the core standby mode. In case of other setting, power shutdown sequence is not activated by the WFI instruction. See section 13, Advanced Power Management Unit for AP-System Core (APMU).

Power can be resumed by an IRQ or FIQ interrupt on the Arm core. After resuming power of Cortex-A57, Cortex-A53, CPUs by IRQ/FIQ, read the value of SYSCEERSR, SYSCEERSR 2, and SYSCEERSR3 registers. Without reading those registers after power-resuming, the shutdown sequence of related CPUs will not start.

Correction (to):

14.3.2 Initial state of power domains

Table 14.5 and 14.6 shows initial states of each power domain. Initial power state of CPUs depends on the selection of boot CPU, which was specified by mode pins.

Table 14.5 Initial state of power domains (RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0)

Domain name	Cortex-A57 Boot	Cortex-A53 Boot	Remark
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Cortex-A57 CPU1/2/3	OFF	OFF	—
Cortex-A57 SCU	ON	OFF	—
Cortex-A53 CPU0	OFF	ON	—
Cortex-A53 CPU1/2/3	OFF	OFF	—
Cortex-A53 SCU	OFF	ON	—
3DG-A/B/C/D/E	OFF	OFF	—
A3IR/A3VP/A3VC/A2VC0/A2VC1	OFF	OFF	—

Table 14.6 Initial state of power domains (RZ/G2E)

Domain name	Cortex-A53 Boot	Remark
Cortex-A53 CPU0	ON	—
Cortex-A53 CPU1	OFF	—
Cortex-A53 SCU	ON	—
A3VC/A2VC1	OFF	—
3DG-A/B	OFF	—

Table 14.7 Initial state of power domains (RZ/G2N)

Domain name	Cortex-A57 Boot	Remark
Cortex-A57 CPU0	ON	—
Cortex-A57 CPU1	OFF	—
Cortex-A57 SCU	ON	—
A3VP/A3VC/A2VC1	OFF	—
3DG-A/B	OFF	—

14.3.3 Power Control of Arm CPUs

The AP system cores (Cortex-A53 and Cortex-A57) can be powered off by executing the WFI instruction. Similarly, power of Arm CPUs can be resumed either by controlling the APMU (Advanced Power Management Unit) registers or by an IRQ or FIQ interrupt.

For detail of power control by APMU registers, see section 13, Advanced Power Management Unit for AP-System Core (APMU).

— (14-74 page none)

(1) Power Control by WFI Instruction and Interrupts

The power shutdown by the WFI instruction is performed only when Cortex-A57/ Cortex-A53 CPUn power status control register (CA57CPUnCR, CA53CPUnCR) are in the core standby mode. In case of other setting, power shutdown sequence is not activated by the WFI instruction. See section 13, Advanced Power Management Unit for AP-System Core (APMU).
Power can be resumed by an IRQ or FIQ interrupt on the Arm core. After resuming power of Cortex-A57, Cortex-A53, CPUs by IRQ/FIQ, read the value of SYSCEERSR, SYSCEERSR 2, and SYSCEERSR3 registers. Without reading those registers after power-resuming, the shutdown sequence of related CPUs will not start.

[Description]

The 3rd column of the Table 14.6 Initial state of power domains (RZ/G2E) is deleted. And the Table 14.7 Initial state of power domains (RZ/G2N) is added.

[Reason for Correction]

To clarify the specification, initial state of power domain of RZ/G2N was added.
Initial boot power domain of RZ/G2E without core name was deleted to clarify the table.

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