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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0075A/E	Rev.	1.00
Title	RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N and RZ/G2E Specification Changes for CSI2.		Information Category	Technical Notification		
Applicable Product	RZ/G Series, 2nd Generation RZ/G2H, G2M V1.3, G2M V3.0, G2N and G2E	Lot No. All lots	Reference Document	RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.01 (R01UH0808EJ0101)		

This technical update describes specification changes of RZ/G Series, 2nd Generation product.

[Summary]

Specification changes for “RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.01”.

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Products]

RZ/G2H

RZ/G2M V1.3

RZ/G2M V3.0

RZ/G2N

RZ/G2E

[Section number and title]

29. CSI2

[Correction]

1. Section 29. CSI2, Page 29-33, 29.2.13 Interrupt Source Mask Register (INTCLOSE). Added Note of RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N and RZ/G2E.

Current (from):

Bit	Bit Name	Initial Value	R/W	Description
4	ICL[4]	B'0	R/W	Interrupt 4 (INT_ERRSOTHS) source mask 0: Enables the interrupt source. 1: Masks the interrupt source.
3	ICL[3]	B'0	R/W	Interrupt 3 (INT_ERRSOTSYNCHS) source mask 0: Enables the interrupt source. 1: Masks the interrupt source.
2	ICL[2]	B'0	R/W	Interrupt 2 (INT_ERRESC) source mask 0: Enables the interrupt source. 1: Masks the interrupt source.
1	—	B'0	R	Reserved This bit is always read as 0. The write value should always be 0.
0	ICL[0]	B'0	R/W	Interrupt 0 (INT_ERRCONTROL) source mask 0: Enables the interrupt source. 1: Masks the interrupt source.

Note: The settings of this register are applied the instant the register is set (immediate reflection).

Correction (to):

Bit	Bit Name	Initial Value	R/W	Description
4	ICL[4]	B'0	R/W	Interrupt 4 (INT_ERRSOTHS) source mask 0: Enables the interrupt source. 1: Masks the interrupt source.
3	ICL[3]	B'0	R/W	Interrupt 3 (INT_ERRSOTSYNCHS) source mask 0: Enables the interrupt source. 1: Masks the interrupt source.
2	ICL[2]	B'0	R/W	Interrupt 2 (INT_ERRESC) source mask 0: Enables the interrupt source. 1: Masks the interrupt source.
1	—	B'0	R	Reserved This bit is always read as 0. The write value should always be 0.
0	ICL[0]	B'0	R/W	Interrupt 0 (INT_ERRCONTROL) source mask 0: Enables the interrupt source. 1: Masks the interrupt source.

Note: The settings of this register are applied the instant the register is set (immediate reflection).

The settings of this register are optional. When INTCLOSE is set, the following sequence is recommended before "Start of PHY" operation.

1. Set INTCLOSE
2. Clear INTSTATE and INTERRSTATE
3. Set INTEN

[Description]

Supplementary explanation.

[Reason for Correction]

Addition of description for clarification.

2. Section 29. CSI2, Page 29-99, 29.3.8 Initial Setting of PHY. Subsection of “29.3.8.1 Terminology” was added for RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N and RZ/G2E.

Correction (from):

To initially set the PHY IP, the TESTCLR bit in the PHY test interface clear register must be cleared to 0.

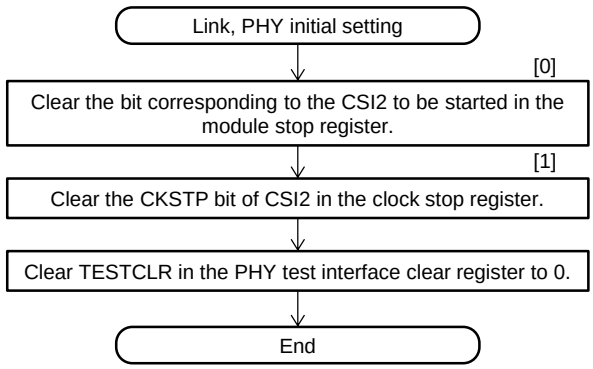

Figure 29.16 Example of PHY Initial Setting Procedure

Correction (to):

To initially set the PHY IP, the TESTCLR bit in the PHY test interface clear register must be cleared to 0.

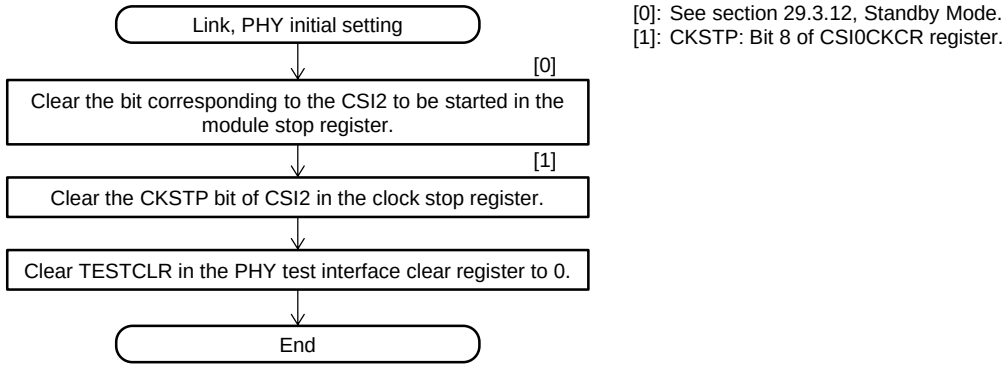

Figure 29.16 Example of PHY Initial Setting Procedure

29.3.8.1 Terminology

This section explains the terminology for CSI2.

Start of PHY

Initialization of CSI-2 receiver module. After initialization, CSI-2 receiver module expects that CSI-2 transmitter device stays StopState (LP-11).

Start of camera side device

Initialization of CSI-2 transmitter device. After initialization, CSI-2 transmitter device keeps StopState (LP-11).

Confirmation of PHY start

CSI-2 receiver module confirms that CSI-2 transmitter device stays StopState (LP-11) after initialization.

Start data transfer

CSI-2 transmitter device starts to send high-speed data to CSI-2 receiver module.

[Description]

Supplementary explanation.

[Reason for Correction]

Addition of description for clarification.

3. Section 29. CSI2, Page 29-106, 29.3.9 PHY Control and Monitoring through Register Setting.

Table 29.9 HSFREQRANGE Bit Set Values (RZ/G2H, RZ/G2N) was corrected.

Correction (from):

Table 29.9 HSFREQRANGE Bit Set Values (RZ/G2H, RZ/G2N)

Range (Mbps)	Default Bit Rate (Mbps)	HSFREQRANGE [6:0]	Range (Mbps)	Default Bit Rate (Mbps)	HSFREQRANGE [6:0]
80 - 97.125	80	B’000_0000	463.125 - 538.125	500	B’010_0110
80 - 107.625	90	B’001_0000	498.75 - 590.625	550	B’011_0111
83.125 - 118.125	100	B’010_0000	558.125 - 643.125	600	B’000_0111
92.625 - 128.625	110	B’011_0000	605.625 - 695.625	650	B’001_1000
102.12 - 139.125	120	B’000_0001	653.125 - 748.125	700	B’010_1000
111.62 - 149.625	130	B’001_0001	700.625 - 800.625	750	B’011_1001
121.12 - 160.125	140	B’010_0001	748.125 - 853.125	800	B’000_1001
130.625 - 170.625	150	B’011_0001	795.625 - 905.625	850	B’001_1001
140.125 - 181.125	160	B’000_0010	843.125 - 958.125	900	B’010_1001
149.625 - 191.625	170	B’001_0010	890.625 - 1010.625	950	B’011_1010
159.125 - 202.125	180	B’010_0010	938.125 - 1063.125	1000	B’000_1010
168.625 - 212.625	190	B’011_0010	985.625 - 1115.625	1050	B’001_1010
182.875 - 228.375	205	B’000_0011	1033.125 - 1168.125	1100	B’010_1010
197.125 - 224.125	220	B’001_0011	1080.625 - 1220.625	1150	B’011_1011
211.375 - 259.875	235	B’010_0011	1128.125 - 1273.125	1200	B’000_1011
225.625 - 275.625	250	B’011_0011	1175.625 - 1325.625	1250	B’001_1011
249.375 - 301.875	275	B’000_0100	1211.25 - 1378.125	1300	B’010_1011
273.125 - 328.125	300	B’001_0100	1270.625 - 1430.625	1350	B’011_1100
296.875 - 354.375	325	B’010_0101	1318.125 - 1483.125	1400	B’000_1100
320.625 - 380.625	350	B’011_0101	1365.625 - 1500.00	1450	B’001_1100
368.125 - 433.125	400	B’000_0101	1413.125 - 1500.000	1500	B’010_1100
415.125 - 485.125	450	B’001_0110			

Note: Must set the values above in HSFREQRANGE.

Correction (to):

Table 29.9 HSFREQRANGE Bit Set Values (RZ/G2H, RZ/G2N)

Range (Mbps)	Default Bit Rate (Mbps)	HSFREQRANGE [6:0]	Range (Mbps)	Default Bit Rate (Mbps)	HSFREQRANGE [6:0]
80 - 97.125	80	B’000_0000	463.125 - 538.125	500	B’010_0110
80 - 107.625	90	B’001_0000	498.75 - 590.625	550	B’011_0111
83.125 - 118.125	100	B’010_0000	558.125 - 643.125	600	B’000_0111
92.625 - 128.625	110	B’011_0000	605.625 - 695.625	650	B’001_1000
102.12 - 139.125	120	B’000_0001	653.125 - 748.125	700	B’010_1000
111.62 - 149.625	130	B’001_0001	700.625 - 800.625	750	B’011_1001
121.12 - 160.125	140	B’010_0001	748.125 - 853.125	800	B’000_1001
130.625 - 170.625	150	B’011_0001	795.625 - 905.625	850	B’001_1001
140.125 - 181.125	160	B’000_0010	843.125 - 958.125	900	B’010_1001
149.625 - 191.625	170	B’001_0010	890.625 - 1010.625	950	B’011_1010
159.125 - 202.125	180	B’010_0010	938.125 - 1063.125	1000	B’000_1010
168.625 - 212.625	190	B’011_0010	985.625 - 1115.625	1050	B’001_1010
182.875 - 228.375	205	B’000_0011	1033.125 - 1168.125	1100	B’010_1010
197.125 - 244.125	220	B’001_0011	1080.625 - 1220.625	1150	B’011_1011
211.375 - 259.875	235	B’010_0011	1128.125 - 1273.125	1200	B’000_1011
225.625 - 275.625	250	B’011_0011	1175.625 - 1325.625	1250	B’001_1011
249.375 - 301.875	275	B’000_0100	1211.25 - 1378.125	1300	B’010_1011
273.125 - 328.125	300	B’001_0100	1270.625 - 1430.625	1350	B’011_1100
296.875 - 354.375	325	B’010_0101	1318.125 - 1483.125	1400	B’000_1100
320.625 - 380.625	350	B’011_0101	1365.625 - 1500.00	1450	B’001_1100
368.125 - 433.125	400	B’000_0101	1413.125 - 1500.000	1500	B’010_1100
415.125 - 485.125	450	B’001_0110			

Note: Must set the values above in HSFREQRANGE.

[Description]

Correction of frequency range.

[Reason for Correction]

General error correction.

- End of Document -