Date: Jun. 3, 2022

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0092A/E	Rev.	1.00
Title	RZ/G2H, G2M V1.3, V3.0, G2N and G2E Document corrections for Booting		Information Category	Technical Notification		
Applicable Product	RZ/G Series, 2nd Generation RZ/G2H RZ/G2M V1.3, V3.0 RZ/G2N RZ/G2E	Lot No. All lots	Reference Document	RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.10 (R01UH0808EJ0110)		

This technical update describes document correction of RZ/G Series, 2nd Generation product.

[Summary]

Document corrections for “RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.10”.

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Products]

RZ/G2H

RZ/G2M V1.3, V3.0

RZ/G2N

RZ/G2E

[Section number and title]

Section 24. Booting

“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. Section 24. Booting, Page 24-6, 24.1.2.6 USB download Mode Pins, USB VBUS of supporting for RZ/G2E is corrected.

Current (from):

24.1.2.6 USB Download Mode Pins

				RZ/G Series 2nd Generation			
				RZ/G2H	RZ/G2M V1.3 RZ/G2M V3.0	RZ/G2N	RZ/G2E
Name	**Pin Name**	**I/O**	**Function**				
USB D+ data	DP0	I/O	D+ Input/output of the on-chip transceiver. Connect this pin to the D+ pin of the USB bus.	√	—	√	√
USB D- data	DM0	I/O	D- Input/output of the on-chip transceiver. Connect this pin to the D- pin of the USB bus.	√	—	√	√
USB VBUS	VBUS0	I	Connect to USB VBUS with external 30kΩ±1% series resistor.	√	—	√	√

Correction (to):

24.1.2.6 USB Download Mode Pins

Name	Pin Name	I/O	Function	RZ/G Series 2nd Generation			
				RZ/G2H	RZ/G2M V1.3 RZ/G2M V3.0	RZ/G2N	RZ/G2E
USB D+ data	DP0	I/O	D+ Input/output of the on-chip transceiver. Connect this pin to the D+ pin of the USB bus.	√	—	√	√
USB D- data	DM0	I/O	D- Input/output of the on-chip transceiver. Connect this pin to the D- pin of the USB bus.	√	—	√	√
USB VBUS	VBUS0	I	Connect to USB VBUS with external 30kΩ±1% series resistor.	√	—	√	—

[Description]

Correction of USB VBUS supporting product, RZ/G2E is corrected.

[Reason for Correction]

Corrected the error because RZ/G2E don't support “USB Download Mode”.

[Correction]

2. Section 24. Booting, Page 24-12, 24.2.5 eMMC Using DMA Boot Sequence, Boot ROM size is corrected.

Current (from):

24.2.5 eMMC Using DMA Boot Sequence

1. The master boot processor jumps to H'EB10_0000 (RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N, RZ/G2E AArch32) or H'00_EB10_C000(RZ/G2M V1.3, RZ/G2M V3.0 AArch64) or H'00_EB11_2800 (RZ/G2H, RZ/G2N, RZ/G2E AArch64). The processor executes the instructions in Boot ROM and 3KB data are transferred from eMMC to System RAM using MMC's DMA with 512-Byte transfer size.
2. These 3KB data contain Boot parameters, address information and data size information of IPL.
3. The amount of data specified by data size information is transferred to System RAM. After the transfer, the master processor jumps to the address specified by address information of IPL.

If boot operation from partition 1 fails, switching from boot partition 1 to partition 2 (dual boot mode) is performed.

Note: eMMC device must meet the following conditions.

- eMMC device that conforms to JEDEC eMMC standard 4.4 or higher
- Set the EXT_CSD register byte179, PARTITION_CONFIG bit[6] = H'0(No boot acknowledge sent).
- Set the EXT_CSD register byte179, PARTITION_CONFIG bit[5:3] = H'1 (Boot Area partition1).
- Set the EXT_CSD register byte177, BOOT_BUS_CONDITIONS bit[4:3] = H'1(50MHz SDR).
- Set the EXT_CSD register byte177, BOOT_BUS_CONDITIONS bit[1:0] = H'2(x8 bus widths).
- eMMC device's IO voltage should be 1.8V.

Place the boot data in eMMC boot area Partition 1 and 2 if dual boot mode is used.

Correction (to):

24.2.5 eMMC Using DMA Boot Sequence

1. The master boot processor jumps to H'EB10_0000 (RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N, RZ/G2E AArch32) or H'00_EB10_C000(RZ/G2M V1.3, RZ/G2M V3.0 AArch64) or H'00_EB11_2800 (RZ/G2H, RZ/G2N, RZ/G2E AArch64). The processor executes the instructions in Boot ROM and 2KB data are transferred from eMMC to System RAM using MMC's DMA with 512-Byte transfer size.
2. These 2KB data contain Boot parameters, address information and data size information of IPL.
3. The amount of data specified by data size information is transferred to System RAM. After the transfer, the master processor jumps to the address specified by address information of IPL.

If boot operation from partition 1 fails, switching from boot partition 1 to partition 2 (dual boot mode) is performed.

Note: eMMC device must meet the following conditions.

- eMMC device that conforms to JEDEC eMMC standard 4.4 or higher
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- Set the EXT_CSD register byte179, PARTITION_CONFIG bit[5:3] = H'1 (Boot Area partition1).
- Set the EXT_CSD register byte177, BOOT_BUS_CONDITIONS bit[4:3] = H'1(50MHz SDR).
- Set the EXT_CSD register byte177, BOOT_BUS_CONDITIONS bit[1:0] = H'2(x8 bus widths).
- eMMC device's IO voltage should be 1.8V.
- Place the boot data in eMMC boot area Partition 1 and 2 if dual boot mode is used.

[Description]

Correction of transfer size.

[Reason for Correction]

General error correction.

[Correction]

3. Section 24. Booting, Page 24-14, 24.2.5 eMMC Using DMA Boot Sequence, Boot ROM size is corrected.

Current (from):

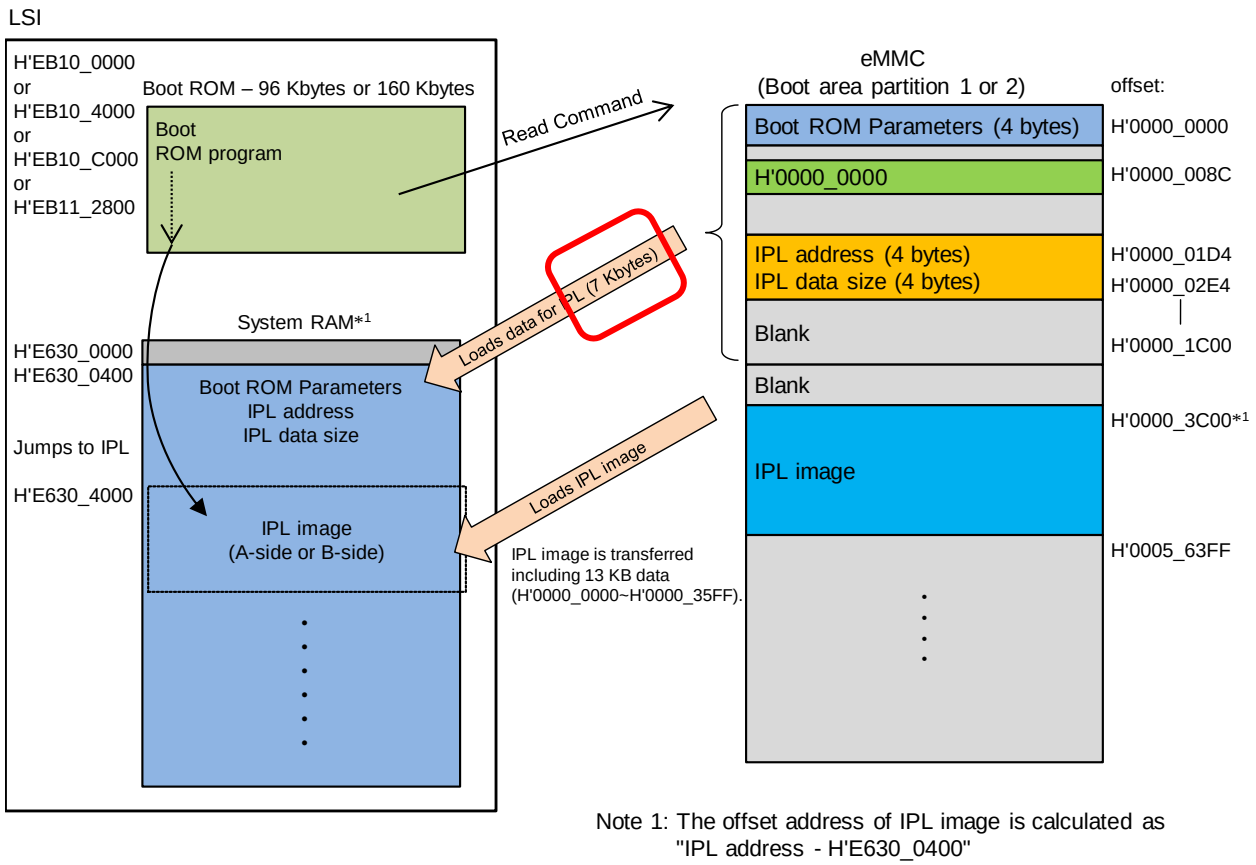

Figure 24.6 IPL transfer and Program image(eMMC)

Correction (to):

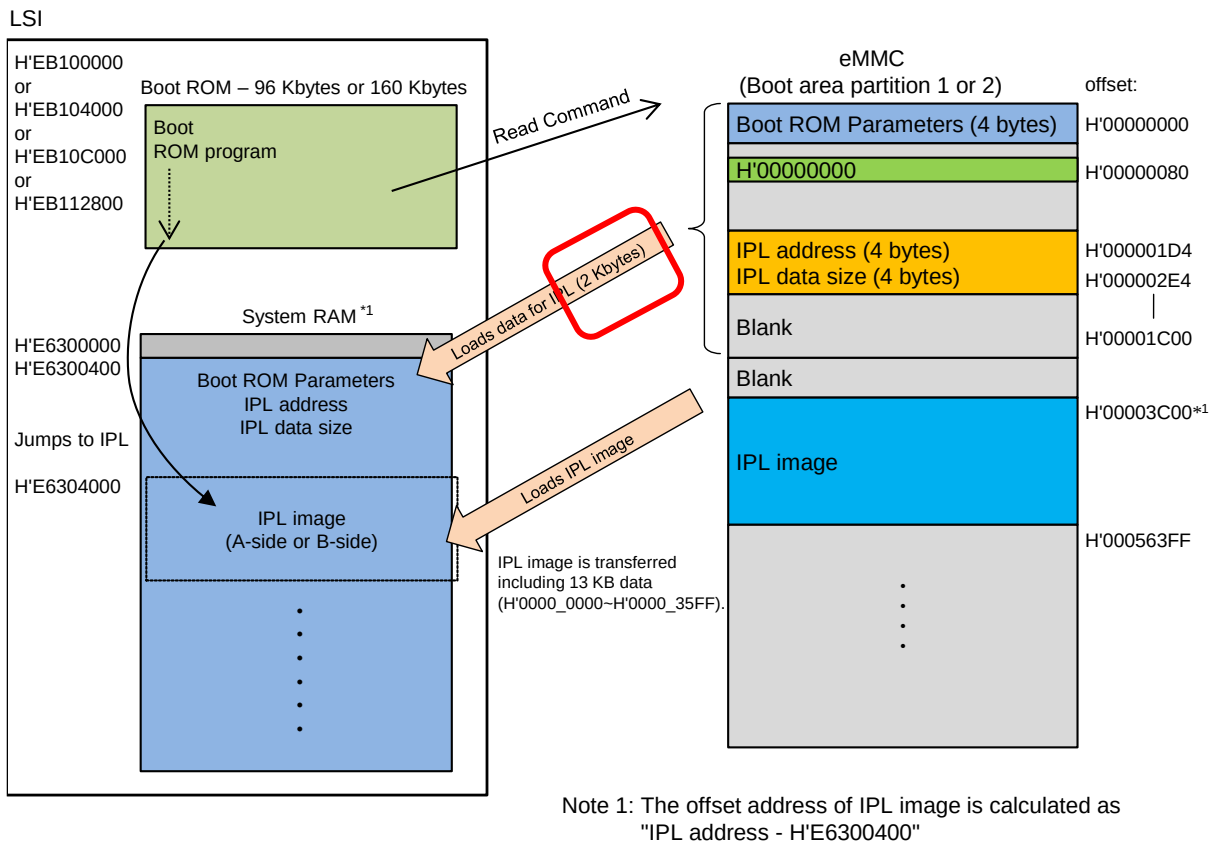

Figure 24.6 IPL transfer and Program image(eMMC)

[Description]

Correction of transfer size.

[Reason for Correction]

General error correction.

[Correction]

4. Section 24. Booting, Page 24-19, 24.3.1 IPL Address and Data Size Limitation. Clarified the IPL start address, and end address.

Current (from):

24.3 Usage Note

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

24.3.1 IPL Address and Data Size Limitation

The IPL end address can be calculated by IPL address and data size. It should be lower than the address below.

RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N: H'E635_67FF

RZ/G2E: H'E635_7FFF

The IPL address of HyperFlash and Serial Flash ROM boot requires 64-byte alignment. And the IPL address of eMMC boot requires 512-byte alignment.

24.3.2 Cleanup

Before jumping to the IPL, Boot ROM program cleans hardware registers used for loading the IPL and the master boot processor, as listed below.

AArch32 Cortex-A57/Cortex-A53

— Disable I-cache.

AArch64 Cortex-A57/Cortex-A53

— SYS-DMAC registers are set to hardware initial value.
— Disables Stack Alignment check. Disables Alignment fault checking. Disable I-cache.

Note

— The PFC setting is not cleared after jumping to the IPL.
— The settings of RPC-IF module for the transfer is automatically set by MD pin settings. Therefore, registers of RPC-IF module are not cleaned in Boot ROM.
— In the case of eMMC boot, initialize the SDHI interface registers.
— IRQ and FIQ are disabled.

Correction (to):

24.3 Usage Note

RZ/G2H
RZ/G2M V1.3 RZ/G2M V3.0
RZ/G2N RZ/G2E

24.3.1 IPL Address and Data Size Limitation

The IPL end address can be calculated by IPL address and data size. The IPL should be between IPL start address and end address below.

Product name	IPL start address	IPL end address
RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N	H'E630_2000	H'E635_7FFF
RZ/G2E	H'E630_2000	H'E631_7FFF

The IPL address of HyperFlash and Serial Flash ROM boot requires 64-byte alignment. And the IPL address of eMMC boot requires 512-byte alignment.

24.3.2 Cleanup

Before jumping to the IPL, Boot ROM program cleans hardware registers used for loading the IPL and the master boot processor, as listed below.

AArch32 Cortex-A57/Cortex-A53

— Disable I-cache.

AArch64 Cortex-A57/Cortex-A53

— SYS-DMAC registers are set to hardware initial value.
— Disables Stack Alignment check. Disables Alignment fault checking. Disable I-cache.

Note

— The PFC setting is not cleared after jumping to the IPL.
— The settings of RPC-IF module for the transfer is automatically set by MD pin settings. Therefore, registers of RPC-IF module are not cleaned in Boot ROM.
— In the case of eMMC boot, initialize the SDHI interface registers.
— IRQ and FIQ are disabled.

[Description]

Correction of IPL end address and addition of IPL start address.

[Reason for Correction]

Clarified the address range of the initial program loader area to avoid misunderstanding of users.

- End of Document -