# **RENESAS TECHNICAL UPDATE**

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Product Category	MPU/MCU	Document No.	TN-RZ*-A0093A/E	Rev.	1.00					
Title	RZ/G2H, G2M V1.3, G2M V3.0, G2N and G2 Document Correction for DU	?E	Information Category	Technical Notification						
Applicable Product	RZ/G Series, 2nd Generation RZ/G2H RZ/G2M V1.3, V3.0 RZ/G2N RZ/G2E	Lot No. All lots	Reference Document	RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.10 (R01UH0808EJ0110)						
This technica	I update describes document correction of RZ	/G Series, 2i	nd Generation p	roduct.						
[Summary]										
Document co	rrection for"RZ/G Series, 2nd Generation User	r's Manual: H	lardware Rev.1	.10".						
[Priority level]	]									
Importance: "	'Normal"									
Urgency: "No	rmal"									
[Products]										
RZ/G2H	3 \/3 0									
RZ/G2N										
RZ/G2E										
[Section number and title]										
Section 36. DU										



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(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)



#### [Correction]

 Section 36. Booting, Page 36-81, 36.2.2 Display Timing Generation Registers. (3) Vertical Display Start Register n (VDSRn) is corrected. RZ/G2E limitation is removed.

Current (from):

## (2) Horizontal Display End Register n (HDERn)

Address: DU0: H'FEB0\_0044, DU1: H'FEB3\_0044, DU2: H'FEB4\_0044, DU3: H'FEB7\_0044

Initial value:       -	Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Initial value:       A		_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_
NVX         R	Initial value:				_	_		_		_	_		_	_	L	_	
Bit         15         14         13         12         11         10         9         8         7         6         5         4         3         2         1         0           Internal ROW:         R	R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value:         -         -         -         -         HDE           Bit         R	Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value       Imital value       R       R       R       R       R       R/W		_	_	_							HDE						
Bit       Initial       R/W       Internal       Update       Description         31 to 13       -       -       R       -       Reserved         12 to 0       HDE       -       R       -       Reserved         12 to 0       HDE       -       R/W       Available       Horizontal Display End         12 to 0       HDE       -       R/W       Available       Horizontal Display End         To enable bit 11, set the DEFE5 bit in DEF5Rm to 1. In the initial state, bit 12 cannot be written to.       To enable bit 12, set the DEFE10 bit in DEF10Rm to 1. In the initial state, bit 12 cannot be written to.         These bits are used to set the horizontal display end position in dot clock units.       These bits are used to set the horizontal display end position in dot clock units.         Address:       DU0: HFEB0_0048, DU1: HFEB3_0048, DU2: HFEB4_0048, DU3: HFEB7_0048         Bit:       31 30       29       28       27       26       24       23       22       21       20       19       18       17       16         Initial value:       -	Initial value:	— R	— R					— R/W									
Bit         Name         Value         R/W         Update         Description           31 to 13         -         -         R         -         Reserved The read value is undefined. The write value should always be 0.           12 to 0         HDE         -         R/W         Available         Horizontal Display End To enable bit 11, set the DEFE5 bit in DEF50m to 1. In the initial state, bit 12 cannot be written to. To enable bit 12, set the DEFE10 bit in DEF10Rm to 1. In the initial state, bit 12 cannot be written to. These bits are used to set the horizontal display end position in dot clock units.           30         Vertical Display Extr Register n (VDSR)           Address:         DU0: HFEB0_0048, DU1: HFEB3_0048, DU2: HFEB4_0048, DU3: HFEB7_0048           Bit:         31         30         29         28         27         26         25         24         23         22         21         20         19         18         17         16           -	10.00	Bit	IX.	Initial	10,00	10,00	Internal	10,00	10,00	10.00	1011	10,00	10,00	10,00	10,00	10,00	10/00
31 to 13       -       R       -       Reserved The read value is undefined. The write value should always be 0.         12 to 0       HDE       -       R/W       Available       Horizontal Display End To enable bit 11, set the DEFES bit in DEF10Rm to 1. In the initial state, bit 12 cannot be written to. To enable bit 12, set the DEFE10 bit in DEF10Rm to 1. In the initial state, bit 12 cannot be written to. These bits are used to set the horizontal display end position in dot clock units. The set value is retained at a reset.         30       Vertical Display Start Register n (VDSRn)         Address:       DU0: HFEB0_0048, DU1: HFEB3_0048, DU2: HFEB4_0048, DU3: HFEB7_0048         Bit       31       30       29       28       27       26       25       24       23       22       21       0       18       17       16         Initial value:       - <td>Bit</td> <td>Nam</td> <td>ne</td> <td>Value</td> <td>R/W</td> <td>1</td> <td>Update</td> <td>De</td> <td>scripti</td> <td>on</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>	Bit	Nam	ne	Value	R/W	1	Update	De	scripti	on							
The read value is undefined. The write value should always be 0.         12 to 0       HDE       -       R/W       Available       Horizontal Display End         12 to 0       HDE       -       R/W       Available       To enable bit 11, set the DEFE5 bit in DEF5Rm to 1. In the initial state, bit 11 cannot be written to. To enable bit 12, set the DEFE10 bit in DEF10Rm to 1. In the initial state, bit 12 cannot be written to. These bits are used to set the horizontal display end position in dot clock units. The set value is retained at a reset.         (3)       Vertical Display Start Register n (VDSRn)         Address:       DU0: H/FEB0_0048, DU1: H/FEB3_0048, DU2: H/FEB4_0048, DU3: H/FEB7_0048         Bit:       31       30       29       28       27       26       25       24       23       22       21       20       19       18       17       16         Initial value:       - <td>31 to 13</td> <td>—</td> <td></td> <td>_</td> <td>R</td> <td></td> <td>_</td> <td>Re</td> <td>served</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>	31 to 13	—		_	R		_	Re	served								
12 10 0       HDE       -       R/W       Available       Horzontal Display End         To enable bit 11, set the DEFE5 bit in DEF10Rm to 1. In the initial state, bit 12 cannot be written to.       To enable bit 12, set the DEFE10 bit in DEF10Rm to 1. In the initial state, bit 12 cannot be written to.         These bits are used to set the horizontal display end position in dot clock units.       The set value is retained at a reset.         (3)       Vertical Display Start Register n (VDSRn)         Address: DU0: H'FEB0_0048, DU1: H'FEB3_0048, DU2: H'FEB4_0048, DU3: H'FEB7_0048         Bit:       31       30       29       28       27       26       25       24       23       22       21       20       19       18       17       16         -	101 0						A		e read	value is	s undef	ined. Tł	ne write	e value	should	always	be 0.
To enable bit 11, set the DEFES bit in DEF50km to 1. In the initial state, bit 11 cannot be written to. To enable bit 12, set the DEFE10 bit in DEF10Rm to 1. In the initial state, bit 12 cannot be written to. These bits are used to set the horizontal display end position in dot clock units. The set value is retained at a reset.         (3) Vertical Display Start Register n (VDSR)         Address: DU0: HFEB0_0048, DU1: HFEB3_0048, DU2: HFEB4_0048, DU3: HFEB7_0048         Bit:         31       30       29       28       27       26       25       24       23       22       21       20       19       18       17       16         Initial value:         Bit:       31       30       29       28       27       26       25       24       23       22       21       20       19       18       17       16         Initial value:       -       <	12 to 0	HDE			R/W		Available	e Ho	rizonta	l Displa	y End	DEEE	<b>F b</b> 14 1.4	DEEE	<b>)</b> (	La tha	
Bit       31       30       29       28       27       26       25       24       23       22       21       20       19       18       17       16         Address:       DU0:       H'FEB0_0048, DU1:       H'FEB3_0048, DU2:       H'FEB4_0048, DU3:       H'FEB7_0048         Bit       31       30       29       28       27       26       25       24       23       22       21       20       19       18       17       16         Initial value:       - <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>10 sta</td> <td>enable</td> <td>DIT 11, 11 cann</td> <td>set the</td> <td>UEFE</td> <td>5 dit in</td> <td>DEF5F</td> <td>Cm to 1</td> <td>. In the</td> <td>Initial</td>								10 sta	enable	DIT 11, 11 cann	set the	UEFE	5 dit in	DEF5F	Cm to 1	. In the	Initial
Initial state, bit 12 cannot be written to.         These bits are used to set the horizontal display end position in dot clock units.         The set value is retained at a reset.         (3) Vertical Display Start Register n (VDSRn)         Address: DU0: H'FEB0_0048, DU1: H'FEB3_0048, DU2: H'FEB4_0048, DU3: H'FEB7_0048         Bit:       31       30       29       28       27       26       25       24       23       22       21       20       19       18       17       16         Initial value:       -       -       -       -       -       -       -       -       -         Initial value:       -								To	enable	hit 12	set the		0. 10 hit iı		0Rm to	1 In ti	he
These bits are used to set the horizontal display end position in dot clock units. The set value is retained at a reset. 3. Vertical Display Start Register n (VDSR) Address: DU0: H'FEB0_0048, DU1: H'FEB3_0048, DU2: H'FEB4_0048, DU3: H'FEB7_0048 Bit <u>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16</u> <u> </u>								init	tial state	e. bit 12	2 canno	t be wr	itten to			, i. iii u	
dot clock units. The set value is retained at a reset.         (3) Vertical Display Start Register n (VDSRn)         Address:       DU0: H'FEB0_0048, DU1: H'FEB3_0048, DU2: H'FEB4_0048, DU3: H'FEB7_0048         Bit:       31       30       29       28       27       26       25       24       23       22       21       20       19       18       17       16         Initial value:       -								Th	ese bits	s are us	sed to s	et the h	norizon	tal disp	lav end	l positio	on in
The set value is retained at a reset.         (J) Vertical Display Start Register n (VDSRn)         Address: DU0: HIFEB0_0048, DU1: HIFEB3_0048, DU2: HIFEB4_0048, DU3: HIFEB7_0048         Bit:       31       30       29       28       27       26       25       24       23       22       21       20       19       18       17       16       -       -         Bit:       31 10       10       -       Reserved         The read value is undefined. The write value should always be 0.         8 to 0       VDS       -         NUCS       -       Reserved         The read value is undefined. The write value should always be 0.       Reserved         The read value is retained at a reset.       VDS         -       Reserved         The read value is retained of a reset.       VDS should be set to 1 or greater.								do	t clock	units.					,		
Vertical Display Start Register n (VDSRn)         Address: DU0: HFEB0_0048, DU1: HFEB3_0048, DU2: HFEB4_0048, DU3: HFEB7_0048         Bit:       31       30       29       28       27       26       25       24       23       22       21       20       19       18       17       16         Initial value:       - <t< td=""><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>Th</td><td>e set va</td><td>alue is i</td><td>retained</td><td>d at a re</td><td>eset.</td><td></td><td></td><td></td><td></td></t<>								Th	e set va	alue is i	retained	d at a re	eset.				
Address: DU0: H'FEB0_0048, DU1: H'FEB3_0048, DU2: H'FEB4_0048, DU3: H'FEB7_0048         Bit:       31       30       29       28       27       26       25       24       23       22       21       20       19       18       17       16         Initial value:       -       <	(3) Ve	rtical I	Displa	y Start	Registe	r n ('	VDSRn)										
Initial value:       -	Address: I Bit:	31 31	FEB0 <u>.</u> 30	_0048, [ 	28	27	_0048, D 	25 U2: H	FEB4_( 24	23	22	FEB7_( 21	20 20	19	18	17	16
Initial value:       -				—	—	—	—	—	—	—	-	-	-	—	—	-	_
R/W:       R	Initial value:	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_
Bit:       15       14       13       12       11       10       9       8       7       6       5       4       3       2       1       0         Initial value:       -       -       -       -       -       -       -       VDS         Initial value:       -<	R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value:       Image: Initial value: <td>Bit:</td> <td>15</td> <td>14</td> <td>13</td> <td>12</td> <td>11</td> <td>10</td> <td>9</td> <td>8</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td>	Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:		_		—	—	_	—	—		1	1	1	VDS	1	1	1	1
BitBit NameInitial ValueR/WInternal UpdateDescription31 to 9RReserved The read value is undefined. The write value should always be 0.8 to 0VDSR/WAvailableVertical Display Start These bits are used to set the vertical display start position in raster line units. The set value is retained at a reset. VDS should be set to 1 or greater.	Initial value: R/W:	— R	 R	— R	 R	R	— R	 R	— R/W	 R/W	 R/W	 R/W	 R/W	 R/W	 R/W	 R/W	 R/W
31 to 9       -       R       -       Reserved The read value is undefined. The write value should always be 0.         8 to 0       VDS       -       R/W       Available       Vertical Display Start These bits are used to set the vertical display start position in raster line units. The set value is retained at a reset. VDS should be set to 1 or greater.	Bit	Bit Na	ime	Initial Value	R/W		Internal Update	De	scriptio	on							
8 to 0       VDS       —       R/W       Available       Vertical Display Start         These bits are used to set the vertical display start position in raster line units.       The set value is retained at a reset.       VDS should be set to 1 or greater.	31 to 9	_		_	R	-	_	Re	served								
8 to 0 VDS — R/W Available Vertical Display Start These bits are used to set the vertical display start position in raster line units. The set value is retained at a reset. VDS should be set to 1 or greater.								The	e read v	alue is	undefi	ned. Th	ne write	value	should	always	be 0.
These bits are used to set the vertical display start position in raster line units. The set value is retained at a reset. VDS should be set to 1 or greater.	8 to 0	VDS			R/W	4	Available	e Vei	rtical Di	splay S	Start						
raster line units. The set value is retained at a reset. VDS should be set to 1 or greater.								The	ese bits	are us	ed to s	et the v	ertical	display	start po	osition i	in
The set value is retained at a reset. VDS should be set to 1 or greater.								ras	ter line	units.							
								The	e set va	lue is r	etainec	l at a re	eset.				
									<b>NO SHOU</b>	iiu be s		u yiea					
								VL	5 5100			or grea					



Correction (to):

# (2) Horizontal Display End Register n (HDERn)

## Address: DU0: H'FEB0\_0044, DU1: H'FEB3\_0044, DU2: H'FEB4\_0044, DU3: H'FEB7\_0044

Initial value:	— — R	— — R	_	_	—	—	_	-	_	_	_	_	_	_	_	_
Initial value:	 R	— R	I			1										
R/W: Bit:	R	R				_	_	_	_	_	_		_	_	_	_
Bit:			R	R	R	R	R	R	R	R	R	R	R	R	R	R
-	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	_	_	—							HDE						
nitial value:	— R	— R	 R	 R/W	 R/W		 R/W		 R/W	 R/W	 R/W	 R/W	 R/W	 R/W	 R/W	 R/W
Rit	Bit Namo		Initial Value	D/M	l	Internal	Do	scripti	n							
31 to 13				R			Re	served	511							
							Th	e read	/alue is	undefi	ned. Tł	ne write	value	should	always	be 0
12 to 0	HDE	-	_	R/W		Available	e Ho	rizontal	Displa	y End					,	
							То	enable	bit 11,	set the	DEFE	5 bit in	DEF5F	Rm to 1.	In the	initial
							sta	ite, bit 1	1 cann	ot be w	ritten to	э.				
							То	enable	bit 12,	set the	DEFE	10 bit ir	n DEF1	0Rm to	1. In th	ne
							init	ial state	e, bit 12	canno	t be wr	itten to				
							Th	ese bits	are us	ed to s	et the h	norizon	tal disp	lay end	positio	n in
							doi	t clock I	units.							
) <del>.</del>	1.0.	,	<u> </u>		/-		۱h	e set va	aue is r	etained	at a re	eset.				
5) veru	cal DI	spiay	Start	Registe	г <b>п</b> ( <b>v</b>	DSKII)										
ddress: DU	10: H'F	EB0_	.0048, C	0U1: H'F	EB3_	0048, D	0U2: H'	FEB4_(	048, D	0U3: H'F	EB7_0	048				
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	_	—	—	—	—	—	—		—	—	—	—	—		—
nitial value:	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	—	_	—	—	_	—	_					VDS	1	1	1	1
nitial value: R/W:	— R	R	R	R	R	R	 R	 R/W	R/W	 R/W	 R/W	 R/W	 R/W	 R/W	 R/W	R/W
Bit Bi	it Nam		Initial Value	R/W	l	nternal	De	scrintic	'n							
21 to 0	it itali		value	D		puale	De									
31109 —	-	-	_	ĸ	_	_	Re: The	served e read v	alue is	undefir	ned. Th	e write	values	should a	alwavs	be 0.
8 to 0 VI	DS		_	R/W	A	vailable	e Ver	rtical Di	splav S	tart			Value (		amayo	
						The	These bits are used to set the vertical display start position in									
							The		units. Iucis ri	hanicte	at a ro	sot				
							\//h	en the	SCM hi	its in D	SYSRn	are B'	10 and	B'11 \/	DS sho	hluc
							be RZ	set to 1 /G2N1	or grea	ater [RZ	Z/G2H,	RZ/G2	M V1.3	, RZ/G2	2M V3.0	0,



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(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)



### [Description]

Add Scan Mode condition to VDS restriction.

[Reason for Correction]

When Scan Mode is Non-interlaced mode, can be displayed even if VDS is 0.

Therefore, "VDS should be set to 1 or greater" restriction is only for Interlace sync mode (the SCM bits in DSYSRn are B'10) and Interlace sync & video mode (the SCM bits in DSYSRn are B'11).

Since RZ/G2E can only specify Non-interlaced mode, "VDS should be set to 1 or greater" restriction is out of scope.



#### [Correction]

 Section 36. Booting, Page 36-150, 36.3.10 Display Timing Generation, Correspondence Table of Settings of Display Timing Generation Registers, Note 3 is corrected. RZ/G2E limitation is removed.

Current (from):

## Table 36.34 Correspondence Table of Settings of Display Timing Generation Registers

		Synchronization Method						
Register Name	Bit Name	Master Mode	TV Sync Mode					
Horizontal display start register n (HDSRn)	HDS*6	hsw + xs – 19* <sup>5</sup>	hsw + xs – 25* <sup>2*5</sup>					
Horizontal display end register n (HDERn)	HDE	hsw + xs – 19* <sup>5</sup> + xw	hsw + xs – 25 + xw <sup>*2*5</sup>					
Vertical display start register n (VDSRn)	VDS	ys – 2* <sup>3</sup>	ys – 2* <sup>3</sup>					
Vertical display end register n (VDERn)	VDE	ys – 2 + yw	ys – 2 + yw					
Horizontal synch width register n (HSWRn)	HSW	hsw – 1	hsw – 1					
Horizontal cycle register n (HCRn)	HC	hc – 1	hc – 1					
Vertical synch point register n (VSPRn)	VSP	vc – vsw – 1	vc – vsw – 1					
Vertical cycle register n (VCRn)	VC	vc – 1	vc – 1					

Notes: 1. In all scan modes, VDS, VDE, VSP, VC settings are in single-field units.

2. The values of HDS and HDE are from the fourth rising edge of DCLKOUT after detection of the falling edge of EXHSYNC through the rising edge of DCLKOUT



- 3. VDS should be set to 1 or greater.
- 4. HC should be set so as to satisfy HC > HDE.
- 5. If the function below is used, the following correction value is subtracted from both HDS and HDE in Table 36.34.
- 6. HDS should be set to 1 or greater.
- When using the YC-RGB conversion function (YCRGB0 or YCRGB1 bits in DEF5Rm are set to 1), 3 should be subtracted.



Correction (to):

		Synchronization Method						
Register Name	Bit Name	Master Mode	TV Sync Mode					
Horizontal display start register n (HDSRn)	HDS*6	hsw + xs – 19* <sup>5</sup>	hsw + xs – 25* <sup>2*5</sup>					
Horizontal display end register n (HDERn)	HDE	hsw + xs – 19* <sup>5</sup> + xw	hsw + xs – 25 + xw <sup>*2*5</sup>					
Vertical display start register n (VDSRn)	VDS	ys – 2* <sup>3</sup>	ys – 2* <sup>3</sup>					
Vertical display end register n (VDERn)	VDE	ys – 2 + yw	ys – 2 + yw					
Horizontal synch width register n (HSWRn)	HSW	hsw – 1	hsw – 1					
Horizontal cycle register n (HCRn)	HC	hc – 1	hc – 1					
Vertical synch point register n (VSPRn)	VSP	vc – vsw – 1	vc – vsw – 1					
Vertical cycle register n (VCRn)	VC	vc - 1	vc – 1					

## Table 36.34 Correspondence Table of Settings of Display Timing Generation Registers

Notes: 1. In all scan modes, VDS, VDE, VSP, VC settings are in single-field units.

2. The values of HDS and HDE are from the fourth rising edge of DCLKOUT after detection of the falling edge of EXHSYNC through the rising edge of DCLKOUT



- 3. When the SCM bits in DSYSRn are B'10 and B'11, VDS should be set to 1 or greater [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N].
- 4. HC should be set so as to satisfy HC > HDE.
- 5. If the function below is used, the following correction value is subtracted from both HDS and HDE in Table 36.34.
- 6. HDS should be set to 1 or greater.
- When using the YC-RGB conversion function (YCRGB0 or YCRGB1 bits in DEF5Rm are set to 1), 3 should be subtracted.

Description]

Add Scan Mode condition to VDS restriction.

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and Interlace sync & video mode (the SCM bits in DSYSRn are B'11).

Since RZ/G2E can only specify Non-interlaced mode, "VDS should be set to 1 or greater" restriction is out of scope.

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