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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0105A/E	Rev.	1.00
Title	RZ/G2E Correction of section 26:External Bus Controller for LPDDR4/DDR3L SDRAM (DBSC4)		Information Category	Technical Notification		
Applicable Product	RZ/G Series, 2nd Generation RZ/G2E	Lot No. All lots	Reference Document	RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.10 (R01UH0808EJ0110)		

This technical update describes document correction of RZ/G Series, 2nd Generation product.

[Summary]

Correction of section 26:External Bus Controller for LPDDR4/DDR3L SDRAM (DBSC4)

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Product]

RZ/G2E

[section number and title]

26. External Bus Controller for LPDDR4/DDR3L SDRAM (DBSC4)

“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. Section 26, Page 26-10, 26.4 MRESET# pin level during DDR power-up, addition of the new section.

Current (from):

— (None)

Correction (to):

26.4 MRESET# pin level during DDR power-up

The pin level of MRESET# of RZ/G2E is undefined during DDR power-up as shown in Figure 26.5.

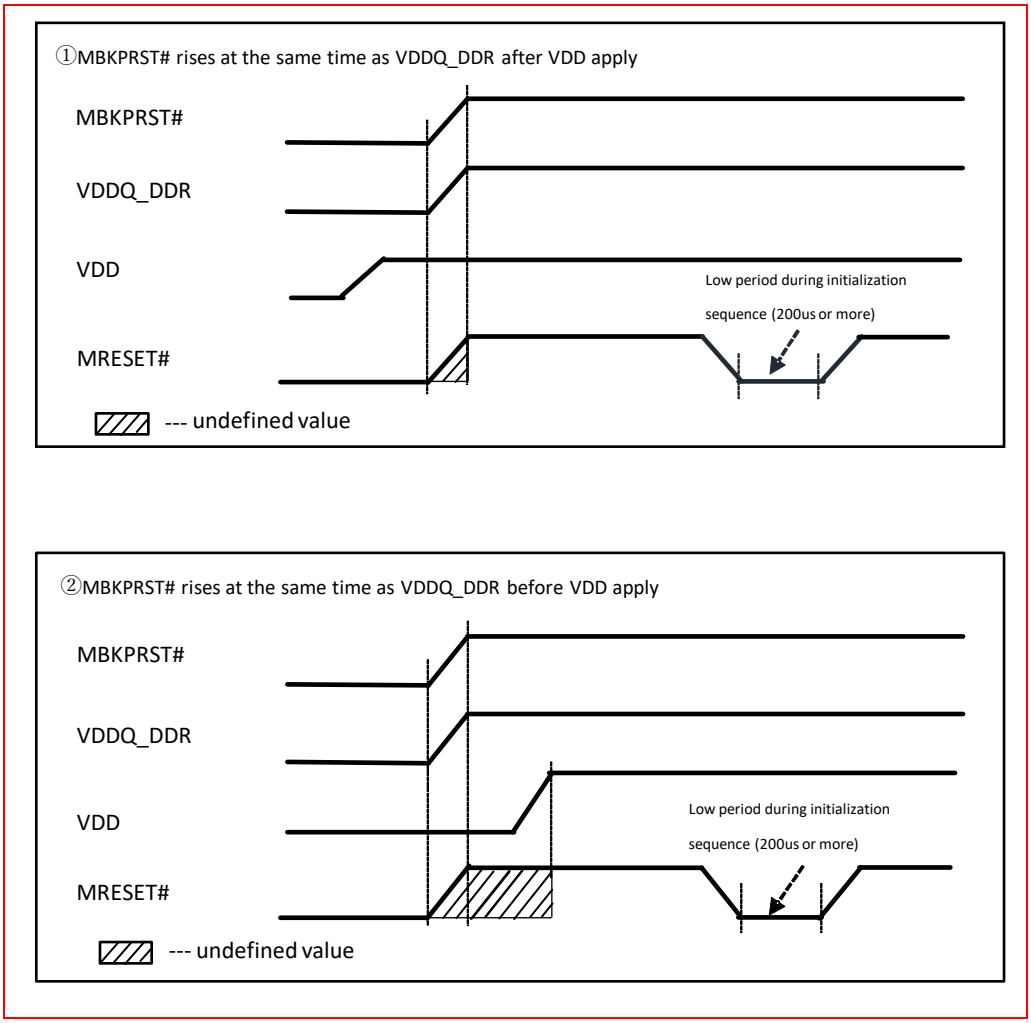

Figure 26.5 MRESET# pin level during DDR power-up

[Description]

MRESET# pin level during DDR power-up.

[Reason for Correction]

Caution for MRESET# pin level during DDR power-up.

- End of Document -

Caution for RESET pin status at DDR power-up

[Caution]

The DDR pins of RZ/G2E may become undefined during DDR power-up.

[Detail Explanation]

The JEDEC recommends (but does not require) that the controller drive RESET# to “Low” at power-ramp. On the other hand, the JEDEC specifies that the DRAM should initialize by driving RESET# Low after when the power supply is stable.

RZ/G2E is based on this specification that the DRAM should initialize by setting RESET# to Low after when the power supply is stable, so the pin level of MxRESET# (SOC pin connected into RESET#) is undefined when power ramp. Even in this case, we are considering it is not a problem according to the JEDEC standard since the MxRESET# pin goes Low to initialize the DRAM device in the SOC initialization sequence.

However, some memory suppliers' DRAM products have a condition that RESET# pin should be set as "Low" during power-ramp. When using these memory products, please make sure that RZ/G2E’s MxRESET# pin level specification matches your memory devices.