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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A020A/E	Rev.	1.00
Title	RZ/G Series User's Manual: Hardware Corrections (MSIOF)		Information Category	Technical Notification		
Applicable Product	RZ/G Series, RZ/G1H, M, N and E	Lot No. All lots	Reference Document	Refer to Table 1		

This technical update describes document corrections for RZ/G Series.

[Summary]

RZ/G Series User's Manual: Hardware Correction (manual errata)

[Products]

RZ/G1H, M, N and E

[Note]

There is no specification change (document correction only).

[Correction]

Gray highlighted parts (abcd) are corrected.

1. RZ/G Series

- Section 46.3.13 MSIOF FIFO Control Register (SIFCTR) [Page 46-28]

Descriptions of Bit 12 to 4 RFUA[8:0]

Current (from):

Indicate the number of words that can be transferred by the CPU or DMAC as B'0000000 (empty) to B'1000000 (full).

Correction (to):

Indicate the number of words that can be transferred by the CPU or DMAC as B'000000000 (empty) to B'010000000 (full).

2. RZ/G1H

- Section 1. Overview [Page 1-23]

Descriptions of Clock-synchronized serial interface with FIFO (MSIOF)

Current (from):

Internal 64-byte transmit FIFOs/internal 256-byte receive FIFOs

Correction (to):

Internal 64-stage transmit FIFOs/internal 128-stage receive FIFOs

3. RZ/G1M

- Section 1. Overview [Page 1-21]

Descriptions of Clock-synchronized serial interface with FIFO (MSIOF)

Current (from):

Internal 64-byte transmit FIFOs/internal 256-byte receive FIFOs

Correction (to):

Internal 64-stage transmit FIFOs/internal 128-stage receive FIFOs

4. RZ/G1N

- Section 1. Overview [Page 1-21]

Descriptions of Clock-synchronized serial interface with FIFO (MSIOF)

Current (from):

Internal 64-byte transmit FIFOs/internal 256-byte receive FIFOs

Correction (to):

Internal 64-stage transmit FIFOs/internal 128-stage receive FIFOs

5. RZ/G1E

- Section 1. Overview [Page 1-21]

Descriptions of Clock-synchronized serial interface with FIFO (MSIOF)

Current (from):

Internal 64-byte transmit FIFOs/internal 256-byte receive FIFOs

Correction (to):

Internal 64-stage transmit FIFOs/internal 128-stage receive FIFOs

[Reference Document]

Table 1 Reference Document

Products	Document Title or Category	Revision	Date
RZ/G Series	RZ/G Series User's Manual: Hardware	1.00	Sep. 30, 2016
RZ/G1H	RZ/G1H User's Manual: Hardware	1.00	Sep. 30, 2016
RZ/G1M	RZ/G1M User's Manual: Hardware	1.00	Sep. 30, 2016
RZ/G1N	RZ/G1N User's Manual: Hardware	1.00	Sep. 30, 2016
RZ/G1E	RZ/G1E User's Manual: Hardware	1.00	Sep. 30, 2016

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