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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A0242B/E	Rev.	2.00
Title	RX21A Group, RX220 Group Errata to User's Manual: Hardware Regarding the Realtime Clock (RTC)		Information Category	Technical Notification		
Applicable Product	RX21A Group, RX220 Group	Lot No. All	Reference Document	RX21A Group User's Manual: Hardware Rev.1.10 (R01UH0251EJ0110) RX220 Group User's Manual: Hardware Rev.1.10 (R01UH0292EJ0110)		

This document describes corrections to the "Realtime Clock (RTC)" chapter in User's Manual: Hardware for the applicable products.
Page and section numbers and the target registers for RTC software reset are based on the manual for the RX21A Group. Refer to the table on the last page for the corresponding page and section numbers in the RX220 Group.

• Page 744 of 1390

A note is added to the table in (1) In calendar count mode of section 26.2.18, RTC Control Register 2 (RCR2) as follows.

Before correction

26.2.18 RTC Control Register 2 (RCR2)

(1) In calendar count mode:

Address(es): 0008 C424h

	b7	b6	b5	b4	b3	b2	b1	b0
	CNTMD	HR24	AADJP	AADJE	RTCOE	ADJ30	RESET	START
Value after reset:	x	x	x	x	0	0	0	x

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	START	Start	0: Year, month, day-of-week, date, hour, minute, second, and 64-Hz counters, and prescaler are stopped. 1: Year, month, day-of-week, date, hour, minute, second, and 64-Hz counters, and prescaler operate normally.	R/W
b1	RESET	RTC Software Reset	• In writing 0: Writing is invalid. 1: The prescaler and the target registers are reset by RTC software reset. (R64CNT, RSECAR/BCNT0AR, RMINAR/BCNT1AR, RHRAR/BCNT2AR, RWKAR/BCNT3AR, RDAYAR/BCNT0AER, RMONAR/BCNT1AER, RYRAR/BCNT2AER, RYRAREN/BCNT3AER, RADJ, RTCCRy, RSECCPy/BCNT0CPy, RMINCPy/BCNT1CPy, RHRCPy/BCNT2CPy, RDAYCPy/BCNT3CPy, RMONCPy, RCR2.ADJ30, RCR2.AADJE, RCR2.AADJP) • In reading 0: In normal time operation, or an RTC software reset has completed. 1: During an RTC software reset	R/W
b2	ADJ30	30-Second Adjustment	• In writing 0: Writing is invalid. 1: 30-second adjustment is executed. • In reading 0: In normal time operation, or 30-second adjustment has completed. 1: During 30-second adjustment	R/W
b3	RTCOE	RTCOUT Output Enable	0: RTCOUT output disabled. 1: RTCOUT output enabled.	R/W
b4	AADJE	Automatic Adjustment Enable	0: Automatic adjustment is disabled. 1: Automatic adjustment is enabled.	R/W
b5	AADJP	Automatic Adjustment Period Select	0: The RADJ.ADJ[5:0] setting value is adjusted from the count value of the prescaler every minute. 1: The RADJ.ADJ[5:0] setting value is adjusted from the count value of the prescaler every 10 seconds.	R/W
b6	HR24	Hours Mode	0: The RTC operates in 12-hour mode. 1: The RTC operates in 24-hour mode.	R/W
b7	CNTMD	Count Mode Select	0: The calendar count mode. 1: The binary count mode.	R/W

After correction

26.2.18 RTC Control Register 2 (RCR2)

(1) In calendar count mode:

Address(es): 0008 C424h

	b7	b6	b5	b4	b3	b2	b1	b0
	CNTMD	HR24	AADJP	AADJE	RTCOE	ADJ30	RESET	START
Value after reset:	x	x	x	x	0	0	0	x

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	START	Start*1	0: Year, month, day-of-week, date, hour, minute, second, and 64-Hz counters, and prescaler are stopped. 1: Year, month, day-of-week, date, hour, minute, second, and 64-Hz counters, and prescaler operate normally.	R/W
b1	RESET	RTC Software Reset	• In writing 0: Writing is invalid. 1: The prescaler and the target registers are reset by RTC software reset. (R64CNT, RSECAR/BCNT0AR, RMINAR/BCNT1AR, RHRAR/BCNT2AR, RWKAR/BCNT3AR, RDAYAR/BCNT0AER, RMONAR/BCNT1AER, RYRAR/BCNT2AER, RYRAREN/BCNT3AER, RADJ, RTCCRy, RSECCPy/BCNT0CPy, RMINCPy/BCNT1CPy, RHRCPy/BCNT2CPy, RDAYCPy/BCNT3CPy, RMONCPy, RCR2.ADJ30, RCR2.AADJE, RCR2.AADJP) • In reading 0: In normal time operation, or an RTC software reset has completed. 1: During an RTC software reset	R/W
b2	ADJ30	30-Second Adjustment	• In writing 0: Writing is invalid. 1: 30-second adjustment is executed. • In reading 0: In normal time operation, or 30-second adjustment has completed. 1: During 30-second adjustment	R/W
b3	RTCOE	RTCOUT Output Enable	0: RTCOUT output disabled. 1: RTCOUT output enabled.	R/W
b4	AADJE	Automatic Adjustment Enable*1	0: Automatic adjustment is disabled. 1: Automatic adjustment is enabled.	R/W
b5	AADJP	Automatic Adjustment Period Select*1	0: The RADJ.ADJ[5:0] setting value is adjusted from the count value of the prescaler every minute. 1: The RADJ.ADJ[5:0] setting value is adjusted from the count value of the prescaler every 10 seconds.	R/W
b6	HR24	Hours Mode*1	0: The RTC operates in 12-hour mode. 1: The RTC operates in 24-hour mode.	R/W
b7	CNTMD	Count Mode Select*1	0: The calendar count mode. 1: The binary count mode.	R/W

Note 1. After writing to this bit, confirm that its value has actually changed before proceeding with further processing. Refer to section 26.6.5, Points for Caution when Writing to and Reading from Registers, regarding changes to the values of the AADJE, AADJP, and HR24 bits.

• Page 745 of 1390

Description of the CNTMD bit in section 26.2.18, RTC Control Register 2 (RCR2) is corrected as follows.

Before correction

CNTMD Bit (Count Mode Select)

This bit specifies whether the RTC count mode is operated in calendar count mode or in binary count mode.
After a new value is written to this bit, reflecting the value in the internal circuitry takes a certain amount of time. Read the bit to confirm whether a value written has actually been reflected.

After correction

CNTMD Bit (Count Mode Select)

This bit specifies whether the RTC count mode is operated in calendar count mode or in binary count mode.
After setting the count mode, execute an RTC software reset and start again from the initial settings.
The CNTMD bit is updated in synchronization with the count source, so when the value of the CNTMD bit has been changed, check that the value of the bit has actually been updated before applying the RTC software reset. The count mode changes to that which was specified beforehand in the CNTMD bit after the RTC software reset is applied.
For details on initial settings, refer to section 26.3.1, Outline of Initial Settings of Registers after Power-On.

• Page 746 of 1390

A note is added to the table in (2) In binary count mode of section 26.2.18, RTC Control Register 2 (RCR2) as follows.

Before correction

(2) In binary count mode:

Address(es): 0008 C424h

	b7	b6	b5	b4	b3	b2	b1	b0
	CNTMD	—	AADJP	AADJE	RTCOE	—	RESET	START
Value after reset:	x	x	x	x	0	0	0	x

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	START	Start	0: The 32-bit binary counter, 64-Hz counter, and prescaler are stopped. 1: The 32-bit binary counter, 64-Hz counter, and prescaler are in normal operation.	R/W
b1	RESET	RTC Software Reset	• In writing 0: Writing is invalid. 1: The prescaler and registers to be reset by RTC software are reset. (R64CNT, RSECAR/BCNT0AR, RMINAR/BCNT1AR, RHRAR/BCNT2AR, RWKAR/BCNT3AR, RDAYAR/BCNT0AER, RMONAR/BCNT1AER, RYRAR/BCNT2AER, RYRAREN/BCNT3AER, RADJ, RTCCRy, RSECCPy/BCNT0CPy, RMINCPy/BCNT1CPy, RHRCPy/BCNT2CPy, RDAYCPy/BCNT3CPy, RMONCPy, RCR2.ADJ30, RCR2.AADJE, RCR2.AADJP) • In reading 0: In normal time operation, or an RTC software reset has completed. 1: During an RTC software reset	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	RTCOE	RTCOUT Output Enable	0: RTCOUT output disabled. 1: RTCOUT output enabled.	R/W
b4	AADJE	Automatic Adjustment Enable	0: Automatic adjustment is disabled. 1: Automatic adjustment is enabled.	R/W
b5	AADJP	Automatic Adjustment Period Select	0: Adds or subtracts the RADJ.ADJ[5:0] bits from the prescaler count value every 32 seconds 1: Adds or subtracts the RADJ.ADJ[5:0] bits from the prescaler count value every 8 seconds	R/W
b6	—	Reserved	This bit is undefined. The write value should be 0.	R/W
b7	CNTMD	Count Mode Select	0: The calendar count mode. 1: The binary count mode.	R/W

After correction

(2) In binary count mode:

Address(es): 0008 C424h

	b7	b6	b5	b4	b3	b2	b1	b0
	CNTMD	—	AADJP	AADJE	RTCOE	—	RESET	START
Value after reset:	x	x	x	x	0	0	0	x

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	START	Start*1	0: The 32-bit binary counter, 64-Hz counter, and prescaler are stopped. 1: The 32-bit binary counter, 64-Hz counter, and prescaler are in normal operation.	R/W
b1	RESET	RTC Software Reset	• In writing 0: Writing is invalid. 1: The prescaler and registers to be reset by RTC software are reset. (R64CNT, RSECAR/BCNT0AR, RMINAR/BCNT1AR, RHRAR/BCNT2AR, RWKAR/BCNT3AR, RDAYAR/BCNT0AER, RMONAR/BCNT1AER, RYRAR/BCNT2AER, RYRAREN/BCNT3AER, RADJ, RTCCRy, RSECCPy/BCNT0CPy, RMINCPy/BCNT1CPy, RHRCPy/BCNT2CPy, RDAYCPy/BCNT3CPy, RMONCPy, RCR2.ADJ30, RCR2.AADJE, RCR2.AADJP) • In reading 0: In normal time operation, or an RTC software reset has completed. 1: During an RTC software reset	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	RTCOE	RTCOUT Output Enable	0: RTCOUT output disabled. 1: RTCOUT output enabled.	R/W
b4	AADJE	Automatic Adjustment Enable*1	0: Automatic adjustment is disabled. 1: Automatic adjustment is enabled.	R/W
b5	AADJP	Automatic Adjustment Period Select*1	0: Adds or subtracts the RADJ.ADJ[5:0] bits from the prescaler count value every 32 seconds 1: Adds or subtracts the RADJ.ADJ[5:0] bits from the prescaler count value every 8 seconds	R/W
b6	—	Reserved	This bit is undefined. The write value should be 0.	R/W
b7	CNTMD	Count Mode Select*1	0: The calendar count mode. 1: The binary count mode.	R/W

Note 1. After writing to this bit, confirm that its value has actually changed before proceeding with further processing. Refer to section 26.6.5, Points for Caution when Writing to and Reading from Registers, regarding changes to the value of the AADJE and AADJP bits.

• Page 758 of 1390

The setting procedure described in Figure 26.3, Clock and Count Mode Setting Procedure is corrected as follows.

Before correction

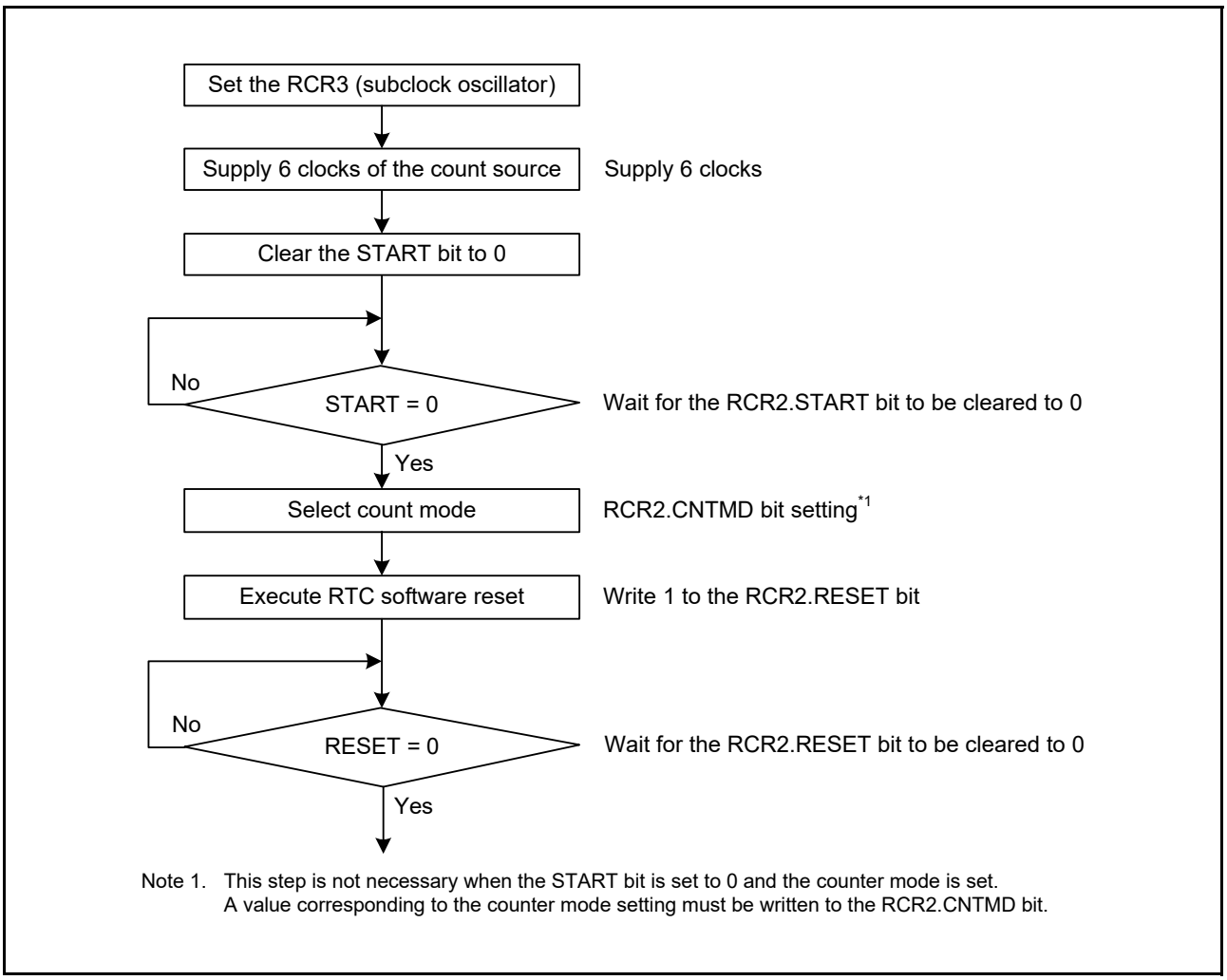

Figure 26.3 Clock and Count Mode Setting Procedure

After correction

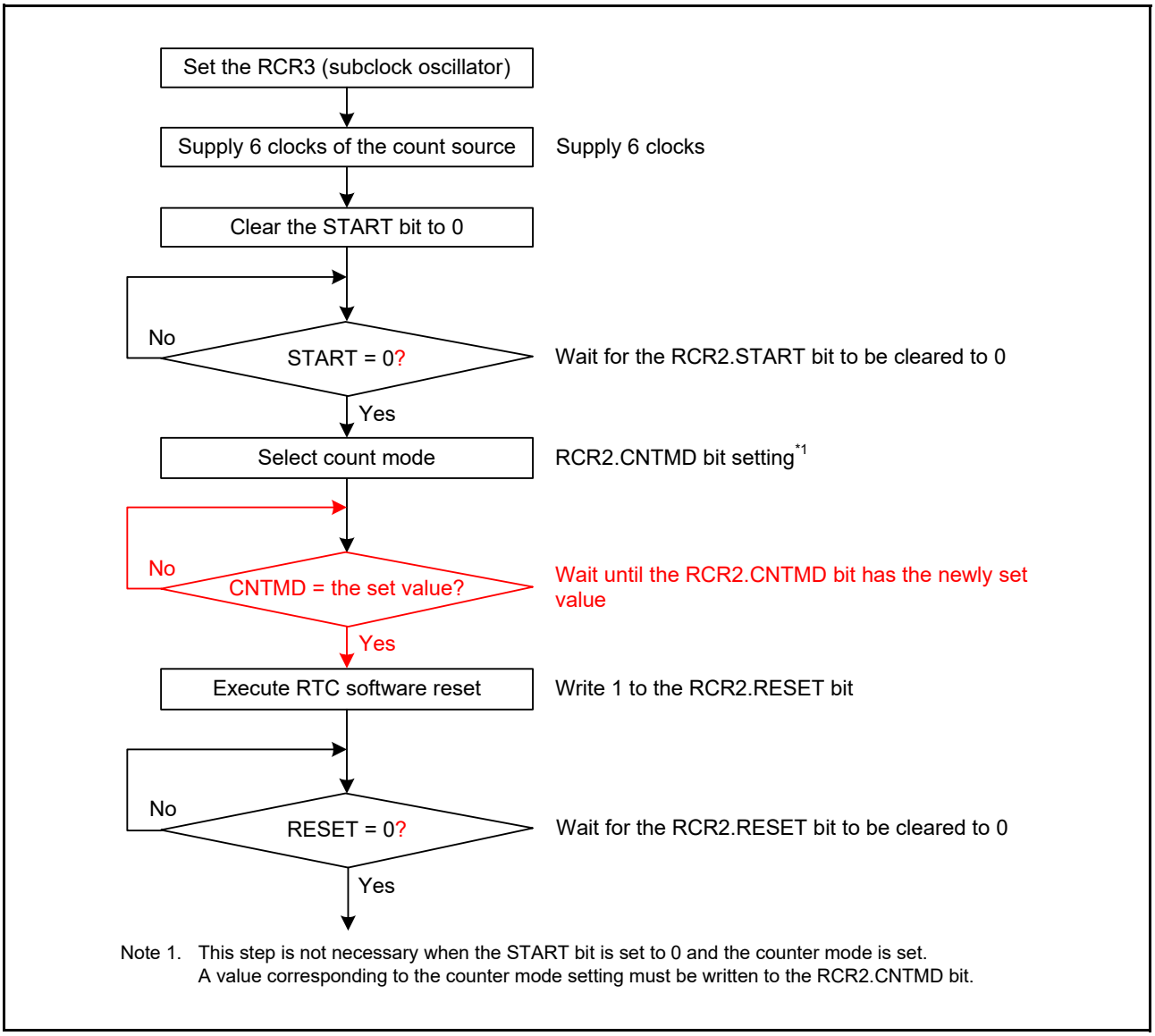

Figure 26.3 Clock and Count Mode Setting Procedure

Page Number, Section/Figure/Table Number

Item	Page Number, Section/Figure/Table Number	
	RX21A Group	RX220 Group
Table for (1) In calendar count mode of RTC Control Register 2 (RCR2)	Page 744 26.2.18	Page 674 25.2.18
Descriptions of the CNTMD bit	Page 745 26.2.18	Page 675 25.2.18
Table for (2) In binary count mode of RTC Control Register 2 (RCR2)	Page 746 26.2.18	Page 676 25.2.18
Figure of the clock and count mode setting procedure	Page 758 Figure 26.3	Page 681 Figure 25.3