Date: Oct. 15, 2015

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RL*-A010C/E	Rev.	3.00
Title	RL78/L13 Direction of use		Information Category	Technical Notification		
Applicable Product	RL78/L13 Group R5F10WxxA, R5F10WxxG Refer to Appendix1.	Lot No. All lot	Reference Document	RL78/L13 User's Manual: Hardware Rev. 2.00 R01UH0382EJ0200 (Nov. 2013)		

A new direction of use on the products below has been added
.

1. Direction added in Rev. 2.00

No.	Description	Products	Pages in this document for corrections
1.1	Restrictions on "PWM output function for IH control" of 16-BIT TIMER KB20 2)	All	Page 2

2. Direction previously notified

No.	Description	Products	Pages in this document for corrections
2.1	Restrictions on "PWM output function for IH control" of 16-BIT TIMER KB20 1)	Lot number "Before the week13 of 2015" (Please see 2.1.3 Permanent measures)	Pages 3 to 5
2.2	Operating Precaution for Data Flash read access	All	Pages 6 to 7

3. Revision history

Revision history of RL78/L13 directions of use

Document Number	Issued Date	Description
TN-RL*-A010A/E	Aug. 9, 2013	First edition issued List of direction previously: No.2.2
TN-RL*-A010B/E	Apr. 7, 2015	Second edition List of direction previously: No.2.1
TN-RL*-A010C/E	Oct. 15, 2015	Third edition List of direction added: No.1.1 (This document)

1． Restrictions Added by This Notice Update

1.1 16-Bit Timer KB20: Restriction on IH-PWM Output 2)

1.1.1 Restriction

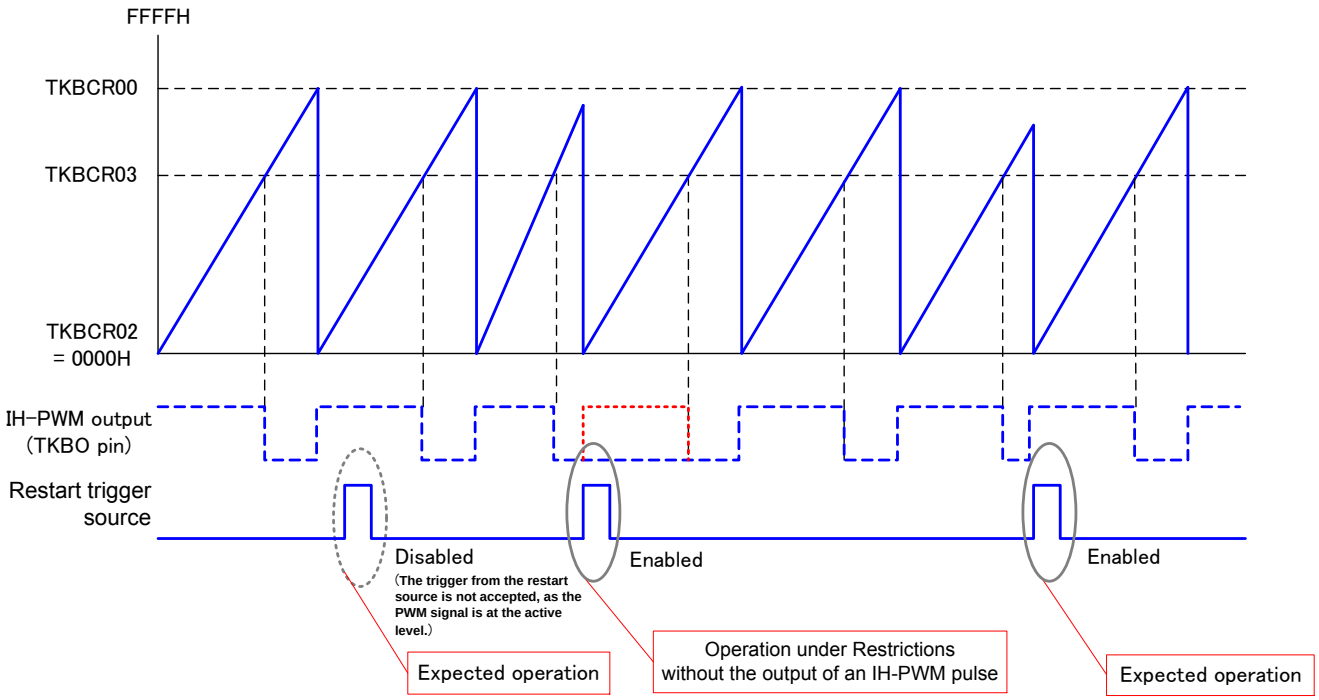
【Applicable usage】

The restriction applies when all of conditions 1 to 3 listed below are satisfied.

1. The IH-PWM output function is in use (Bit 15(TKBIHE0) =1 of TKBCTL00 register).
2. The setting of compare register 02 (TKBCR02) is 0000H.
3. A value other than 00H (no division) is set in the timer clock select register (TKBPSCS0).

【Restriction details】

Regarding the IH-PWM output function, one pulse of IH-PWM output may not be produced in response to the signal from an enabled restart trigger source if all of conditions 1 to 3 listed above are satisfied.



1.1.2 Workaround

When the IH-PWM output function (TKBIHE0=1) is used, solve this problem through one of the countermeasures listed below.

1. Set a value other than 0000H in compare register 02 (TKBCR02).
2. Set the timer clock select register (TKBPSCS0) for no frequency division of the clock.

1.1.3 Permanent measures

This matter is added to 16-BIT TIMER KB20 in the user's manual by the next revision.

2. Previous restrictions

2.1 Restrictions when using "PWM output function for IH control" of 16-BIT TIMER KB20 1)

2.1.1 Restrictions

【Applicable usage】

If you use the function below, the restriction is applicable

- Use IH-only PWM output function (Bit 15(TKBIHE0) =1 of TKBCTL00 register)

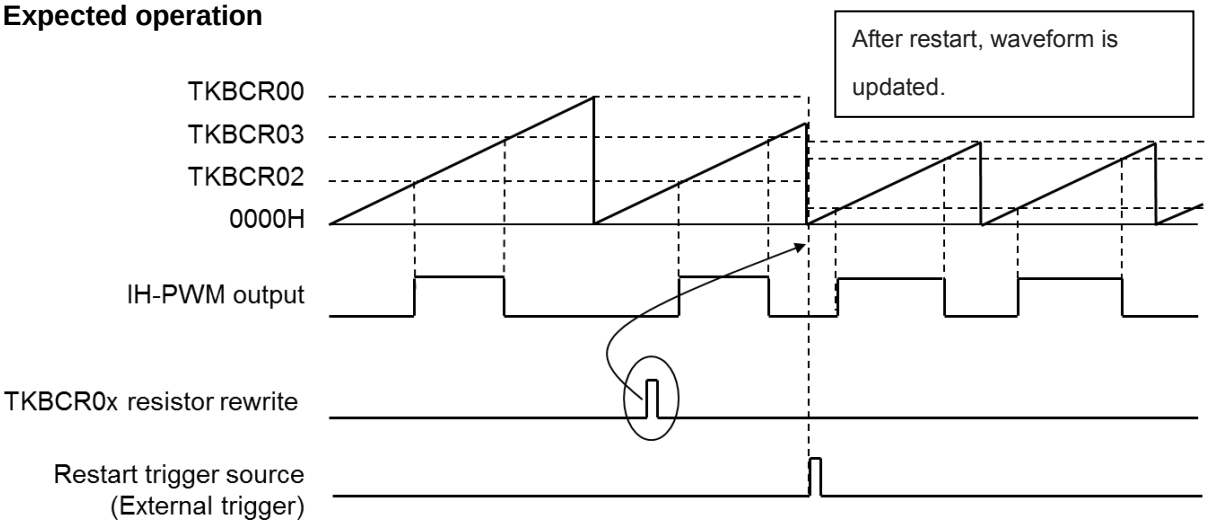
【Restriction details】

There are two restrictions.

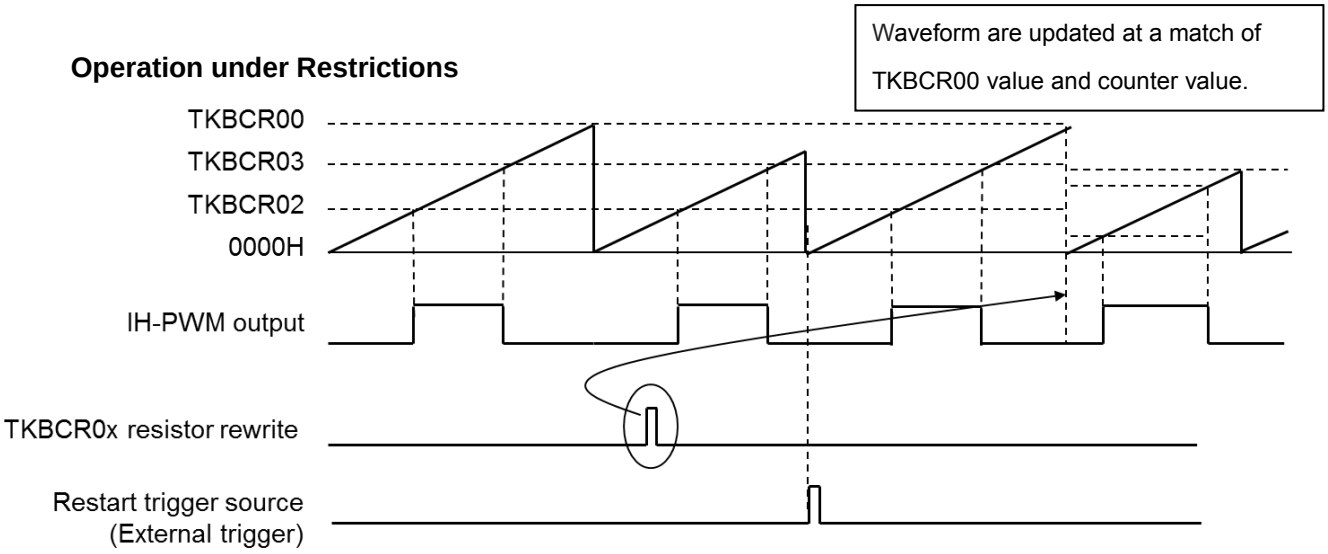
① the batch overwrite operation of compare register (TKBCR00, TKBCR02, TKBCR03) by an external trigger does not work.

If the compare register batch overwrite operation by an external trigger (Bit 2(TKBTSE0) =1 of TKBCTL00 resistor) is set, rewriting of the compare register (TKBCR00, TKBCR02, TKBCR03) by an external trigger is not performed as follows. In addition, re-start trigger is accepted.

Expected operation

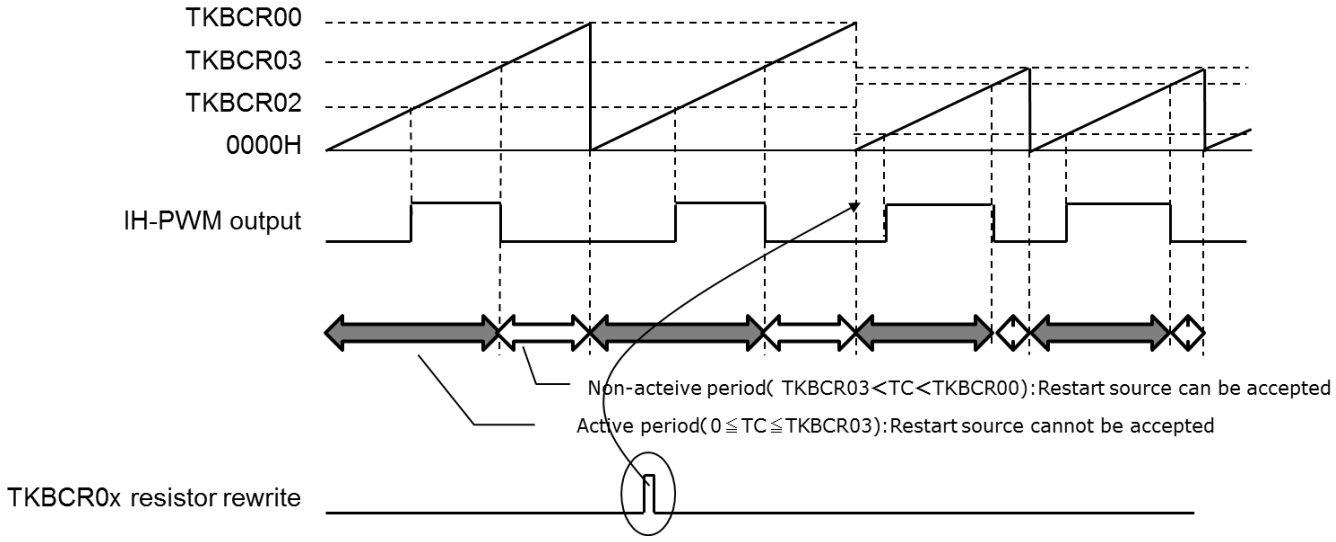


Operation under Restrictions

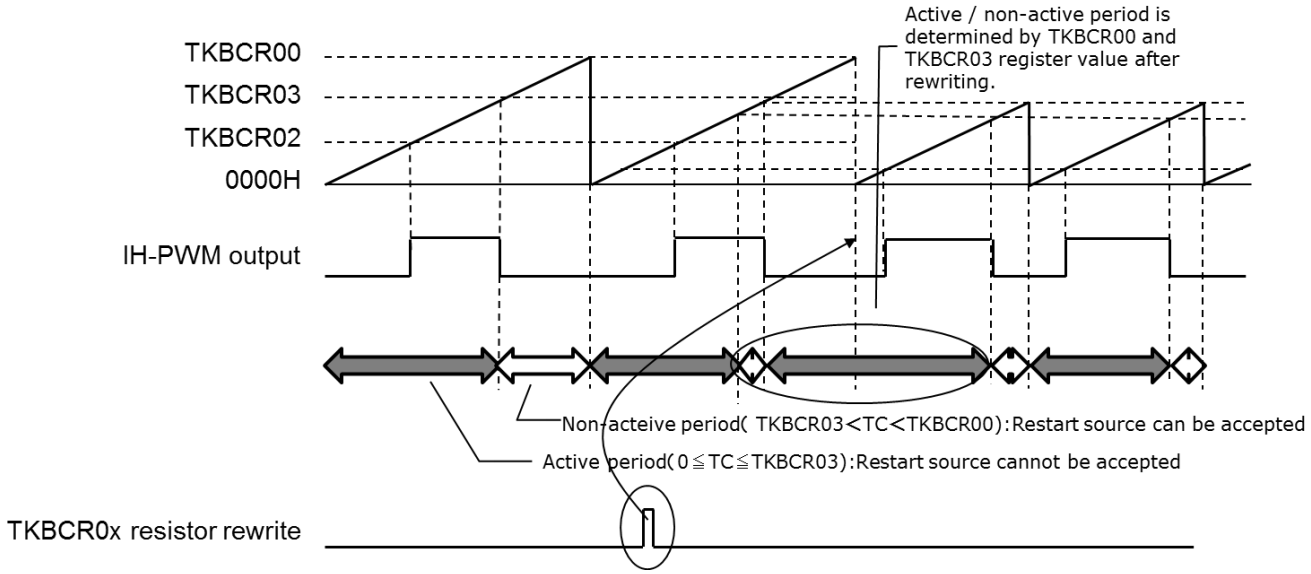


② In case of rewriting TKBCR00 or TKBCR03 when operating IH-PWM output function, even before the restart trigger factors or the comparison match with TKBCR03 value, the value of active period / non-active period is set to the rewritten value. As a result, there is the case that IH-PWM output restart request is accepted even in active period, or the case that IH-PWM output restart request is not accepted even in non-active period. The example is as follows.

Correct operation



Operation of Restrictions



2.1.2. Workaround

Please use as “IH-only PWM output function not used (Bit 15(TKBIHE0) =0 of TKBCTL00 register)”.

2.1.3. Permanent measures

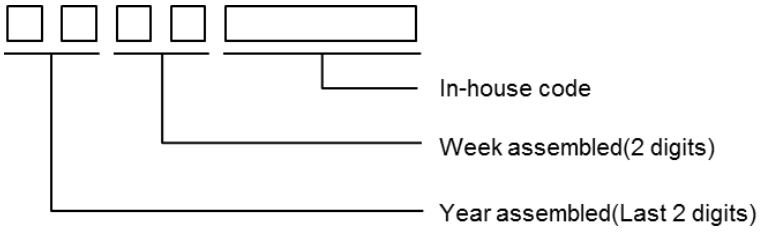
The products revision are planned. PWM output function for IH control becomes available at bit 15(TKBIHE0) of TKBCTL00 resistor = 1. In addition, there is no change of electrical specifications from the non-revised version. Please contact our sales department with regard to the shipment schedule of revised products,

Lot number on the package shows the availability of IH PWM output function.

View of lot number

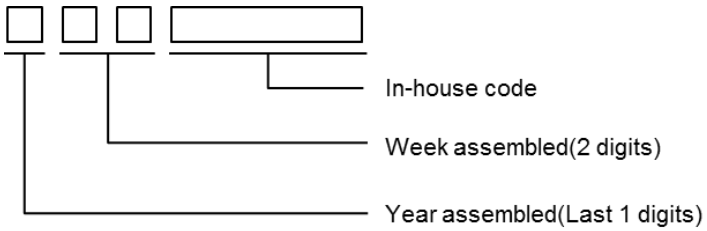
・LQFP,0.65mm pitch products（R5F10WxxAFA）

First four digits, "1514" and later: it means April 2015 and after April 2015.



・LFQFP,0.50mm pitch products（R5F10WxxAFB, R5F10WxxGFB）

First three digits, "514" and later: it means April 2015 and after April 2015.



2. Operating Precaution for Data Flash read access

2.2.1 Applicable Usage:

The usage which meets to all of (1), (2), and (3) is applicable to the restriction.

(1) Using both DMA and Data Flash.
(2) DMA is operating when Data Flash [Note1] read occurs.
(3) Data Flash is read using flash-related libraries Renesas Electronics is offering, which are listed below. Otherwise instead of using those libraries, the combination of CPU Related instructions [Note2] are used for reading related memory [Note3] and Data Flash.
- The EEL(EEPROM emulation library) [Note1] Pack01 V1.12 or earlier version.
- The FDL(Data Flash library) Type01 V1.11 or earlier version.
- The FDL Type02 V1.00 or earlier version.
- The FDL Type04 V1.04 or earlier version.

Note1. When EEL is used, commands other than READ command are also related: they also make read access to the Data Flash.
Note2. See Appendix2 about the combination of the related instructions1 and 2.
Note3. Related memory is RAM(Include general purpose register area),SFR,2nd SFR,ES,CS,PSW,SP

Detail of Restriction:

In the case that DMA transfer is operated and it is immediately followed by read access to the target memory (Related instructions 1) which access is also immediately followed in sequence, by read access to Data Flash (Related instructions 2), because of the conflict on the internal bus between read access to the target memory and to the Data Flash, the read out result from the target memory may be wrongly changed.

Example for an instruction sequence causing this issue:

```
    DMA transfer trigger
    DMA transfer
MOVW        HL,!addr16      ; read data from RAM (Related instruction 1)
MOV         A,[DE]          ; read data from Data Flash (Related instructions 2)
```

When DMA transfer occurs as mentioned above timing, a wrong data is loaded into HL register.

2.1.2 Workaround

If you have any possibility that read access to the Data Flash and the DMA transfer could operate in the same time, please apply the following procedures according to the way to read out the Data Flash.

Case 1:

Data Flash Read access via the 'Data Flash Access Library' (FDL) and/or EEPROM Emulation Library (EEL). Both libraries are developed under the responsibility of Renesas.

Workaround for Case 1:

There are currently one type of EEL supported and three type of FDL supported and all of them will be updated to cover the aforementioned workaround.

Library version (Not installer version)
- EEL (Pack01) version V1.13 [Note] or later
- FDL (Type01) version V1.12 [Note] or later
- FDL (Type02) version V1.01 [Note] or later
- FDL (Type04) version V1.05 [Note] or later

Case 2:

Data Flash Read access directly executed in the user software without library.

Workaround for Case 2:

Please apply either of the following procedures.

(A) Holding DMA or forcing termination DMA

In case, the user software has to perform a direct Data Flash Read access without using the FDL read commend, any possible DMA transfer must be stopped before the Data Flash read access is executed. To stop any DMA transfer, please follow the procedure given in the User Manual.

Furthermore, please make sure to wait at least 3 clocks(f_{CLK}) after setting DWAITn bit to “1” before the Data Flash read instruction is executed. Restart any DMA transfer (by clearing DWAITn bit to “0”) after the Data Flash read access have been finished.

(B) Reading Data Flash by using library

When access Data Flash, please use latest Data Flash library of case 1.

(C) Inserting a NOP instruction

Such kind of conflict can be avoided by inserting a NOP instruction immediately prior to any Data Flash Read access.

Example to avoid this issue: operand

```
MOVW    HL, !addr16    ; Read data from RAM
NOP                    ; Insert a NOP prior to the DF read access
MOV     A,[DE]         ; Read data from Data Flash
```

In case the application software will use the DMA feature, Renesas strongly recommend not to perform a direct Data Flash Read access in the user software, because in case of a high level language (e.g. C-Language) it cannot be avoided that the C-compiler may generate a code sequence as described before. Therefore, Renesas strongly recommend to perform the Data Flash Read access ONLY via the corresponding FDL read command.

Note. The modified version of EEL(EEPROM Emulation library) and FDL(Data Flash library) will be released in sequence after July 2013.

Remark. F_{CLK}: CPU/peripheral hardware clock frequency

2.1.3 Modification schedule

This matter is added to “Procedure for accessing data flash memory” of CHAPTER 28 FLASH MEMORY in the user’s manual by the next revision.

Appendix1

[Target products' name list]

RL78/L13 (R5F10W)

64-pin LFQFP 12x12mm	R5F10WLAAFA, R5F10WLCAFA, R5F10WLDAFA, R5F10WLEAFA, R5F10WLFAFA, R5F10WLGAFA,
64-pin LFQFP 10x10mm	R5F10WLAAFB, R5F10WLCAFB, R5F10WLDAFB, R5F10WLEAFB, R5F10WLFAFB, R5F10WLGAFB, R5F10WLAGFB, R5F10WLCGFB, R5F10WLDGFB, R5F10WLEGFB, R5F10WLFGFB, R5F10WLGGFB
80-pin LQFP 14x14mm	R5F10WMAAFA, R5F10WMCAFA, R5F10WMDAFA, R5F10WMEAFA, R5F10WMFAFA, R5F10WMGAFA,
80-pin LQFP 12x12mm	R5F10WMAAFB, R5F10WMCAFB, R5F10WMDAFB, R5F10WMEAFB, R5F10WMFAFB, R5F10WMGAFB, R5F10WMAGFB, R5F10WMCGFB, R5F10WMDGFB, R5F10WMEGFB, R5F10WMFGFB, R5F10WMGGFB

Appendix2-1

[Related instructions list]

In case that the Data Flash is read out by "Related instructions 2" immediately after the target memory is read out by "Related instructions 1", this is within the restriction; however, particular combinations of related instructions shown in Appendix2-2 are excepted.

Related instructions 1: Read instructions of RAM(Include general purpose register area), SFR,2nd SFR,ES,CS, PSW,SP

Note: Read instructions of mirror area and Data Flash are not related.

	Operand
MOV	A, saddr
	A, sfr
	A, !addr16
	A, PSW
	A, ES
	A, CS
	A, [DE]
	A, [DE+byte]
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
	A, word[B]
	A, word[C]
	A, word[BC]
	A, [SP+byte]
MOVW	AX, saddrp
	AX, sfrp
	AX, !addr16
	AX, [DE]
	AX, [DE+byte]
	AX, [HL]
	AX, [HL+byte]
	AX, word[B]
	AX, word[C]
	AX, word[BC]
	AX, [SP+byte]
ADD	A, saddr
	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]

	Operand
ADDC	A, saddr
	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
SUB	A, saddr
	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
SUBC	A, saddr
	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
AND	A, saddr
	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
OR	A, saddr
	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]

	Operand
XOR	A, saddr
	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
CMP	A, saddr
	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
ADDW	AX, saddrp
	AX, !addr16
	AX, [HL+byte]
SUBW	AX, saddrp
	AX, !addr16
	AX, [HL+byte]
CMPW	AX, saddrp
	AX, !addr16
	AX, [HL+byte]
MOVW	AX, SP

	Operand
MOV	ES, saddr
	B, saddr
	B, !addr16
	C, saddr
	C, !addr16
	X, saddr
	X, !addr16
MOVW	BC, saddrp
	BC, !addr16
	DE, saddrp
	DE, !addr16
	HL, saddrp
	HL, !addr16
	BC, SP
	DE, SP
	HL, SP
CMP	saddr, #byte
	!addr16, #byte
CMP0	saddr
	!addr16
CMPS	X, [HL+byte]

	Operand
MOV1	CY, saddr.bit
	CY, sfr.bit
	CY, PSW.bit
	CY, [HL].bit
AND1	CY, saddr.bit
	CY, sfr.bit
	CY, PSW.bit
	CY, [HL].bit
OR1	CY, saddr.bit
	CY, sfr.bit
	CY, PSW.bit
	CY, [HL].bit
XOR1	CY, saddr.bit
	CY, sfr.bit
	CY, PSW.bit
	CY, [HL].bit
POP	rp

Related instructions 2: Read instructions of Data Flash

	Operand
MOV	A, !addr16
	A, [DE]
	A, [DE+byte]
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
	A, word[B]
	A, word[C]
	A, word[BC]

	Operand
ADD	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
ADDC	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
SUB	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
SUBC	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]

	Operand
AND	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
OR	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
XOR	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]
CMP	A, !addr16
	A, [HL]
	A, [HL+byte]
	A, [HL+B]
	A, [HL+C]

	Operand
MOV	B, !addr16
	C, !addr16
	X, !addr16
CMP	!addr16, #byte
CMP0	!addr16
CMPS	X, [HL+byte]

Safe combinations of related instructions1 and 2 <1>

Related instruction 1		Related instruction 2	
	Operand		**Operand**
MOVW	DE, saddrp	MOV	A, [DE]
	DE, !addr16		A, [DE+byte]
	DE, SP		
POP	DE		

Safe combinations of related instructions1 and 2 <2>

Related instruction 1		Related instruction 2					
	Operand		**Operand**		**Operand**		**Operand**
MOVW	HL, saddrp	MOV	A, [HL]	ADD	A, [HL]	AND	A, [HL]
	HL, !addr16		A, [HL+byte]		A, [HL+byte]		A, [HL+byte]
	HL, SP		A, [HL+B]		A, [HL+B]		A, [HL+B]
POP	HL		A, [HL+C]		A, [HL+C]		A, [HL+C]
				ADDC	A, [HL]	OR	A, [HL]
			Operand		A, [HL+byte]		A, [HL+byte]
		CMPS	X, [HL+byte]		A, [HL+B]		A, [HL+B]
					A, [HL+C]		A, [HL+C]
				SUB	A, [HL]	XOR	A, [HL]
					A, [HL+byte]		A, [HL+byte]
					A, [HL+B]		A, [HL+B]
					A, [HL+C]		A, [HL+C]
				SUBC	A, [HL]	CMP	A, [HL]
					A, [HL+byte]		A, [HL+byte]
					A, [HL+B]		A, [HL+B]
					A, [HL+C]		A, [HL+C]

Safe combinations of related instructions1 and 2 <3>

Related instruction 1		Related instruction 2					
	Operand		**Operand**		**Operand**		**Operand**
MOV	B, saddr	MOV	A, [HL+B]	ADD	A, [HL+B]	AND	A, [HL+B]
	B, !addr16		A, word[B]	ADDC	A, [HL+B]	OR	A, [HL+B]
MOVW	BC, saddrp			SUB	A, [HL+B]	XOR	A, [HL+B]
	BC, !addr16			SUBC	A, [HL+B]	CMP	A, [HL+B]
	BC, SP						
POP	BC						

Safe combinations of related instructions1 and 2 <4>

Related instruction 1		Related instruction 2					
	Operand		**Operand**		**Operand**		**Operand**
MOV	C, saddr	MOV	A, [HL+C]	ADD	A, [HL+C]	AND	A, [HL+C]
	C, !addr16		A, word[C]	ADDC	A, [HL+C]	OR	A, [HL+C]
MOVW	BC, saddrp			SUB	A, [HL+C]	XOR	A, [HL+C]
	BC, !addr16			SUBC	A, [HL+C]	CMP	A, [HL+C]
	BC, SP						
POP	BC						

Safe combinations of related instructions1 and 2 <5>

Related instruction 1		Related instruction 2	
	Operand		**Operand**
MOV	B, saddr	MOV	A, word[BC]
	B, !addr16		
	C, saddr		
	C, !addr16		
MOVW	BC, saddrp		
	BC, !addr16		
	BC, SP		
POP	BC		