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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A0266A/E	Rev.	1.00
Title	Addition to the Electrical Characteristics for the RIICHS of the RX671 Group MCU Products		Information Category	Technical Notification		
Applicable Product	RX671 Group	Lot No. All	Reference Document	RX671 Group User's Manual: Hardware Rev.1.10 (R01UH0899EJ0110)		

This document describes addition of specifications for the electrical characteristics of the RIICHS in the RX671 Group User's Manual: Hardware, Rev.1.10.

• Page 3012 of 3046

The characteristics of SCLHS output minimum high/low pulse widths are added to Table 56.49, RIICHS Timing (2) as follows. Some terms are also corrected.

Before correction

Table 56.49 RIICHS Timing (2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item			Symbol	Min.*1	Max.	Unit	Test Conditions
RIICHS (Hs-mode) ICFER.HSME = 1	SCLHS input cycle time		t_{SCL}	10(12) × t_{IICcyc} + 80	—	ns	Figure 56.87
	SCLHS input high pulse width		t_{SCLH}	5(6) × t_{IICcyc}	—	ns	
	SCLHS input low pulse width		t_{SCLL}	5(6) × t_{IICcyc}	—	ns	
	SCLHS input rise time	C_b = 400pF	t_{SrCL}	—	80	ns	
		C_b = 100pF		—	40		
	SDAHS input rise time	C_b = 400pF	t_{SrDA}	—	160	ns	
		C_b = 100pF		—	80		
	SCLHS input fall time	C_b = 400pF	t_{SfCL}	—	80	ns	
		C_b = 100pF		—	40		
	SDAHS input fall time	C_b = 400pF	t_{SfDA}	—	160	ns	
		C_b = 100pF		—	80		
	SCLHS, SDAHS input spike pulse removal time		t_{SP}	0	1(1) × t_{IICcyc}	ns	Figure 56.86
	SDAHS input bus free time		t_{BUF}	5(6) × t_{IICcyc} + 40	—	ns	
	Start condition input hold time		t_{STAH}	t_{IICcyc} + 40	—	ns	Figure 56.87
	Restart condition input setup time		t_{STAS}	40	—	ns	
	Stop condition input setup time		t_{STOS}	40	—	ns	
	Data input setup time		t_{SDAS}	10	—	ns	
	Data input hold time	C_b = 400pF	t_{SDAH}	0	150	ns	
		C_b = 100pF		0	70		
	SCLHS, SDAHS capacitive load		C_b*2	—	400	pF	

After correction

Table 56.49 RIICHS Timing (2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item			Symbol	Min.*1	Typ.	Max.	Unit	Test Conditions
RIICHS (Hs-mode) ICFER.HSME = 1	SCLHS input cycle time		t_{SCL}	10(12) × t_{IICcyc} + 80	—	—	ns	Figure 56.87
	SCLHS input high pulse width		t_{SCLH}	5(6) × t_{IICcyc}	—	—	ns	
	SCLHS input low pulse width		t_{SCLL}	5(6) × t_{IICcyc}	—	—	ns	
	SCLHS input rise time	C_b = 400pF	t_{SrCL}	—	—	80	ns	
		C_b = 100pF		—	—	40		
	SDAHS input rise time	C_b = 400pF	t_{SrDA}	—	—	160	ns	
		C_b = 100pF		—	—	80		
	SCLHS input fall time	C_b = 400pF	t_{SfCL}	—	—	80	ns	
		C_b = 100pF		—	—	40		
	SDAHS input fall time	C_b = 400pF	t_{SfDA}	—	—	160	ns	
		C_b = 100pF		—	—	80		
	SCLHS, SDAHS input spike pulse removal time		t_{SP}	0	—	1(1) × t_{IICcyc}	ns	Figure 56.86
	SDAHS input bus free time		t_{BUF}	5(6) × t_{IICcyc} + 40	—	—	ns	
	START condition input hold time		t_{STAH}	t_{IICcyc} + 40	—	—	ns	Figure 56.87
	Repeated START condition input setup time		t_{STAS}	40	—	—	ns	
	STOP condition input setup time		t_{STOS}	40	—	—	ns	
	Data input setup time		t_{SDAS}	10	—	—	ns	
	Data input hold time	C_b = 400pF	t_{SDAH}	0	—	150	ns	
		C_b = 100pF		0	—	70		
	SCLHS, SDAHS capacitive load		C_b*2	—	—	400	pF	
	SCLHS output minimum high pulse width	C_b = 400pF	$t_{SCLH(min)}$	—	120	233	ns	
		C_b = 100pF		—	60	150		
	SCLHS output minimum low pulse width	C_b = 400pF	$t_{SCLL(min)}$	—	—	320	ns	
		C_b = 100pF		—	—	160		