

To our customers,

---

## Old Company Name in Catalogs and Other Documents

---

On April 1<sup>st</sup>, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

Send any inquiries to <http://www.renesas.com/inquiry>.

# RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan  
Renesas Technology Corp.

Product Category	MPU&MCU		Document No.	TN-H8*-A344A/E	Rev.	1.00
Title	Restrictions for use regarding the stall cancellation mode enable bit (SCME) in the USB endpoint stall register 1 (UESTL1)		Information Category	Technical Notification		
Applicable Product	H8S/2215 Group H8S/2218 Group H8S/2212 Group	Lot No.	Reference Document	H8S/2215 Group Hardware Manual (REJ09B0140-0600, Rev. 6.00) H8S/2218, H8S/2212 Group Hardware Manual (REJ09B0074-0400O, Rev. 4.00)		
		All lots				

Thank you for your consistent patronage of Renesas semiconductor products.

We would like to inform you of the restrictions for use regarding the USB module in the H8S/2215, H8S/2215R, H8S/2218, and H8S/2212 Groups.

## 1. Contents

When the stall cancellation mode enable bit (SCME) in the USB endpoint stall register 1 (UESTL1) is set to 1, this enables stall cancellation mode for all endpoints.

When the EPnSTL bit of the corresponding endpoint is set to 1 by software while the SCME bit in UESTL1 is 1, the EPnSTL bit, however, may be cleared to 0 by hardware, though the USB function module does not return a stall handshake to the host.

## 2. Phenomenon

While the SCME bit in UESTL1 is 1, if the EPnSTL bit of the corresponding endpoint is set to 1 by software, and an IN token or OUT token is received to the corresponding endpoint from the USB host simultaneously, the EPnSTL bit may be cleared to 0 by hardware, though the USB function module does not return a stall handshake to the host.

## 3. Measures

When the EPnSTL bit is cleared to 0 by hardware, whether this bit is cleared due to the above phenomenon or not is not determined by software. Therefore, to set the EPnSTL bit to 1 to enable stall cancellation mode for all endpoints is prohibited. The EPnSTL bit should be always cleared to 0 to disable stall cancellation mode for all endpoints.

4. Modifications in Hardware Manuals

**[Before Change]**

Section 15.3.10, USB Endpoint Stall Register 1 (UESTL1), in the H8S/2215 Group Hardware Manual

Section 14.3.7, USB Endpoint Stall Register 1 (UESTL1), in the H8S/2218, H8S/2212 Group Hardware Manual

Bit	Bit Name	Initial Value	R/W	Description
7	SCME	0	R/W	Stall Cancellation Mode Enable Controls stall cancellation mode. When this bit is set to 1, the EPnSTL bit, which has been set once, is automatically cleared to 0 after returning a handshake to the host. This bit is common to all endpoints. The stall cancellation mode cannot be specified for each endpoint. When this bit is cleared to 0, the EPnSTL bit, which has been set once, cannot be cleared automatically. To cancel the stall state of the EPn, clear the EPnSTL bit to 0. 0: Disables stall cancellation mode for all endpoints (EP0 to EP3). 1: Enables stall cancellation mode for all endpoints (EP0 to EP3).

**[After Change]**

Section 15.3.10, USB Endpoint Stall Register 1 (UESTL1), in the H8S/2215 Group Hardware Manual

Section 14.3.7, USB Endpoint Stall Register 1 (UESTL1), in the H8S/2218, H8S/2212 Group Hardware Manual

Bit	Bit Name	Initial Value	R/W	Description
7	SCME	0	R/W	Reserved The write value should always be 0.

**[Before Change]**

Section 15.5.11, Stall Operations, in the H8S/2215 Group Hardware Manual

Section 14.5.9, Stall Operations, in the H8S/2218, H8S/2212 Group Hardware Manual

**(2) Forcible Stall by Firmware**

The firmware uses the UESTL register to issue a stall request for the USB function module. When the firmware wishes to stall a specific endpoint, it sets the corresponding EPnSTL bit (1-1 in figure xx.xx). The internal status bits are not changed at this time.

When a transaction is sent from the host for the endpoint for which the EPnSTL bit was set, the USB function module refers the internal status bit, and if this is not set, refers the corresponding EPnSTL bit (1-2 in figure xx.xx). If the corresponding EPnSTL bit is not set, the internal status bit is not changed and the transaction is accepted. If the corresponding EPnSTL bit is set, the USB function module sets the internal status bit and returns a stall handshake to the host (1-3 in figure xx.xx). If the SCME bit in UESTL1 is set at this time, the EPnSTL bit is automatically cleared (1-4 in figure xx.xx).

Once an internal status bit is set, it remains set until cleared by a Clear Feature command from the host, without regarding to EPnSTL. Even after a bit is cleared by the Clear Feature command (3-1 in figure xx.xx), the USB function module continues to return a stall handshake while the EPnSTL bit is set, since the internal status bit is set each time a transaction is executed for the corresponding endpoint (1-2 in figure xx.xx). To clear a stall, therefore, it is necessary for the corresponding EPnSTL bit to be cleared by the firmware (or set the SCME bit so that the EPnSTL bit is automatically cleared when the USB function module returns a stall handshake), and also for the internal status bit to be cleared with a Clear Feature command (2-1 to 2-3 in figure xx.xx).

Note: Figure xx.xx in the description above indicates figure 15.23 in the H8S/2215 Group Hardware Manual, and figure 14.20 in the H8S/2218, H8S/2212 Group Hardware Manual, respectively.

**[After Change]**

Section 15.5.11, Stall Operations, in the H8S/2215 Group Hardware Manual

Section 14.5.9, Stall Operations, in the H8S/2218, H8S/2212 Group Hardware Manual

**(2) Forcible Stall by Firmware**

The firmware uses the UESTL register to issue a stall request for the USB function module. When the firmware wishes to stall a specific endpoint, it sets the corresponding EPnSTL bit (1-1 in figure xx.xx). The internal status bits are not changed at this time.

When a transaction is sent from the host for the endpoint for which the EPnSTL bit was set, the USB function module refers the internal status bit, and if this is not set, refers the corresponding EPnSTL bit (1-2 in figure xx.xx). If the corresponding EPnSTL bit is not set, the internal status bit is not changed and the transaction is accepted. If the corresponding EPnSTL bit is set, the USB function module sets the internal status bit and returns a stall handshake to the host (1-3 in figure xx.xx).

Once an internal status bit is set, it remains set until cleared by a Clear Feature command from the host, without regarding to EPnSTL. Even after a bit is cleared by the Clear Feature command (3-1 in figure xx.xx), the USB function module continues to return a stall handshake while the EPnSTL bit is set, since the internal status bit is set each time a transaction is executed for the corresponding endpoint (1-2 in figure xx.xx). To clear a stall, therefore, it is necessary for the corresponding EPnSTL bit to be cleared by the firmware, and also for the internal status bit to be cleared with a Clear Feature command (2-1 to 2-3 in figure xx.xx).

Step 1-4 is deleted in figure xx.xx, Forcible Stall by Firmware.

Note: Figure xx.xx in the description above indicates figure 15.23 in the H8S/2215 Group Hardware Manual, and figure 14.20 in the H8S/2218, H8S/2212 Group Hardware Manual, respectively.