To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Date: Nov. 14. 2007

RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Renesas Technology Corp.

Product Category	Development Environment		Document No.	TN-EML-A137A/E	Rev.	1.00
Title	Registers in on-chip peripheral modules initialized after software breakpoints have been set while the SH7211 E200F or E10A-USB emulator is in use		Information Category	Technical notification		
Applicable Product	SH7211 E200F emulator (R0E0200F1EMU00 + R0E572110VKK00) E10A-USB emulator (HS0005KCU01H/HS0005KCU02H)	Lot No. All lots	Reference Document	• SH-2A, SH-2 E200F Emulator Additional Document for User's Manual Supplementary Information on Using the SH7211 (REJ10J1264-0400) • SuperH™ Family E10A-USB Emulator Additional Document for User's Manual Supplementary Information on Using the SH7211 (REJ10J1273-0200)		

Thank you for using our products.

We have found a problem with the SH7211 E200F emulator (model name: R0E0200F1EMU00 + R0E572110VKK00) and E10A-USB emulator (model name: HS0005KCU01H/HS0005KCU02H).

Please take this information into account when you use the emulators.

1. Problem

1.1 Description

While the SH7211 E200F or E10A-USB emulator is in use, resuming the execution of the user program after setting a software breakpoint will initialize the values of the following registers in the on-chip modules.

- Compare match timer (CMT)
  - Compare match timer start register (CMSTR)
  - Compare match timer control/status register_0 (CMCSR_0)
  - Compare match counter_0 (CMCNT_0)
  - Compare match constant register_0 (CMCOR_0)
  - Compare match timer control/status register_1 (CMCSR_1)
  - Compare match counter_1 (CMCNT_1)
  - Compare match constant register_1 (CMCOR_1)
- A/D converter (ADC)
  - A/D control register (ADCR)
  - A/D status register (ADSR)
  - A/D start trigger select register (ADSTRGR)
  - A/D analog input channel select register (ADANSR)
  - A/D data register 0 (ADDR0)
  - A/D data register 1 (ADDR1)

- A/D data register 2 (ADDR2)
- A/D data register 3 (ADDR3)
- A/D data register 4 (ADDR4)
- A/D data register 5 (ADDR5)
- A/D data register 6 (ADDR6)
- A/D data register 7 (ADDR7)

- I^2C bus interface 3 (IIC3)
  - Bits BC[2:0] of the I^2C bus mode register (ICMR)

1.2 Condition

This problem occurs when the value of the frequency control register (FRQCR) is changed from H'1003 (default value) or H'1000 to any value that will change the frequency multiplication rate.

2. Actions of E200F and E10A-USB Emulators

The SH7211 E200F and E10A-USB emulators set H'1000 in FRQCR to change the operating frequency when the flash memory is to be programmed (programming of the flash memory takes place if the user program is run after a software breakpoint has been set in the flash memory area), as stated in section 21, Flash Memory, of the SH7211 Group Hardware Manual.

If this setting also changes the frequency multiplication rate, the registers listed in section 1.1 will be initialized as if the actual MCU is in the software standby mode as stated in section 4, Clock Pulse Generator (CPG) of the said hardware manual.

3. Resolutions for E200F and E10A-USB Emulators

3.1 Temporary Resolution

Do not set software breakpoints in the flash memory area. For the flash memory area, use of on-chip breakpoints is recommended.

3.2 Permanent Resolution

We will introduce an additional feature to the emulators so that the emulator software will save the values of CMT, ADC, and bits BC[2:0] of ICMR beforehand and restore these values after programming of the flash memory is completed.

3.3 Restrictions That Will Remain after the Permanent Resolution is Taken

(1) Even after the flash memory is programmed, the following registers hold the default values.

Table 1

Register	**Value**
Compare match flag (CMF) bits of the compare match timer control/status registers (CMCSR_0 and CMCSR_1)	0 (default value)
Compare match counter (CMCNT)	H'0000 (default value)
A/D end flag (ADF) bit of the A/D status register (ADSR)	0 (default value)
A/D data registers 0 to 7 (ADDR0 to ADDR7)	H'0000 (default value)

Note: These bits and registers hold the default values because (a) only 0 can be written to, (b) the register is read-only, or (c) correct values cannot be restored.

(2) Peripheral modules other than the watchdog timer (WDT) continue their operations even during an emulator break. The frequency division ratio of an internal clock (Iϕ), a bus clock (Bϕ), and a peripheral clock (Pϕ) is 4:4:4 while the flash memory is being programmed.

3.4 Product Versions in Which the Permanent Resolution Will be Introduced

The permanent resolution will be introduced in the following versions of emulator software.

- E200F emulator: V.2.05 release 00
- E10A-USB emulator: V.2.10 release 00