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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-R8C-A038A/E	Rev.	1.00
Title	R8C/L3xx Group Timer RE Supplement and Correction		Information Category	Technical Notification		
Applicable Products	R8C/L35A, L35B, L35C, L35M Groups R8C/L36A, L36B, L36C, L36M Groups R8C/L38A, L38B, L38C, L38M Groups R8C/L3AA, L3AB, L3AC, L3AM Groups	Lot No. –	Reference Document			

This document supplements and corrects descriptions of timer RE in the User's Manual: Hardware of the above applicable MCUs. Some MCUs may not have the functions. Refer to the User's Manual: Hardware of your product.

1. Correction on timer RE reset bit (TRERST bit)

The follow correction to the timer RE reset bit (TRERST bit) is taken from the R8C/L35M, R8C/L36M, R8C/L38M, and R8C/L3AM Group User's Manual: Hardware (R01UH0110EJ0100). Refer to the User's Manual: Hardware of your product.

22.2.5 Timer RE Control Register 1 (TRECR1) in Real-Time Clock Mode

Address 011Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TSTART	H12_H24	PM	TRERST	INT	TOENA	TCSTF	—
After Reset	X	X	X	X	X	0	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	TCSTF	Timer RE count status flag	0: Count stopped 1: Counting	R
b2	TOENA	TREO pin output enable bit	0: Clock output disabled 1: Clock output enabled	R/W
b3	INT	Interrupt request timing bit	Set to 1 in real-time clock mode.	R/W
b4	TRERST	Timer RE reset bit	When setting this bit to 0 after setting it to 1, the following will occur: • Registers TRESEC, TREMIN, TREHR, TREWK, and TRECR2 are set to 00h. • Bits TCSTF, INT, PM, H12_H24, and TSTART in the TRECR1 register are set to 0. • The 8-bit counter is set to 00h and the 4-bit counter is set to 0h.	R/W
b5	PM	A.m./p.m. bit	When the H12_H24 bit is set to 0 (12-hour mode) (1) 0: a.m. 1: p.m. When the H12_H24 bit is set to 1 (24-hour mode), its value is undefined.	R/W
b6	H12_H24	Operating mode select bit	0: 12-hour mode 1: 24-hour mode	R/W
b7	TSTART	Timer RE count start bit	0: Count stops 1: Count starts	R/W

Note:
1. This bit is automatically modified while timer RE counts.

When setting this bit to 1, the following will occur and timer RE control circuit will be initialized. After setting this bit to 1, make sure to set it to 0.

The above correction also applies in output compare mode.

2. Correction on notes on timer RE

The following correction to notes on timer RE is taken from the R8C/L35M, R8C/L36M, R8C/L38M, and R8C/L3AM Group User's Manual: Hardware (R01UH0110EJ0100). Refer to the manual of your product.

22.4 Notes on Timer RE

22.4.1 Reset

A reset input does not reset the timer RE data registers that store data of seconds, minutes, hours, and days of the week. This requires the initial setting of all registers after power on.

The registers and bits associated with timer RE below will not be reset by hardware reset, power-on reset, voltage monitor 0 reset, watchdog timer reset, or software reset. As the content of such registers and bits are undefined after power on, initialize these registers and bits after setting the TRERST bit to 0. When the TRERST bit is set to 1, the registers and bits are set to 0, and the timer RE control circuit will be initialized. After setting the TRERST bit to 1, make sure to set it to 0.

Applicable registers and bits:
Registers TRESEC, TREMIN, TREHR, TREWK, and TRECR2
Bits TCSTF, INT, TRERST, PM, H12_H24, TSTART in the TRECR1 register

3. Supplement information for the setting example in output compare mode