Date: Mar. 24, 2017

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	System LSI	Document No.	TN-RIN-A018A/E	Rev.	1.00
Title	Notification of R-IN32M3 Series User's Manual: R-IN32M3-EC (Rev.4.00 to Rev.4.01) Revised contents: Corrections and new functions		Information Category	Technical Notification	
Applicable Product	See following	Lot No. / All lots	Reference Document	R-IN32M3 Series User's Manual: R-IN32M3-EC Rev. 4.01 (R18UZ0003EJ0401)	

R-IN32M3 Series User's Manual: R-IN32M3-EC Rev. 4.01 (R18UZ0003EJ0401) has been released on Renesas website. This technical update follows revision 4.00 and includes the entirety of revised items. For details, refer to "2. Documentation Updates" given below. Please take note that items marked with "*note" may have severe impact on the specification and limitation of corresponding devices.

1 Applicable Product

Product Type	Model Marking	Product Code
R-IN32M3-EC	MC-10287F1	MC-10287F1-HN4-A
		MC-10287F1-HN4-M1-A
	MC-10287BF1	MC-10287BF1-HN4-A
		MC-10287BF1-HN4-M1-A
R-IN32M3-CL	D60510F1	UPD60510F1-HN4-A
		UPD60510F1-HN4-M1-A
	D60510BF1	UPD60510BF1-HN4-A
		UPD60510BF1-HN4-M1-A

2 Documentation Updates

No	Applicable Item (Rev. 4.01 Section)	Applicable Page (Rev. 4.01)	Contents
1	2.1.2 EtherCAT Slave Controller Pins	9	Error correction
2	2.1.5 Port Pins and Real-Time Port Pins	15	Error correction
3	2.1.14 CC-Link Pins (Intelligent Device Station)	20	Complement
4	2.1.16 System Pins	22	Expression alignment
5	4.2 List of Interrupts, Table 4.1 (2/4)	47	Expression alignment
6	4.2 List of Interrupts, Table 4.1 (3/4), (4/4)	48-49	New function
7	5. Peripheral Modules	50	Expression alignment
8	6.3 Interrupt and I/O Signals, Table 6.3	53	Error correction
9	6.6.3 EtherCAT Reset Register (CATRESET)	65	Complement
10	6.11.1 AL Control Register (AL_CONTROL)	79	New function
11	6.11.2 AL Status Register (AL_STATUS)	80	New function
12	6.12.3 PDI Configuration Register (PDI_CNFIG)	85	Error correction
13	6.22 Reset circuit *note	142-143	Complement
14	7.2.4 Fast Link-Loss Detection Function	150	Error correction
15	7.3.1 Hardware Power-Down mode *note	151	Complement
16	7.4 MII Management Registers in Ethernet PHY	153	Complement
17	7.4.1 Register 0 – Control Register to 7.4.24 Register 31 – PHY Special Control/Status Register	154-176	Error correction
18	7.5.3 Ethernet PHY Power-Up Status Register (PHYPUS)	179	Complement
19	7.6 LED signal	180	Complement

No.1 2.1.2 EtherCAT Slave Controller Pins
Active level of CATRESTOUT modified

V4.00

Page	Description
9	**[2.1.2 EtherCAT Slave Controller Pins]**

Pin Name	I/O	Function	Shared Port	Active	Level during & after Reset
CATRESTOUT	O	EtherCAT PHY RESETOUT	P56	-	Hi-Z（High）

V4.01

Page	Description
9	**[2.1.2 EtherCAT Slave Controller Pins]**

Pin Name	I/O	Function	Shared Port	Active	Level during & after Reset
CATRESTOUT	O	EtherCAT PHY RESETOUT	P56	High	Hi-Z（High）

No.2 2.1.5 Port Pins and Real-Time Port Pins
Mode 2 of P73 pin modified

V4.00

Page	Description
15	**[2.1.5 Port Pins and Real-Time Port Pins]** **(3/4)**

	Pin Name	Mode 1	Mode 2	Mode 3	Mode 4	Level during & after Reset
P7	P73	CSICS11	P0SPEED10LED	CCS_STATION_NO_3 / CCM_SNIN3	-	**Hi-Z**

V4.01

Page	Description
15	**[2.1.5 Port Pins and Real-Time Port Pins]** **(3/4)**

	Pin Name	Mode 1	Mode 2	Mode 3	Mode 4	Level during & after Reset
P7	P73	CSICS11	P0SPEED10LEDZ	CCS_STATION_NO_3 / CCM_SNIN3	-	**Hi-Z**

No.3 2.1.14 CC-Link Pins (Intelligent Device Station)
Description for the CCM_MDIN0-3 signals modified.

V4.00

Page	Description
20	**[2.1.14 CC-Link Pins (Intelligent Device Station)]**

Pin Name	I/O	Function	Shared Port	Active	Level during & after Reset
CCM_LINKERRZ	O	Link error LED control output	P20	Low	Hi-Z
CCM_ERRZ	O	Error LED control output	P21	Low	
CCM_RUNZ	O	Run LED control output	P26	Low	
CCM_MDIN0-CCM_MDIN3	I	Mode setting switch input	P62-P65	—	
CCM_SNIN0-CCM_SNIN7	I	Station no. setting switch input	P70-P77	—	

V4.01

Page	Description
20	**[2.1.14 CC-Link Pins (Intelligent Device Station)]**

Pin Name	I/O	Function	Shared Port	Active	Level during & after Reset
CCM_LINKERRZ	O	Link error LED control output	P20	Low	Hi-Z
CCM_ERRZ	O	Error LED control output	P21	Low	
CCM_RUNZ	O	Run LED control output	P26	Low	
CCM_MDIN0-CCM_MDIN3	I	Transfer rate and mode setting switch input	P62-P65	—	
CCM_SNIN0-CCM_SNIN7	I	Station no. setting switch input	P70-P77	—	

No.4 2.1.16 System Pins
Function of PONRZ modified

<table>
<tr><th colspan="2">V4.00</th><th colspan="2">V4.01</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>22</td><td>[2.1.16 System Pins]
<table><tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Active</th><th>Level during & after Reset</th></tr><tr><td>PONRZ</td><td>I</td><td>Internal RAM power on reset input</td><td>Low</td><td>-</td></tr></table></td><td>22</td><td>[2.1.16 System Pins]
<table><tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Active</th><th>Level during & after Reset</th></tr><tr><td>PONRZ</td><td>I</td><td>Power on reset input</td><td>Low</td><td>-</td></tr></table></td></tr>
</table>

No.5 4.2 List of Interrupts
Exception No.54 INTETHSW: Interrupt source name changed

<table>
<tr><th colspan="2">V4.00</th><th colspan="2">V4.01</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>47</td><td>[4.2 List of Interrupts]
[Table 4.1 List of Interrupts]
(2/4)<table><tr><th rowspan="2">Exception No.</th><th rowspan="2">Name</th><th rowspan="2">Interrupt Source</th><th colspan="5">Connected to</th></tr><tr><th>NVIC</th><th>HW-RTOS</th><th>DMAC</th><th>Real Time Port</th><th>Timer</th></tr><tr><td>54</td><td>INTETHSW</td><td>Ether SWITCH interrupt</td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td></tr></table></td><td>47</td><td>[4.2 List of Interrupts]
[Table 4.1 List of Interrupts]
(2/4)<table><tr><th rowspan="2">Exception No.</th><th rowspan="2">Name</th><th rowspan="2">Interrupt Source</th><th colspan="5">Connected to</th></tr><tr><th>NVIC</th><th>HW-RTOS</th><th>DMAC</th><th>Real Time Port</th><th>Timer</th></tr><tr><td>54</td><td>INTETHSW</td><td>Ether SWITCH Timer interrupt <R></td><td>○</td><td>○</td><td>○</td><td>○</td><td>○</td></tr></table></td></tr>
</table>

No.6 4.2 List of Interrupts

ECC error interrupts are added to exception numbers 115 to 120 of Table 4.1.

V4.00

Page: 48-49

Description:

[4.2 List of Interrupts]

[Table 4.1 List of Interrupts]

(3/4)

Exception No.	Name	Interrupt Source	Connected to				
			NVIC	HW-RTOS	DMAC	Real Time Port	Timer
113	—	Reserved	—	—	—	—	—
114	—	Reserved	—	—	—	—	—
115	—	Reserved	—	—	—	—	—
116	—	Reserved	—	—	—	—	—
117	—	Reserved	—	—	—	—	—
118	—	Reserved	—	—	—	—	—
119	—	Reserved	—	—	—	—	—

(4/4)

Exception No.	Name	Interrupt Source	Connected to				
			NVIC	HW-RTOS	DMAC	Real Time Port	Timer
120	—	Reserved	—	—	—	—	—

V4.01

Page: 48-49

Description:

[4.2 List of Interrupts]

[Table 4.1 List of Interrupts]

(3/4)

Exception No.	Name	Interrupt Source	Connected to				
			NVIC	HW-RTOS	DMAC	Real Time Port	Timer
113	—	Reserve	—	—	—	—	—
114	—	Reserve	—	—	—	—	—
115	IRAMECCSEC	Internal instruction RAM 1-bit ECC error correction interrupt	✓	—	—	—	—
116	DRAMECCSEC	Data RAM 1-bit ECC error correction interrupt	✓	—	—	—	—
117	BRAMECCSEC	Buffer RAM 1-bit ECC error correction interrupt	✓	—	—	—	—
118	IRAMECCDED	Internal instruction RAM 2-bit ECC error detection interrupt	✓	—	—	—	—
119	DRAMECCDED	Data RAM 2-bit ECC error detection interrupt	✓	—	—	—	—

(4/4)

Exception No.	Name	Interrupt Source	Connected to				
			NVIC	HW-RTOS	DMAC	Real Time Port	Timer
120	BRAMECCDED	Buffer RAM 2-bit ECC error detection interrupt	✓	—	—	—	—

No.7 5. Peripheral Modules

Expressions of peripheral functions are unified to that in the User's Manual (Peripheral Modules).

<table>
<tr><th colspan="2">V4.00</th><th colspan="2">V4.01</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>50</td><td>[5. Peripheral Modules]

● Clock function
● CPU
● Bus structure
● Hardware real-time OS

● Asynchronous SRAM memory controller
● Synchronous burst access memory controller

● Serial flash ROM memory controller
● DMA function
● Timer array unit J (TAUJ)
● Window watchdog timer A (WDTA)
● Asynchronous serial interface J (UARTJ)
● Clocked serial interface H (CSIH)
● I2C BUS (IICB)
● CAN controller (FCN)
● CC-Link (Intelligent device station)
● CC-Link (Remote device station)
● Other interface control
● Debug function</td><td>50</td><td>[5. Peripheral Modules]

● Clock function/Reset function
● CPU/Internal RAM
● Bus structure
● Hardware real-time OS
● Gigabit Ethernet interface
● Asynchronous SRAM memory controller
● Synchronous burst access memory controller
● External MCU interface
● Serial flash ROM memory controller
● DMA function
● Timer array unit J (TAUJ2)
● Window watchdog timer A (WDTA)
● Asynchronous serial interface J (UARTJ)
● Clocked serial interface H (CSIH)
● I2C BUS (IICB)
● CAN controller (FCN)
● CC-Link (Intelligent device station, Remote device station)

● System registers (APB peripheral register area)
● Debug function</td></tr>
</table>

No.8 6.3 Interrupt and I/O Signals

Active level of CATRESTOUT modified

<table>
<tr><th colspan="2">V4.00</th><th colspan="2">V4.01</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>53</td><td>[6.3 Interrupt and I/O Signals]

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Shared Port</th><th>Active</th></tr>
<tr><td>CATRESTOUT</td><td>O</td><td>EtherCAT PHY RESETOUT</td><td>P56</td><td>-</td></tr>
</table>
</td><td>53</td><td>[6.3 Interrupt and I/O Signals]

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Shared Port</th><th>Active</th></tr>
<tr><td>CATRESTOUT</td><td>O</td><td>EtherCAT PHY RESETOUT</td><td>P56</td><td>High</td></tr>
</table>
</td></tr>
</table>

No.9 6.6.3 EtherCAT Reset Register (CATRESET)

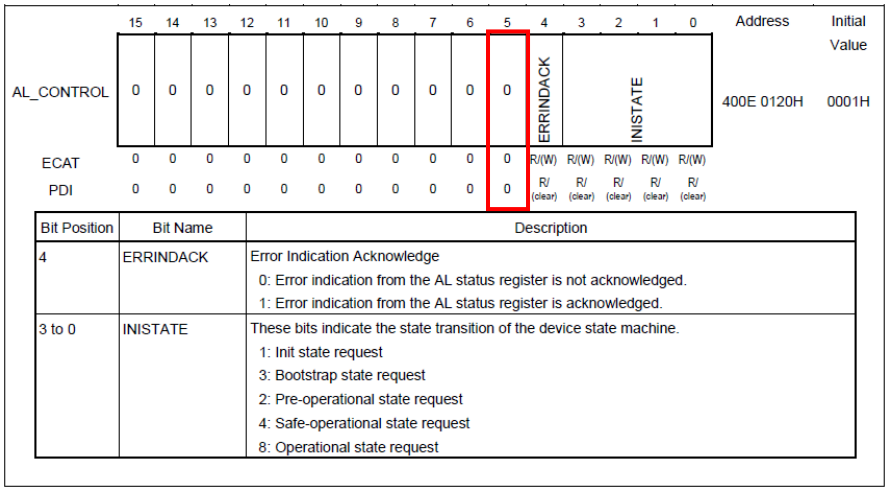
Caution 2 modified

V4.00		V4.01	
Page	Description	Page	Description
65	**[6.6.3 EtherCAT Reset Register (CATRESET)]** Caution 2. Release the reset after securing the time to satisfy reset width to EtherPHY by software in case of resetting EtherCAT again.	65	**[6.6.3 EtherCAT Reset Register (CATRESET)]** Caution 2. Control this register after securing the time to satisfy reset width to EtherPHY by software in case of resetting EtherCAT. For detail, see section 6.22, Reset Circuit <R>.

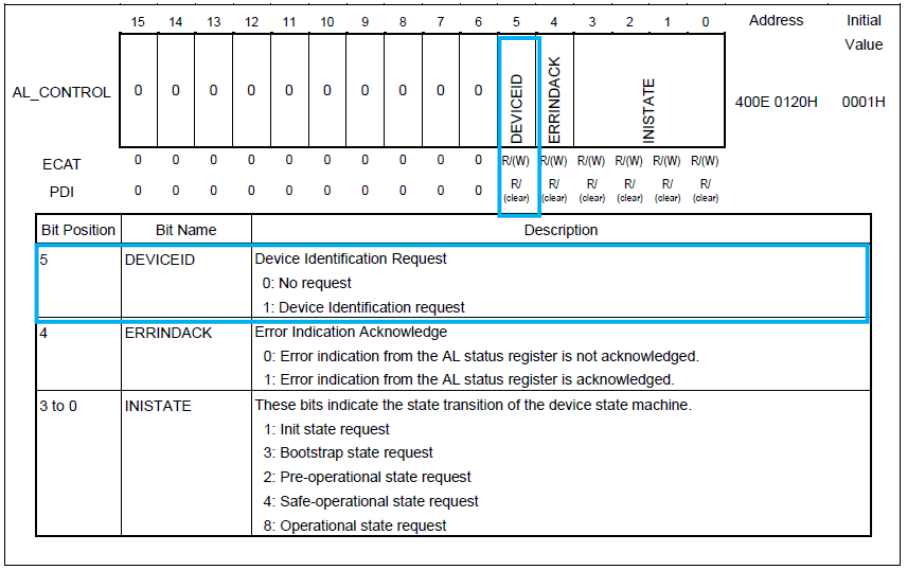
No.10 6.11.1 AL Control Register (AL_CONTROL)

Device Identification Request added into bit5

V4.00		V4.01	
Page	Description	Page	Description
79	**[6.11.1 AL Control Register (AL_CONTROL)]**	79	**[6.11.1 AL Control Register (AL_CONTROL)]**



Bit Position	Bit Name	Description
4	ERRINDACK	Error Indication Acknowledge 0: Error indication from the AL status register is not acknowledged. 1: Error indication from the AL status register is acknowledged.
3 to 0	INISTATE	These bits indicate the state transition of the device state machine. 1: Init state request 3: Bootstrap state request 2: Pre-operational state request 4: Safe-operational state request 8: Operational state request



Bit Position	Bit Name	Description
5	DEVICEID	Device Identification Request 0: No request 1: Device Identification request
4	ERRINDACK	Error Indication Acknowledge 0: Error indication from the AL status register is not acknowledged. 1: Error indication from the AL status register is acknowledged.
3 to 0	INISTATE	These bits indicate the state transition of the device state machine. 1: Init state request 3: Bootstrap state request 2: Pre-operational state request 4: Safe-operational state request 8: Operational state request

No.11 6.11.2 AL Status Register (AL_STATUS)

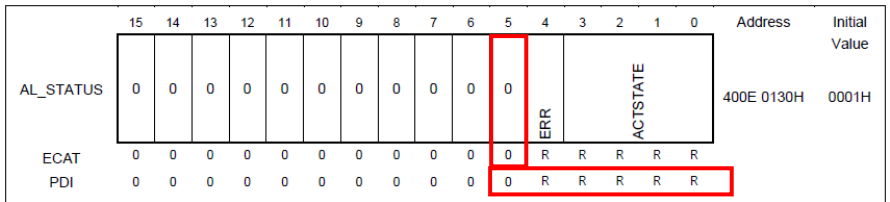
Device Identification Status added into bit5, Write from PDI added

V4.00

Page: 80

Description:

[6.11.2 AL Status Register (AL_STATUS)]



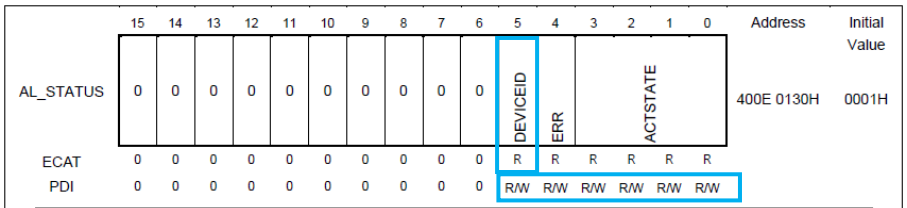
Bit Position	Bit Name	Description
4	ERR	Error Indicator 0: The device is in the state as requested or the flag is cleared by command. 1: The device has not entered the requested state or the state has changed as a result of a local action.
3 to 0	ACTSTATE	Actual State of the Device State Machine 1: Init state 3: Request bootstrap state 2: Pre-operational state 4: Safe-operational state 8: Operational state

V4.01

Page: 80

Description:

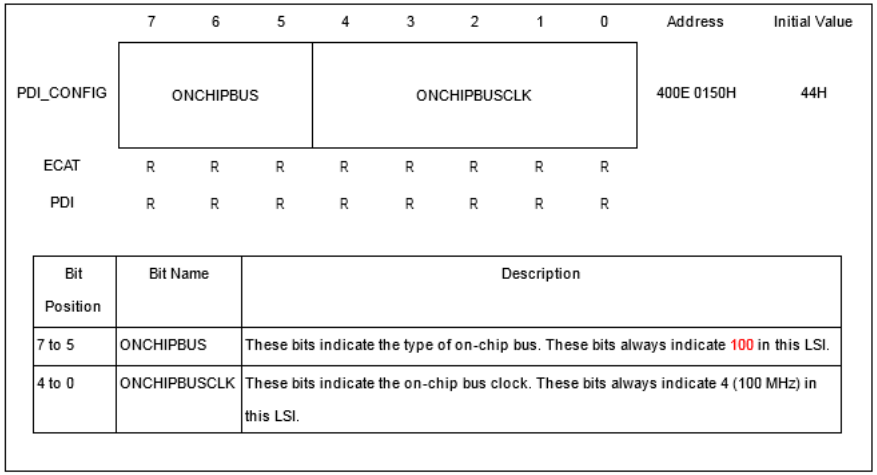
[6.11.2 AL Status Register (AL_STATUS)]

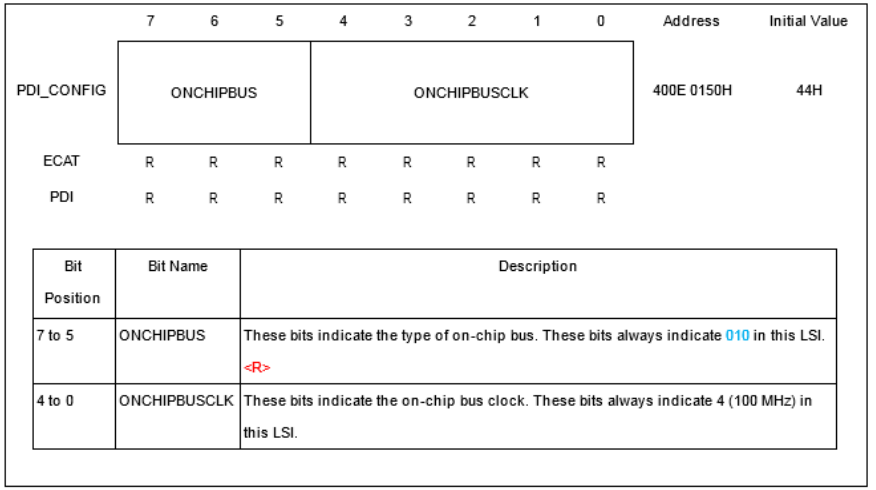


Bit Position	Bit Name	Description
5	DEVICEID	Device Identification Status 0: Device Identification not valid 1: Device Identification loaded
4	ERR	Error Indicator 0: The device is in the state as requested or the flag is cleared by command. 1: The device has not entered the requested state or the state has changed as a result of a local action.
3 to 0	ACTSTATE	Actual State of the Device State Machine 1: Init state 3: Request bootstrap state 2: Pre-operational state 4: Safe-operational state 8: Operational state

No.12 6.12.3 PDI Configuration Register (PDI_CONFIG)

Value indicated by ONCHIPBUS modified (100 → 010).

<table>
<tr><th colspan="2">V4.00</th><th colspan="2">V4.01</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>85</td><td>[6.12.3 PDI Configuration Register (PDI_CONFIG)]
 

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>7 to 5</td><td>ONCHIPBUS</td><td>These bits indicate the type of on-chip bus. These bits always indicate 100 in this LSI.</td></tr>
<tr><td>4 to 0</td><td>ONCHIPBUSCLK</td><td>These bits indicate the on-chip bus clock. These bits always indicate 4 (100 MHz) in this LSI.</td></tr>
</table></td><td>85</td><td>[6.12.3 PDI Configuration Register (PDI_CONFIG)]
 

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>7 to 5</td><td>ONCHIPBUS</td><td>These bits indicate the type of on-chip bus. These bits always indicate 010 in this LSI. <R></td></tr>
<tr><td>4 to 0</td><td>ONCHIPBUSCLK</td><td>These bits indicate the on-chip bus clock. These bits always indicate 4 (100 MHz) in this LSI.</td></tr>
</table></td></tr>
</table>

No.13 6.22 Reset circuit

Explanation of reset circuit around ESC added

V4.00		V4.01	
Page	Description	Page	Description
-	(No entry)	142-143	**[6.22 Reset circuit]** **Newly added**

No.14 7.2.4 Fast Link-Loss Detection Function
Explanation of error count method modified

V4.00		V4.01	
Page	Description	Page	Description
149	**[7.2.4 Fast Link-Loss Detection Function]** ● In the IDLE state when communication is not performed, count the error judged as bit error when received symbol is other than J which means the start of IDLE symbol or frame delimiter. ● When the communication is performed, count the error judged as bit error when received symbol is other than 32 kinds of symbols.	150	**[7.2.4 Fast Link-Loss Detection Function]** ● In the IDLE state when communication is not performed, count the error judged as bit error when received symbol is other than IDLE symbol or J symbol which means the start of frame. Error count is only one when continuous error symbols without normal symbols are received. ● When the communication is performed, count the error judged as bit error when received symbol is other than data code group, IDLE code group or control code group in 32 kinds of symbols. Error count is up whenever error symbol is received.

No.15 7.3.1 Hardware Power-Down Mode
Minimum reset time added

V4.00		V4.01	
Page	Description	Page	Description
150	**[7.3.1 Hardware Power-Down Mode]** The operation is shifted to hardware power-down mode by setting 1 to bit 2 (P0PHYEN) or bit 5（P1PHYEN) in the Ethernet PHY operation mode control register (PHYMD). The Ethernet PHY does not work at all in hardware power-down mode and MII management registers cannot be accessed. The power consumption of the port will be almost 0. To wake up from the hardware power-down mode, set 0 to bit 2 (P0PHYEN) or bit 5 (P1PHYEN) in the Ethernet PHY operation mode control register (PHYMD). When returning from the hardware power-down mode, both analog and digital circuits are initialized by the Ethernet PHY and so are MII management registers.	151	**[7.3.1 Hardware Power-Down Mode]** The operation is shifted to hardware power-down mode by setting 1 to bit 2 (P0PHYEN) or bit 5（P1PHYEN) in the Ethernet PHY operation mode control register (PHYMD). The Ethernet PHY does not work at all in hardware power-down mode and MII management registers cannot be accessed. The power consumption of the port will be almost 0. To wake up from the hardware power-down mode, set 0 to bit 2 (P0PHYEN) or bit 5 (P1PHYEN) in the Ethernet PHY operation mode control register (PHYMD). When returning from the hardware power-down mode, both analog and digital circuits are initialized by the Ethernet PHY and so are MII management registers. Hardware power-down mode must be kept for more than 100us.

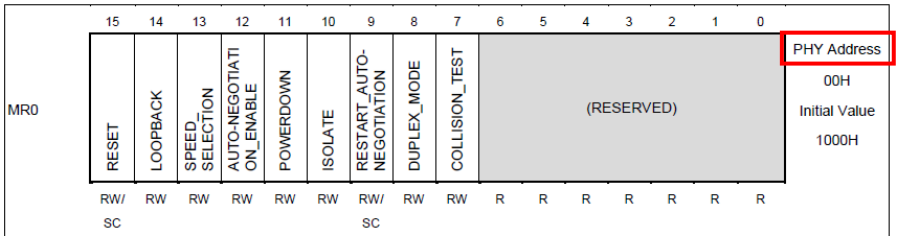
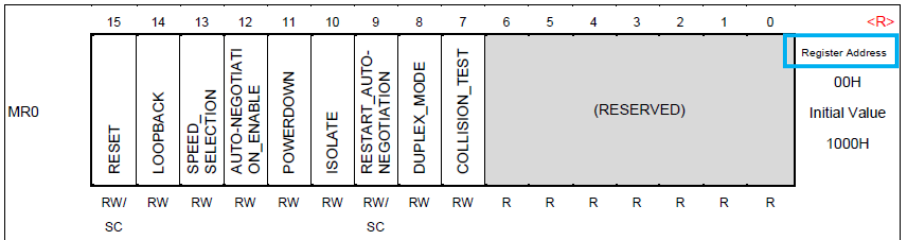
No.16 7.4 MII Management Registers in Ethernet PHY

Explanation about the symbols below bit name of registers added

V4.00		V4.01	
Page	Description	Page	Description
151	**[7.4 MII Management Registers in Ethernet PHY]** (No entry)	153	**[7.4 MII Management Registers in Ethernet PHY]** Symbols except R and W below bit names in each register section mean the following. SC : Self clearing after process completion LL : Latching low level, clear on read of register LH : Latching high level, clear on read of register NASR : Not initialized by software power-down mode

No.17 7.4.1 Register 0 – Control Register to 7.4.24 Register 31 – PHY Special Control/Status Register

Description changed PHY Address to Register Address

V4.00		V4.01	
Page	Description	Page	Description
152-174	**[7.4.1 Register 0 – Control Register to 7.4.24 Register 31 – PHY Special Control/Status Register]** 	154-176	**[7.4.1 Register 0 – Control Register to 7.4.24 Register 31 – PHY Special Control/Status Register]** 

No.18 7.5.3 Ethernet PHY Power-Up Status Register (PHYPUS)

Time for bits to be cleared added

V4.00		V4.01	
Page	Description	Page	Description
177	**[7.5.3 Ethernet PHY Power-Up Status Register (PHYPUS)]** PHYPUS is used to confirm the power-up state of the built-in Ethernet PHY. This register is readable only in 32 bits.	179	**[7.5.3 Ethernet PHY Power-Up Status Register (PHYPUS)]** PHYPUS is used to confirm the power-up state of the built-in Ethernet PHY. This register is readable only in 32 bits. When hardware power-down mode is released, bit1 and/or bit0 are cleared around 5.2ms later.

No.19 7.6 LED signal

Explanation of LED signal added

V4.00		V4.01	
Page	Description	Page	Description
-	(No entry)	180	**[7.6 LED signal]** **Newly added**