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RENESAS TECHNICAL UPDATE

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Product Category	System LSI	Document No.	TN-RIN-A007A/E	Rev.	1.00
Title	Notification of R-IN32M3 Series Datasheet (Rev.3.01 to Rev.4.00) Revised contents: Corrections and new functions		Information Category	Technical Notification	
Applicable Product	See following	Lot No. All lots	Reference Document	R-IN32M3 Series Datasheet Rev.4.00 (R18DS0008EJ0400)	

R-IN32M3 Series Datasheet Rev. 4.00 (R18DS0008EJ0400) has been released on Renesas website. For details, see "2. Documentation Updates" as below. In addition, as the item marked with "caution needed" may cause a failure on the device. Please confirm the item if it corresponds to your usage.

1 Applicable Product

Product Type	Model Marking	Product Code
R-IN32M3-EC	MC-10287F1	MC-10287F1-HN4-A
		MC-10287F1-HN4-M1-A
	MC-10287BF1	MC-10287BF1-HN4-A
		MC-10287BF1-HN4-M1-A
R-IN32M3-CL	D60510F1	UPD60510F1-HN4-A
		UPD60510F1-HN4-M1-A
	D60510BF1	UPD60510BF1-HN4-A
		UPD60510BF1-HN4-M1-A

2 Documentation Updates

No	Applicable Item (Rev.4.00 Section)	Applicable Page (Rev4.00)	Contents	
			MC-10287F1 UPD60510F1	MC-10287BF1 UPD60510BF1
1	2.3 Signals by Function	p.14	Description revised	←
2	2.3.1(1) PHY Interface (R-IN32M3-CL only)	p.15	Complement	←
3	2.3.3 External Memory Interface Signals	p.19	Complement	←
4	2.3.11 Trace Signals	p.27	Errors corrected	←
5	2.3.14 CC-Link IE Field (Intelligent device station) Signals (R-IN32M3-CL only) *caution needed	p.29	Complement	←
6	2.3.15 CC-Link Signals (Intelligent device station)	p.30	Description revised	←
7	2.3.16 CC-Link Signals (Remote device station)	p.31	Description revised	←
8	2.3.17 System Signals	p.32-33	Complement	←
9	2.3.19 Operation Mode Setting Signal	p.36	Complement	←
10	2.4.3 System Signals	p.39	Description revised	←
11	2.4.6 Operation Mode Setting Signal	p.42	Description revised	←
12	3.3 EtherCAT Slave Controller Function (R-IN32M3-EC only)	p.46	Errors corrected	←
13	3.8.1 Features	p.51	Functions newly added	←
14	3.20 Hardware Real-time OS	p.65-66	Description revised	←
15	4.6 Terminal Capacity Values	p.72	Complement	←
16	4.8.1(1) Input clock characteristics	p.74	Description revised	←
17	4.8.3 External Memory Interface Signals	p.78-82	Complement	←
18	4.8.6 External DMA Interface	p.100	Errors corrected	←
19	4.8.7 CSI Interface	p.101-102	Complement	←
20	4.8.10 Ethernet Interface (R-IN32M3-CL only)	p.105-106	Errors corrected	←
21	4.8.11(2) Trace Interface *caution needed	p.107	Errors corrected	←

(← : same as on the left)

Incorrect and correct: highlighted in yellow

1. 2.3 Signals by Function
"Table2.1 Meanings of the Items in the List of Pins", "Table2.2 Meanings of the Symbols and Abbreviations in the List of Pins" added.
Symbol and Abbreviation unified. (p.14)

Rev3.01:

2.3 Signals by Function

No descriptions

Rev4.00:

2.3 Signals by Function

The meanings of the symbols and abbreviations used in this document are given below.

Table2.1 Meanings of the Items in the List of Pins

Item	Meaning
Pin Name	Name of the pin shown in section 2.1, Pin Placement (R-IN32M3-EC Top View), 2.2, Pin Placement (R-IN32M3-CL Top View).
I/O	I/O direction of the given pin
Function	Summary of the given pin function
Active	Active level of the given pin
Level during reset	Indicates the pin state while RSTOUTZ = Low. For details see the R-IN32M3 Series User's Manual (Peripheral Modules).

Table2.2 Meanings of the Symbols and Abbreviations in the List of Pins

Target	Symbol and Abbreviation	Meaning
Pin Name	- (hyphen)	Indicates that the pin is a dedicated pin and is not multiplexed with a port-pin function.
I/O	- (hyphen)	Indicates that the pin is a pin such as a power supply or ground pin and so does not have an I/O direction.
Active	- (hyphen)	Indicates that there is no active level (clock signals, data bus, and address bus).
	High	The active level is high.
	Low	The active level is low.
Level during Reset	- (hyphen)	Indicates an input-dedicated pin that has no initial level or state following a reset.
	High	The pin state during a reset is high.
	Low	The pin state during a reset is low.
	Hi-Z (High)	The pin state during a reset is Hi-Z (High) with the internal pull-up resistor pulling it to the high level.
	Hi-Z (Low)	The pin state during a reset is Hi-Z (Low) with the internal pull-up resistor pulling it to the low level.

2. 2.3.1(1) PHY Interface (R-IN32M3-CL only)

"Level during reset" of ETHn_GTXC, ETHn_TXEN, ETHn_TXER, ETHn_TXD0-7 (n:0-1), modified. (p.15)

Rev3.01:

2.3.1 Ethernet Signals

(1) PHY Interface (R-IN32M3-CL only)

Caution These signals apply to R-IN32M3-CL only.

Pin Name	I/O	Function	Active	Level during reset
ETH0_TXC	I	Ethernet 0 10M/100M Transmit clock port (2.5MHz/25MHz)	↑	-
ETH0_GTXC	O	Ethernet 0 1G Transmit clock port (125MHz)	↑	- Note
ETH0_TXEN	O	Ethernet 0 Transmit enable port	High	Low
ETH0_TXER	O	Ethernet 0 Transmit error port	High	Low
ETH0_TXD0-ETH0_TXD7	O	Ethernet 0 Transmit data port	-	Low
ETH0_GE_INT	I	Ethernet 0 PHY interrupt port	High/Low	-
ETH0_RXC	I	Ethernet 0 Receive clock port	↑	-
ETH0_RXDV	I	Ethernet 0 Receive enable port	High	-
ETH0_RXER	I	Ethernet 0 Receive error port	High	-
ETH0_RXD0-ETH0_RXD7	I	Ethernet 0 Receive data port	-	-
ETH0_CRS	I	Ethernet 0 Carrier sense port	High	-
ETH0_COL	I	Ethernet 0 Collision port	High	-
ETH1_TXC	I	Ethernet 1 10M/100M Transmit clock port (2.5MHz/25MHz)	↑	-
ETH1_GTXC	O	Ethernet 1 1G Transmit clock port (125MHz)	↑	- Note
ETH1_TXEN	O	Ethernet 1 Transmit enable port	High	Low
ETH1_TXER	O	Ethernet 1 Transmit error port	High	Low
ETH1_TXD0-ETH1_TXD7	O	Ethernet 1 Transmit data port	↑	Low
ETH1_GE_INT	I	Ethernet 1 PHY interrupt port	High/Low	-
ETH1_RXC	I	Ethernet 1 Receive clock port	-	-
ETH1_RXDV	I	Ethernet 1 Receive enable port	High	-
ETH1_RXER	I	Ethernet 1 Receive error port	High	-
ETH1_RXD0-ETH1_RXD7	I	Ethernet 1 Receive data port	-	-
ETH1_CRS	I	Ethernet 1 Carrier sense port	High	-
ETH1_COL	I	Ethernet 1 Collision port	High	-
ETH_MDC	O	Ethernet Serial management interface clock	↑	Low
ETH_MDIO	I/O	Ethernet Serial management interface data input/output	-	Hi-Z

Note. Out put the 125MHz clock.

Rev4.00:

2.3.1 Ethernet Signals

(1) PHY Interface (R-IN32M3-CL only)

Caution These signals apply to R-IN32M3-CL only.

Pin Name	I/O	Function	Active	Level during reset
ETH0_TXC	I	Ethernet 0 10M/100M Transmit clock port (2.5MHz/25MHz)	-	-
ETH0_GTXC	O	Ethernet 0 1G Transmit clock port (125MHz)	-	High Note
ETH0_TXEN	O	Ethernet 0 Transmit enable port	High	Low Note
ETH0_TXER	O	Ethernet 0 Transmit error port	High	Low Note
ETH0_TXD0-ETH0_TXD7	O	Ethernet 0 Transmit data port	-	Low Note
ETH0_GE_INT	I	Ethernet 0 PHY interrupt port	High/Low	-
ETH0_RXC	I	Ethernet 0 Receive clock port	-	-
ETH0_RXDV	I	Ethernet 0 Receive enable port	High	-
ETH0_RXER	I	Ethernet 0 Receive error port	High	-
ETH0_RXD0-ETH0_RXD7	I	Ethernet 0 Receive data port	-	-
ETH0_CRS	I	Ethernet 0 Carrier sense port	High	-
ETH0_COL	I	Ethernet 0 Collision port	High	-
ETH1_TXC	I	Ethernet 1 10M/100M Transmit clock port (2.5MHz/25MHz)	-	-
ETH1_GTXC	O	Ethernet 1 1G Transmit clock port (125MHz)	-	High Note
ETH1_TXEN	O	Ethernet 1 Transmit enable port	High	Low Note
ETH1_TXER	O	Ethernet 1 Transmit error port	High	Low Note
ETH1_TXD0-ETH1_TXD7	O	Ethernet 1 Transmit data port	-	Low Note
ETH1_GE_INT	I	Ethernet 1 PHY interrupt port	High/Low	-
ETH1_RXC	I	Ethernet 1 Receive clock port	-	-
ETH1_RXDV	I	Ethernet 1 Receive enable port	High	-
ETH1_RXER	I	Ethernet 1 Receive error port	High	-
ETH1_RXD0-ETH1_RXD7	I	Ethernet 1 Receive data port	-	-
ETH1_CRS	I	Ethernet 1 Carrier sense port	High	-
ETH1_COL	I	Ethernet 1 Collision port	High	-
ETH_MDC	O	Ethernet Serial management interface clock	-	Low
ETH_MDIO	I/O	Ethernet Serial management interface data input/output	-	Hi-Z

Note. The driving ability can be switched by the setting of the ETHDRCTRL register. For details, see section 7.3.3.2, Ethernet Interface Buffer Function Select Register (ETHDRCTRL), in the R-IN32M3 Series User's Manual (Peripheral Modules).

* Applicable item except yellow hatched is unificated description.

3. 2.3.3 External Memory Interface Signals

"Pin Name" of Synchronous burst access memory controller (MA0-MA26, MD0-MD31), added.
"Level during Reset" of BUSCLK Signal, modified. Note1 modified, Note4 added. (p.19)

Rev3.01:

2.3.3 External Memory Interface Signals

Pin Name	I/O	Function	Shared Signal	Shared port	Active	Level during reset
BUSCLK	O	Bus clock output port	-	-	-	-
CSZ0	O	Chip select signal output port	HCSZ	-	Low	Hi-Z With internal pull-up resistor
CSZ1	O		HPGCSZ	P44		
CSZ2	O		-	P51		
CSZ3	O		-	P50		
A1	O	Address output port	HA1	P40	-	Hi-Z With internal pull-up resistor
A2-A20	O		HA2-HA20	-		Hi-Z With internal pull-down resistor
A21-A27	O		-	RP21-RP27		
D0-D15 Note1	I/O	Data bus port	HD0-HD15	-		
D16-D31 Note1	I/O		HD16-HD31	RP30-RP37 RP10-RP17	-	Hi-Z With internal pull-up resistor
RDZ	O	Read strobe output port	HRDZ	-	Low	Hi-Z With internal pull-up resistor
WRSTBZ	O	Write strobe output port	HWRSTBZ	-	Low	
WRZ0, WRZ1/ BENZ0, BENZ1	O	Effectively Byte lane strobe output port	HWRZ0, HWRZ1/ HBENZ0, HBENZ1	-	Low	
WRZ2, WRZ3/ BENZ2, BENZ3	O		HWRZ2, HWRZ3/ HBENZ2, HBENZ3	RP06, RP07		
WAITZ	I	Wait signal input port	HWAITZ	P41	Low	Hi-Z With internal pull-up resistor
WAITZ1-WAITZ3 Note2			-	P45-P47		
BCYSTZ / ADVZ Note3	O	Address valid output port	HBCYSTZ	RP20	Low	Hi-Z With internal pull-up resistor

Remark External Memory Interface Signal expects BUSCLK is an input signal while the internal reset signal (HRESETZ) is active.

Note1. If the ADMUXMODE pin is at the high level, these pin functions are multiplexed with address pin functions.
2. This port is available only when using synchronous burst access MEMC.
3. This port functions as BCYSTZ when using asynchronous SRAM MEMC, it functions as ADVZ when using synchronous burst access MEMC

Rev4.00:

2.3.3 External Memory Interface Signals

Pin Name	I/O	Function	Shared Signal	Shared port	Active	Level during reset
BUSCLK	O	Bus clock output port	-	-	-	clock output
CSZ0	O	Chip select signal output port	HCSZ	-	Low	Hi-Z (High)
CSZ1	O		HPGCSZ	P44		
CSZ2	O		-	P51		
CSZ3	O		-	P50		
A1 / MA0 Note4	O	Address output port	HA1	P40	-	Hi-Z (High)
A2-A20 / MA1-MA19 Note4	O		HA2-HA20	-		Hi-Z (Low)
A21-A27 / MA20-MA26 Note4	O		-	RP21-RP27		
D0-D15 / MD0-MD15 / MA0-MA15 Note1,4	I/O	Data bus port	HD0-HD15	-		
D16-D31 / MD16-MD31 / MA16-MA31 Note1,4	I/O		HD16-HD31	RP30-RP37 RP10-RP17	-	Hi-Z (High)
RDZ	O	Read strobe output port	HRDZ	-	Low	Hi-Z (High)
WRSTBZ	O	Write strobe output port	HWRSTBZ	-	Low	
WRZ0, WRZ1/ BENZ0, BENZ1	O	Effectively Byte lane strobe output port	HWRZ0, HWRZ1/ HBENZ0, HBENZ1	-	Low	
WRZ2, WRZ3/ BENZ2, BENZ3	O		HWRZ2, HWRZ3/ HBENZ2, HBENZ3	RP06, RP07		
WAITZ	I	Wait signal input port	HWAITZ	P41	Low	Hi-Z (High)
WAITZ1-WAITZ3 Note2			-	P45-P47		
BCYSTZ / ADVZ Note3	O	Address valid output port	HBCYSTZ	RP20	Low	Hi-Z (High)

Remark External Memory Interface Signal expects BUSCLK is an input signal while the internal reset signal (HRESETZ) is active.

Note1. If the ADMUXMODE pin is at the high level, these pin functions are multiplexed with address pin functions.
ADMUXMODE = 0: MD0-MD31 (separated address and data lines)
ADMUXMODE = 1: MD0-MD31/MA0-MA31 (multiplexed address and data lines)
2. This port is available only when using synchronous burst access MEMC.
3. This port functions as BCYSTZ when using asynchronous SRAM MEMC, it functions as ADVZ when using synchronous burst access MEMC
4. This pin functions as A1-A27 and D0-D31 functions when the asynchronous SRAM memory controller is in use and as MA1-MA26 and MD0-MD31 functions when the synchronous burst access memory controller is in use.

* Applicable item except yellow hatched is unificated description.

4. 2.3.11 Trace Signals

"Level during reset" of TRACECLK signal, modified. (p.27)

Rev3.01:

2.3.11 Trace Signals

Pin Name	I/O	Function	Active	Level during reset
TRACECLK	O	Trace port clock output port	-	-
TRACEDATA3-TRACEDATA0	O	Trace port data output port	-	Low

Rev4.00:

2.3.11 Trace Signals

Pin Name	I/O	Function	Active	Level during reset
TRACECLK	O	Trace port clock output port	-	clock output
TRACEDATA3-TRACEDATA0	O	Trace port data output port	-	Low

* Applicable item except yellow hatched is unificated description.

5. 2.3.14 CC-Link IE Field (Intelligent device station) Signals (R-IN32M3-CL only)
Note for CCI_WAITEDGEH, CCI_WRLENH signals, added. (p.29)

Rev3.01:

2.3.14 CC-Link IE Field (Intelligent device station) Signals (R-IN32M3-CL only)

Pin Name	I/O	Function	Shared Port	Active	Level during reset
CCI_RUNLEDZ	O	RUN LED control port	P00	Low	Hi-Z With internal pull-up resistor
CCI_DLINKLEDZ	O	Cyclic communication status check LED control port	P02	Low	
CCI_ERRLEDZ	O	Field Network Error LED control port	P03	Low	
CCI_LERR1LEDZ	O	Link error LED control port 1	P04	Low	
CCI_LERR2LEDZ	O	Link error LED control port 2	P05	Low	
CCI_SDLEDZ	O	Transfer data LED control port	P06	Low	
CCI_RDLEDZ	O	Receive data LED control port	P07	Low	
CCI_NMIZ	O	Output NMI interrupt to MPU	P12	Low	Hi-Z With internal pull-up resistor
CCI_WDTIZ	I	Input from Watchdog Timer	P13	Low	
CCI_WAITEDGEH	I/O	Wait Synchronized edge setting 0：rise edge mode 1：low edge mode	P33	-	
CCI_WRLENH	I/O	WRL enable setting 0：byte write enable mode 1：byte enable mode	P34	-	
CCI_PHYREZ1	O	PHY reset output 1 port	P56	Low	
CCI_PHYREZ0	O	PHY reset output 0 port	P57	Low	
CCI_INTZ	O	Output Interrupt signal to MPU	P66	Low	
CCI_CLK2_097M	I	2.097152MHz clock	-	-	-

Rev4.00:

2.3.14 CC-Link IE Field (Intelligent device station) Signals (R-IN32M3-CL only)

Pin Name	I/O	Function	Shared Port	Active	Level during reset
CCI_RUNLEDZ	O	RUN LED control port	P00	Low	Hi-Z (High)
CCI_DLINKLEDZ	O	Cyclic communication status check LED control port	P02	Low	
CCI_ERRLEDZ	O	Field Network Error LED control port	P03	Low	
CCI_LERR1LEDZ	O	Link error LED control port 1	P04	Low	
CCI_LERR2LEDZ	O	Link error LED control port 2	P05	Low	
CCI_SDLEDZ	O	Transfer data LED control port	P06	Low	
CCI_RDLEDZ	O	Receive data LED control port	P07	Low	
CCI_NMIZ	O	Output NMI interrupt to MPU	P12	Low	Hi-Z (High)
CCI_WDTIZ	I	Input from Watchdog Timer	P13	Low	
CCI_WAITEDGEH Note	I/O	Wait Synchronized edge setting 0：rise edge mode 1：low edge mode	P33	-	
CCI_WRLENH Note	I/O	WRL enable setting 0：byte write enable mode 1：byte enable mode	P34	-	
CCI_PHYREZ1	O	PHY reset output 1 port	P56	Low	
CCI_PHYREZ0	O	PHY reset output 0 port	P57	Low	
CCI_INTZ	O	Output Interrupt signal to MPU	P66	Low	
CCI_CLK2_097M	I	2.097152MHz clock	-	-	-

Note. When user does boot with the external memory boot mode, external serial flash ROM boot mode, or instruction RAM boot mode, be sure not to input the low level to P33 (multiplexed with CCI_WAITEDGEH) and P34 (CCI_WRLENH) pins during a reset.
P33 and P34 pins should be left open circuit or the high level should be input to the pins during a reset. If you input the low level to P33 and P34 pins during a reset, you cannot access the CC-Link IE field from the CPU of the R-IN32M3.

* Applicable item except yellow hatched is unificated description.

6. 2.3.15 CC-Link Signals (Intelligent device station)
"Function" of CCM_CLK80M Signals, modified. (p.30)

Rev3.01:

2.3.15 CC-Link Signals (Intelligent device station)

Pin Name	I/O	Function	Shared Port	Active	Level during reset
CCM_LINKERRZ	O	Link error LED control port	P20	Low	Hi-Z R-IN32M3-EC: Hi-Z (without internal resistor) R-IN32M3-CL: With internal pull-up resistor
CCM_ERRZ	O	Error LED control port	P21	Low	
CCM_RUNZ	O	RUN LED control port	P26	Low	
CCM_MDIN0- CCM_MDIN3	I	Mode setting switch input port	P62-P65	-	
CCM_SNIN0- CCM_SNIN7	I	Station No. setting switch port	P70-P77	-	
CCM_LNKRUNZ	O	Link RUN LED control port	P50	Low	Hi-Z With internal pull-up resistor
CCM_RDLEDZ	O	Receive data LED control port	P51	Low	
CCM_SDLEDZ	O	Transfer data LED control port	RP00	Low	
CCM_IRZ	O	Interrupt output port	P35	Low	
CCM_WDTENZ	I	Watchdog Timer error input port	P13	Low	
CCM_MSTZ	O	Operation check LED port	P37	Low	
CCM_SMSTZ	O	Stand-by master LED control port	RP01	Low	
CCM_RD	I	Data receive port	P53	-	
CCM_SD	O	Data transfer port	P54	-	
CCM_SDGCZ	O	Transfer data & gate control port	P42	Low	
CCM_CLK80M	I	CC-Link Clock	-	-	-

Rev4.00:

2.3.15 CC-Link Signals (Intelligent device station)

Pin Name	I/O	Function	Shared Port	Active	Level during reset
CCM_LINKERRZ	O	Link error LED control port	P20	Low	Note
CCM_ERRZ	O	Error LED control port	P21	Low	
CCM_RUNZ	O	RUN LED control port	P26	Low	
CCM_MDIN0- CCM_MDIN3	I	Mode setting switch input port	P62-P65	-	
CCM_SNIN0- CCM_SNIN7	I	Station No. setting switch port	P70-P77	-	
CCM_LNKRUNZ	O	Link RUN LED control port	P50	Low	Hi-Z (High)
CCM_RDLEDZ	O	Receive data LED control port	P51	Low	
CCM_SDLEDZ	O	Transfer data LED control port	RP00	Low	
CCM_IRZ	O	Interrupt output port	P35	Low	
CCM_WDTENZ	I	Watchdog Timer error input port	P13	Low	
CCM_MSTZ	O	Operation check LED port	P37	Low	
CCM_SMSTZ	O	Stand-by master LED control port	RP01	Low	
CCM_RD	I	Data receive port	P53	-	
CCM_SD	O	Data transfer port	P54	-	
CCM_SDGCZ	O	Transfer data & gate control port	P42	Low	
CCM_CLK80M	I	CC-Link Clock input port (80MHz)	-	-	-

Note. R-IN32M3-EC: Hi-Z, R-IN32M3-CL: Hi-Z (High)

* Applicable item except yellow hatched is unificated description.

7. 2.3.16 CC-Link Signals (Remote device station)

"Function" of CCM_CLK80M Signals, modified. Note2 added. (p.31)

Rev3.01:

2.3.16 CC-Link Signals (Remote device station)

Caution To use a remote device station, it is necessary to connect a CCS_REFSTB pin to an external interrupt pin (INTPZ).

Pin Name	I/O	Function	Shared Port	Active	Level during reset
CCS_MON1-CCS_MON3	O	Monitor port	P32-P34	-	Hi-Z With internal pull-up resistor
CCS_MON4	O	Monitor port	P11	-	Hi-Z With internal pull-down resistor
CCS_MON0	O	Monitor port	P06	-	Hi-Z R-IN32M3-EC: Hi-Z (without internal resistor) R-IN32M3-CL: With internal pull-up resistor
CCS_MON5-CCS_MON7	O	Monitor port	P03-P05	-	
CCS_RESOUT	O	reset port	P07	High	
CCS_IOTENSU	I	Initial setting port	P22	-	
CCS_SENYU0	I	Initial setting port	P23	-	
CCS_SENYU1	I	Initial setting port	P24	-	
CCS_ERRZ	O	Operation check LED port	P25	Low	
CCS_RUNZ	O	Operation check LED port	P26	Low	
CCS_STATION_NO_0-CCS_STATION_NO_7	I	Station No. setting switch port	P70-P77	-	
CCS_LNKRUNZ	O	Link RUN LED control port	P50	Low	Hi-Z With internal pull-up resistor
CCS_REFSTB	O	Interrupt port	P10	High	
CCS_WDTZ	I	Watchdog Timer port	P13	Low	
CCS_RDLEDZ	O	Receive data LED control port	P51	Low	
CCS_RD	I	Data receive port	P53	-	
CCS_SD	O	Data transfer port	P54	-	
CCS_SDLEDZ	O	Operation check LED port	RP00	Low	
CCS_SDGATEON	O	Transfer data & gate control port	P52	High	Hi-Z With internal pull-down resistor
CCS_BS1	I	Baud rate setting switch port	RP02	-	Hi-Z With internal pull-up resistor
CCS_BS2	I	Baud rate setting switch port	RP03	-	
CCS_BS4	I	Baud rate setting switch port	RP04	-	
CCS_BS8	I	Baud rate setting switch port	RP05	-	
CCS_FUSEZ	I	Fuse cutting signal port	P36	Low	
CCM_CLK80M	I	CC-Link operation lock	-	-	-

Rev4.00:

2.3.16 CC-Link Signals (Remote device station)

Caution To use a remote device station, it is necessary to connect a CCS_REFSTB pin to an external interrupt pin (INTPZ).

Pin Name	I/O	Function	Shared Port	Active	Level during reset
CCS_MON1-CCS_MON3	O	Monitor port	P32-P34	-	Hi-Z (High)
CCS_MON4	O	Monitor port	P11	-	Hi-Z (Low)
CCS_MON0	O	Monitor port	P06	-	Note1
CCS_MON5-CCS_MON7	O	Monitor port	P03-P05	-	
CCS_RESOUT	O	reset port	P07	High	
CCS_IOTENSU	I	Initial setting port	P22	-	
CCS_SENYU0	I	Initial setting port	P23	-	
CCS_SENYU1	I	Initial setting port	P24	-	
CCS_ERRZ	O	Operation check LED port	P25	Low	
CCS_RUNZ	O	Operation check LED port	P26	Low	
CCS_STATION_NO_0-CCS_STATION_NO_7	I	Station No. setting switch port	P70-P77	-	
CCS_LNKRUNZ	O	Link RUN LED control port	P50	Low	Hi-Z (High)
CCS_REFSTB	O	Interrupt port	P10	High	
CCS_WDTZ	I	Watchdog Timer port	P13	Low	
CCS_RDLEDZ	O	Receive data LED control port	P51	Low	
CCS_RD	I	Data receive port	P53	-	
CCS_SD	O	Data transfer port	P54	-	
CCS_SDLEDZ	O	Operation check LED port	RP00	Low	
CCS_SDGATEON	O	Transfer data & gate control port	P52	High	Hi-Z (Low)
CCS_BS1	I	Baud rate setting switch port	RP02	-	Hi-Z (High)
CCS_BS2	I	Baud rate setting switch port	RP03	-	
CCS_BS4	I	Baud rate setting switch port	RP04	-	
CCS_BS8	I	Baud rate setting switch port	RP05	-	
CCS_FUSEZ	I	Fuse cutting signal port	P36	Low	
CCM_CLK80M[Note2]	I	CC-Link Clock input port (80MHz)	-	-	-

Note1. R-IN32M3-EC: Hi-Z, R-IN32M3-CL: Hi-Z (High)
2. This Signal is shared with CCM_CLK80M for CC-Link Intelligent device station.

* Applicable item except yellow hatched is unificated description.

8. 2.3.17 System Signals

"Function" of XT1, XT2, OSCTH, JTAGSEL signals, modified. "Active" of OSCTH signal, modified.
"Level during Reset" of RSTOUTZ, CLKOUT25M0/1 signals, modified. (p.32-33)

Rev3.01:

2.3.17 System Signals

Pin Name	I/O	Function	Active	Level during reset
XT1	I	Crystal Oscillator ports for system clock *Oscillator output connects to X2 for direct connection.	-	-
XT2	I/O		-	-
RESETZ	I	Reset input port	Low	-
HOTRESETZ Note1	I	Hot reset Input port	Low	-
PONRZ	I	Internal RAM Power on reset input port	Low	-
OSCTH	I	Input High level when external clock input mode	-	-
JTAGSEL	I	JTAG Operation mode setting port	-	-
RSTOUTZ	O	Reset to external circuit output port	Low	-
CLKOUT25M0 Note1	O	PHY clock output port	-	-
CLKOUT25M1 Note1	O	PHY clock output port	-	-
PLL_VDD	-	PLL power supply (1.0V)	-	-
PLL_GND	-	PLL power Ground supply (GND)	-	-
VDD33	-	I/O power supply (3.3V)	-	-
VDD10	-	Internal power supply (1.0V)	-	-
GND	-	Ground supply (GND)	-	-
VDDQ_MII Note1	-	Ethernet I/O power supply (3.3V)	-	-
LX Note2	O	Regulator 1.5V power Output	-	-
EXTRES Note2	-	Reference resistor for EtherPHY connect port	-	-
P0VDDARXTX Note2	-	Analog Port Rx/Tx power supply (1.5V) - Port 0	-	-
P1VDDARXTX Note2	-	Analog Port Rx/Tx power supply (1.5V) - Port 0	-	-
VDDACB Note2	-	EtherPHY Analog Central power supply (3.3V)	-	-
AGND Note2	-	EtherPHY Analog Ground supply (GND)	-	-
VDD15 Note2	-	EtherPHY power supply (1.5V)	-	-
VDDAPLL Note2	-	EtherPHY Analog Central power supply (1.5V)	-	-
VSSAPLLCB Note2	-	EtherPHY Analog Central Ground supply (GND)	-	-
VDD33ESD Note2	-	EtherPHY Analog Test power supply (3.3V)	-	-
AVDD_REG Note2	-	Regulator Analog power supply (3.3V)	-	-
AGND_REG Note2	-	Regulator Analog Ground supply (GND)	-	-
BVDD Note2	-	Regulator power supply (3.3V)	-	-
BGND Note2	-	Regulator Ground supply (GND)	-	-
FB Note2	I	Regulator Feedback port	-	-
VDDQ_PECL_B0 Note2	-	PECL Buffer supply (3.3V)	-	-
VDDQ_PECL_B1 Note2	-	PECL Buffer supply (3.3V)	-	-

Note1. Only applies to R-IN32M3-CL.
Note2. Only applies to R-IN32M3-EC.

Rev4.00:

2.3.17 System Signals

(1/2)

Pin Name	I/O	Function	Active	Level during reset
XT1	I	Clock input pin OSCTH = 1: Oscillator is in use. XT1 and XT2 are respectively connected to GND and oscillator. OSCTH = 0: Resonator is in use. XT1 and XT2 are connected to resonator.	-	-
XT2	I/O		-	-
RESETZ	I	Reset input port	Low	-
HOTRESETZ Note1	I	Hot reset Input port	Low	-
PONRZ	I	Internal RAM Power on reset input port	Low	-
OSCTH	I	External clock input mode setting 0: Resonator connection mode 1: External clock input mode	High	-
JTAGSEL	I	JTAG pin operating mode setting 0: Cortex-M3 JTAG mode 1: B-SCAN JTAG mode	-	-
RSTOUTZ	O	Reset to external circuit output port	Low	Low
CLKOUT25M0 Note1	O	PHY clock output port	-	Note2
CLKOUT25M1 Note1	O	PHY clock output port	-	
PLL_VDD	-	PLL power supply (1.0V)	-	-
PLL_GND	-	PLL power Ground supply (GND)	-	-
VDD33	-	I/O power supply (3.3V)	-	-
VDD10	-	Internal power supply (1.0V)	-	-
GND	-	Ground supply (GND)	-	-
VDDQ_MII Note1	-	Ethernet I/O power supply (3.3V)	-	-

Note1. Only applies to R-IN32M3-CL.
Note2. Oscillation source is passed through to these pins.

(2/2)

Pin Name	I/O	Function	Active	Level during reset
LX Note	O	Regulator 1.5V power Output	-	-
EXTRES Note	-	Reference resistor for EtherPHY connect port	-	-
P0VDDARXTX Note	-	Analog Port Rx/Tx power supply (1.5V) - Port 0	-	-
P1VDDARXTX Note	-	Analog Port Rx/Tx power supply (1.5V) - Port 0	-	-
VDDACB Note	-	EtherPHY Analog Central power supply (3.3V)	-	-
AGND Note	-	EtherPHY Analog Ground supply (GND)	-	-
VDD15 Note	-	EtherPHY power supply (1.5V)	-	-
VDDAPLL Note	-	EtherPHY Analog Central power supply (1.5V)	-	-
VSSAPLLCB Note	-	EtherPHY Analog Central Ground supply (GND)	-	-
VDD33ESD Note	-	EtherPHY Analog Test power supply (3.3V)	-	-
AVDD_REG Note	-	Regulator Analog power supply (3.3V)	-	-
AGND_REG Note	-	Regulator Analog Ground supply (GND)	-	-
BVDD Note	-	Regulator power supply (3.3V)	-	-
BGND Note	-	Regulator Ground supply (GND)	-	-
FB Note	I	Regulator Feedback port	-	-
VDDQ_PECL_B0 Note	-	PECL Buffer supply (3.3V)	-	-
VDDQ_PECL_B1 Note	-	PECL Buffer supply (3.3V)	-	-

Note. Only applies to R-IN32M3-EC.

* Applicable item except yellow hatched is unificated description.

9. 2.3.19 Operation Mode Setting Signal

The Combinations of available operating mode, added. (p.36)

Rev3.01:

No descriptions.

Rev4.00:

The combinations of available operating mode setting pins in this product are as follows.

Boot Mode	External Memory Boot				External MCU Boot				External Serial Flash ROM Boot							
External memory interface	Slave memory interface				External MPU Interface				Slave memory interface				External MPU Interface			
MEMC type	Asynchronous		Synchronous		Asynchronous		Synchronous		Asynchronous		Synchronous		Asynchronous		Synchronous	
External bus width	16bit	32bit	16bit	32bit	16bit	32bit	16bit	32bit	16bit	32bit	16bit	32bit	16bit	32bit	16bit	32bit
BOOT1-0	00	00	00	00	10	10	10	10	01	01	01	01	01	01	01	01
MEMIFSEL	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
MEMCSEL	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
BUS32EN	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
HIFSYNC	0	0	0	0	Note1	Note1	1	1	0	0	0	0	Note1	Note1	1	1
HWRZSEL	0	0	0	0	Note2	Note2	0	0	0	0	0	0	Note2	Note2	0	0
ADMUXMODE	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1

Caution. Any combination of operating mode setting pins other than the above is prohibited.

Note1. The mode of the external MCU interface is selectable by the level on the HIFSYNC pin.
HIFSYNC = 0: Asynchronous SRAM interface mode
HIFSYNC = 1: Synchronous SRAM interface mode
For details, see section 11, External MCU Interface, in the R-IN32M3 Series User's Manual: Peripherals.
Note2. The external MCU interface HWRZ or HBENZ is selectable by the level on the HWRZSEL pin.
For details, see section 2.3.3, External Memory Interface Signals.

Remark1. The combination of operating-mode setting pins used to select booting for instruction RAM (BOOT1-0 = 11) is the same as that for booting from external memory (BOOT1-0 = 00).
Remark2. Asynchronous: asynchronous SRAM memory controller (MEMCSEL = 0)
Synchronous: synchronous burst access memory controller (MEMCSEL = 1)

10. 2.4.3 System Signals

"Recommended connection when not in use" of OSCTH, JTAGSEL, modified. (p.39)

Rev3.01:

2.4.3 System Signals

Pin Name	I/O	Interface	Recommended connection when not in use
NMIZ	I	Input Buffer (3.3V) Schmitt in 50kΩ Pull-up	Connect to VDD33 (3.3V)
XT1	I	Oscillator with EN	Connect to GND
XT2	-		-
RSTOUTZ	O	Output Buffer (3.3V) 6mA	Open
RESETZ	I	Input Buffer (3.3V) Schmitt in	-
PONRZ			
HOTRESETZ			Connect to VDD33 (3.3V)
OSCTH	I	Input Buffer (3.3V) Schmitt in, 50kΩ Pull-down	-
JTAGSEL			

Rev4.00:

2.4.3 System Signals

Pin Name	I/O	Interface	Recommended connection when not in use
NMIZ	I	Input Buffer (3.3V) Schmitt in 50kΩ Pull-up	Connect to VDD33 (3.3V)
XT1	I	Oscillator with EN	Connect to GND
XT2	I/O		-
RSTOUTZ	O	Output Buffer (3.3V) 6mA	Open
RESETZ	I	Input Buffer (3.3V) Schmitt in	-
PONRZ			
HOTRESETZ			Connect to VDD33 (3.3V)
OSCTH	I	Input Buffer (3.3V) Schmitt in, 50kΩ Pull-down	Set these pins according to the operating mode
JTAGSEL			

* Applicable item except yellow hatched is unificated description.

11. 2.4.6 Operation Mode Setting Signals
"Recommended connection when not in use", modified. (p.42)

Rev3.01:

2.4.6 Operation Mode Setting Signals

Pin Name	I/O	Interface	Recommended connection when not in use
BOOT0, BOOT1	I	Input Buffer (3.3V) Schmitt in	-
MEMIFSEL			
BUS32EN			
HIFSYNC			
HWRZSEL			
MEMCSEL			
ADMUXMODE			

Rev4.00:

2.4.6 Operation Mode Setting Signals

Pin Name	I/O	Interface	Recommended connection when not in use
BOOT0, BOOT1	I	Input Buffer (3.3V) Schmitt in	Set these pins according to the operating mode
MEMIFSEL			
BUS32EN			
HIFSYNC			
HWRZSEL			
MEMCSEL			
ADMUXMODE			

12. 3.3 EtherCAT Slave Controller Function (R-IN32M3-EC only) “Table3.1 Features of EtherCAT Slave Controller”, modified. (p.46)

Rev3.01:

3.3 EtherCAT Slave Controller Function (R-IN32M3-EC only)

The EtherCAT Slave Controller (ESC) core is made by Beckhoff Automation GmbH, Germany.
The ESC processes EtherCAT communications and acts as interface between EtherCAT Field bus and Slave applications.

Table3.1 Features of EtherCAT Slave Controller

Feature	R-IN32M3-EC	ET1100	Remark
Ports	2	2-4	-
FMMUs	8	8	-
SyncManagers	8	8	-
RAM [Kbytes]	8	8	-
Distributed Clocks	64bit	64bit	-
EBus	No	Yes (0-4)	-
Process Data Interfaces			
Digital I/O	No	Yes	-
SPI Slave	No	Yes	-
External MPU Interface	Cortex-M3 and 16bit/32bit, async./sync. SRAM Host Interface	8bit/16bit, async./sync.	R-IN32M3 does not support direct access to the ESC from an external CPU.

Rev4.00:

3.3 EtherCAT Slave Controller Function (R-IN32M3-EC only)

The EtherCAT Slave Controller (ESC) core is made by Beckhoff Automation GmbH, Germany.
The ESC processes EtherCAT communications and acts as interface between EtherCAT Field bus and Slave applications.

Table3.1 Features of EtherCAT Slave Controller

Feature	R-IN32M3-EC	ET1100
Ports	2	2-4
FMMUs	8	8
SyncManagers	8	8
RAM [Kbytes]	8	8
Distributed Clocks	64bit	64bit
EBus	No	Yes (0-4)
Process Data Interfaces	-	-
Digital I/O	No	Yes
SPI Slave	No	Yes
External MPU Interface	On-chip bus (External MPU Interface)	8bit/16bit, async./sync.

Caution Register area (0E_0000H-0E_0F7FH) can't be accessed from the external MPU I/F.

13. 3.8.1 Features

External event count function added. (p.51)

Rev3.01:

3.8 Timer Array Unit

3.8.1 Features

- 1 Unit (4 channels)
- 32-bit counter and 32-bit data registers per channel
- Independent channel operation
- Synchronous channel operation (master and slave operation)
- Generation of different types of output signals
- Counter can be triggered by an external signal
- Interrupt generation

Independent channel operation	Synchronous channel operation
Independent channel operation functions	Synchronous channel operation function
Interval timer function	PWM output function
External input interval timer function	
Independent channel signal measurement functions	
Overflow interrupt output function (during External width measurement)	
External input period count detection function	
External input pulse interval judgment function	
External input signal width judgment function	
Other independent channel function	
External input position detection function	

Rev4.00:

3.8 Timer Array Unit

3.8.1 Features

- 1 Unit (4 channels)
- 32-bit counter and 32-bit data registers per channel
- Independent channel operation
- Synchronous channel operation (master and slave operation)
- Generation of different types of output signals
- Counter can be triggered by an external signal
- Interrupt generation

Independent channel operation	Synchronous channel operation
Independent channel operation functions	Synchronous channel operation function
Interval timer function	PWM output function
External input interval timer function	
External event count function	
Independent channel signal measurement functions	
Overflow interrupt output function (during External width measurement)	
External input period count detection function	
External input pulse interval judgment function	
External input signal width judgment function	
Other independent channel function	
External input position detection function	

14. 3.20 Hardware Real-time OS

QINT description modified. “3.20.2 Service Calls” deleted. (p.65-66)

Rev3.01:

3.20 Hardware Real-time OS

The Hardware Real-time OS supports 30 types of system-calls including event, semaphore and mailbox.

3.20.1 Features

- Task Scheduler
  - Hardware ISR : Maximum 32 selectable from 128 QINTs
  - Contexts : 64
  - Semaphores : 128
  - Events : 64
  - Mailboxes : 64
  - Mailbox elements : 92
  - Context priorities: 16
- Hardware Function Manager

Rev4.00:

3.20 Hardware Real-time OS

The Hardware Real-time OS supports 30 types of system-calls including event, semaphore and mailbox.

3.20.1 Features

- Task Scheduler
  - Hardware ISR : Maximum 32 selectable from 128 interrupts
  - Contexts : 64
  - Semaphores : 128
  - Events : 64
  - Mailboxes : 64
  - Mailbox elements : 192
  - Context priorities: 16
- Hardware Function Manager

Remark The hardware real-time OS can be controlled by using the µITRON system calls provided by the sample driver. For how to use the driver, see the R-IN32M3 Series Programming Manual (OS edition).

* Applicable item except yellow hatched is unificated description.

14. 3.20 Hardware Real-time OS

QINT description modified. “3.20.2 Service Calls” deleted. (p.65-66) continued

Rev3.01:

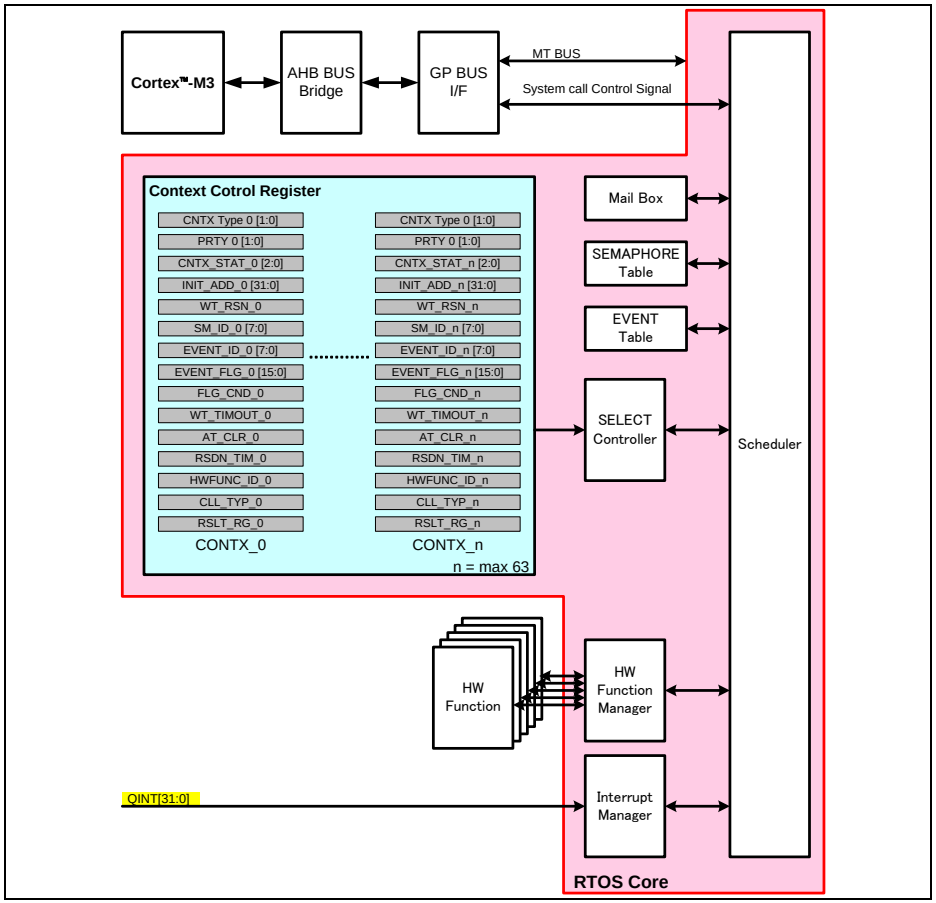

Figure3.1 Structure of Hardware Real-time OS

Rev4.00:

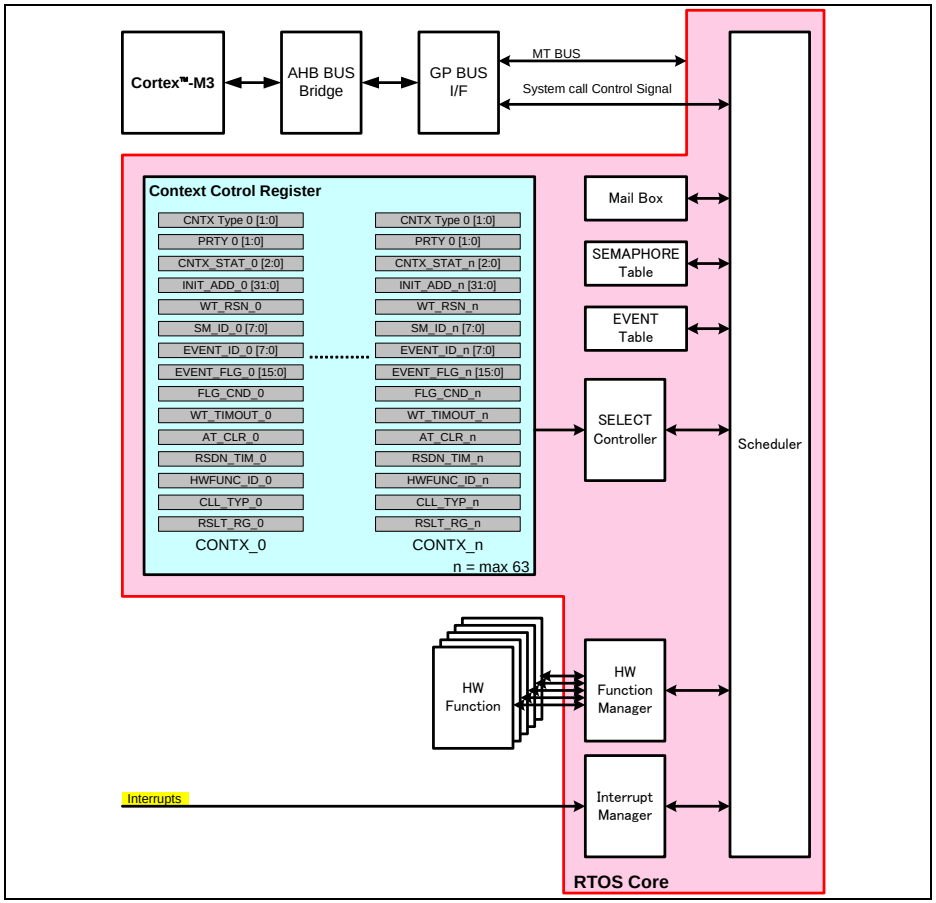

Figure3.1 Structure of Hardware Real-time OS

14. 3.20 Hardware Real-time OS

QINT description modified. “3.20.2 Service Calls” deleted. (p.65-66) continued

Rev3.01:

3.20.2 Service Calls

Rev4.00:

No descriptions

15. 4.6 Terminal Capacity Values

“4.6 Terminal Capacity Values”, added. (p.72)

Rev3.01:

No descriptions

Rev4.00:

4.6 Terminal Capacity Values

表 4.9 Terminal Capacity Values

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Input Buffer	C_B	5.0	-	7.0	pF
Output Buffer		5.0	-	7.0	pF
I/O Buffer		5.0	-	7.0	pF

16. 4.8.1(1) Input clock characteristics

MIN/MAX characteristics of CCI_CLK2_097M signal, modified. (p.74)

Rev3.01:

4.8.1 Clock Signals
(1) Input clock characteristics

Parameter	Symbol	Conditions	MIN	MAX	Unit
XT1, XT2	t_{SYSCLK}	-	25 ± 50ppm		MHz
ETH0_TXC, ETH1_TXC	t_{TXC}	-	-	25	MHz
ETH0_RXC, ETH1_RXC	t_{RXC}	-	-	125	MHz
CCM_CLK80M	t_{CCLCLK}	-	80 ± 50ppm		MHz
CLK2_097M	$t_{CCLIECLK}$	-	2.097 ± 100ppm		MHz
HBUSCLK	$t_{HBUSCLK}$	-	-	50	MHz
CSISCK0, CSISCK1	$t_{CSISSCK}$	Slave mode	-	16.6	MHz
TCK	t_{TCK}	-	-	50.	MHz

Rev4.00:

4.8.1 Clock Signals
(1) Input clock characteristics

Parameter	Symbol	Conditions	MIN	MAX	Unit
XT1, XT2	t_{SYSCLK}	-	25 ± 50ppm		MHz
ETH0_TXC, ETH1_TXC Note	t_{TXC}	-	-	25	MHz
ETH0_RXC, ETH1_RXC Note	t_{RXC}	-	-	125	MHz
CCM_CLK80M	t_{CCLCLK}	-	80 ± 50ppm		MHz
CCI_CLK2_097M Note	$t_{CCLIECLK}$	-	2.097152 ± 100ppm		MHz
HBUSCLK	$t_{HBUSCLK}$	-	-	50	MHz
CSISCK0, CSISCK1	$t_{CSISSCK}$	Slave mode	-	16.6	MHz
TCK	t_{TCK}	-	-	50.	MHz

Note. These signals apply to R-IN32M3-CL only.

* Applicable item except yellow hatched is unificated description.

17. 4.8.3 External Memory Interface Signals

Note1 for WREN register (Figure4.4, 4.5), modified. Timing Diagram of asynchronous memory (Figure4.6, 4.7), modified. (p.78-82)

Rev3.01:

(a) Read timing

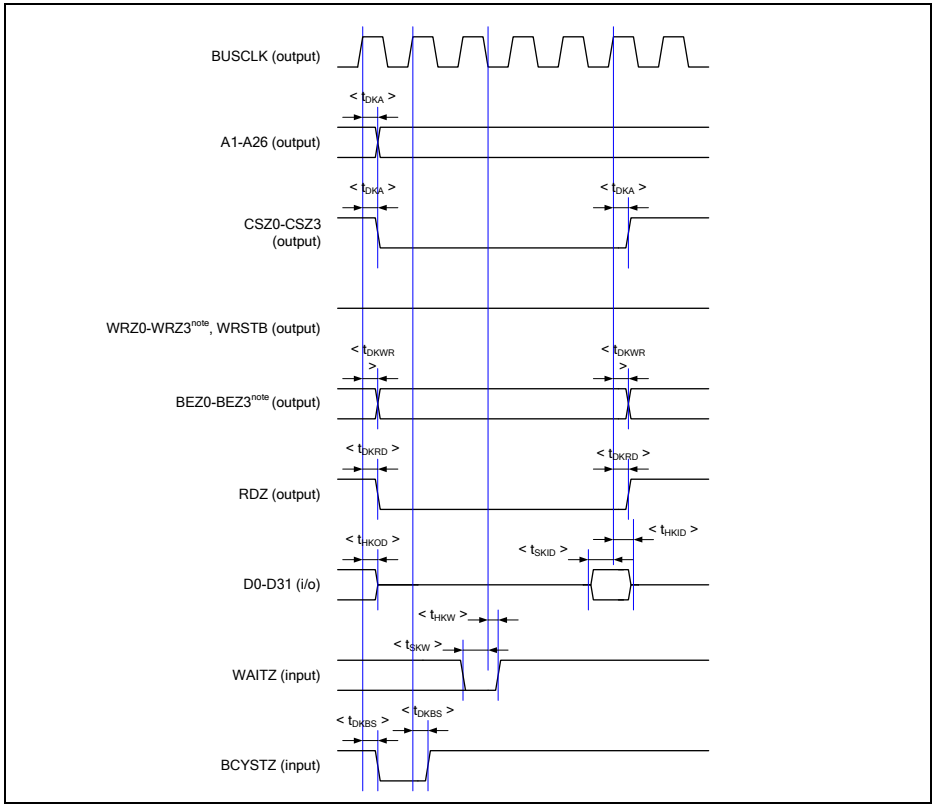

Figure4.4 Memory controller read timing diagram (asynchronous memory)

Note WRZ0-WRZ3 and BENZ0-BENZ3 serve a dual purposes; the function is selected by the WREN registers.

Remark The timing diagram in Figure 4.4 shows the case for when “Idle Wait”, “Write Recovery Wait”, and “Address Wait” are set to 0, and “Data Wait” is set to 3.

Rev4.00:

(a) Read timing

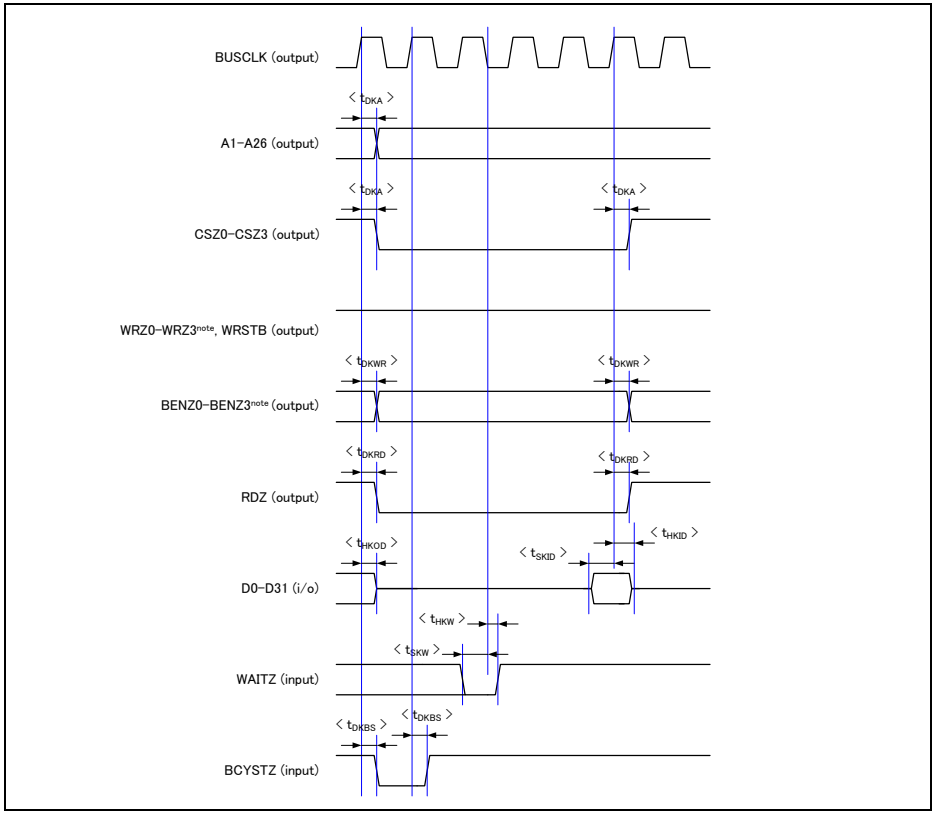

Figure4.4 Memory controller read timing diagram (asynchronous memory)

Note WRZ0-WRZ3 and BENZ0-BENZ3 serve a dual purposes; the function is selected by the WREN registers. For details see section 9.3.5, Write Enable Switch Registers (WREN), in the R-IN32M3 Series User’s Manual: Peripherals.

Remark The timing diagram in Figure 4.4 shows the case for when “Idle Wait”, “Write Recovery Wait”, and “Address Wait” are set to 0, and “Data Wait” is set to 3.

17. 4.8.3 External Memory Interface Signals

Note1 for WREN register (Figure4.4, 4.5), modified. Timing Diagram of asynchronous memory (Figure4.6, 4.7), modified. (p.78-82) continued

Rev3.01:

(b) Write timing

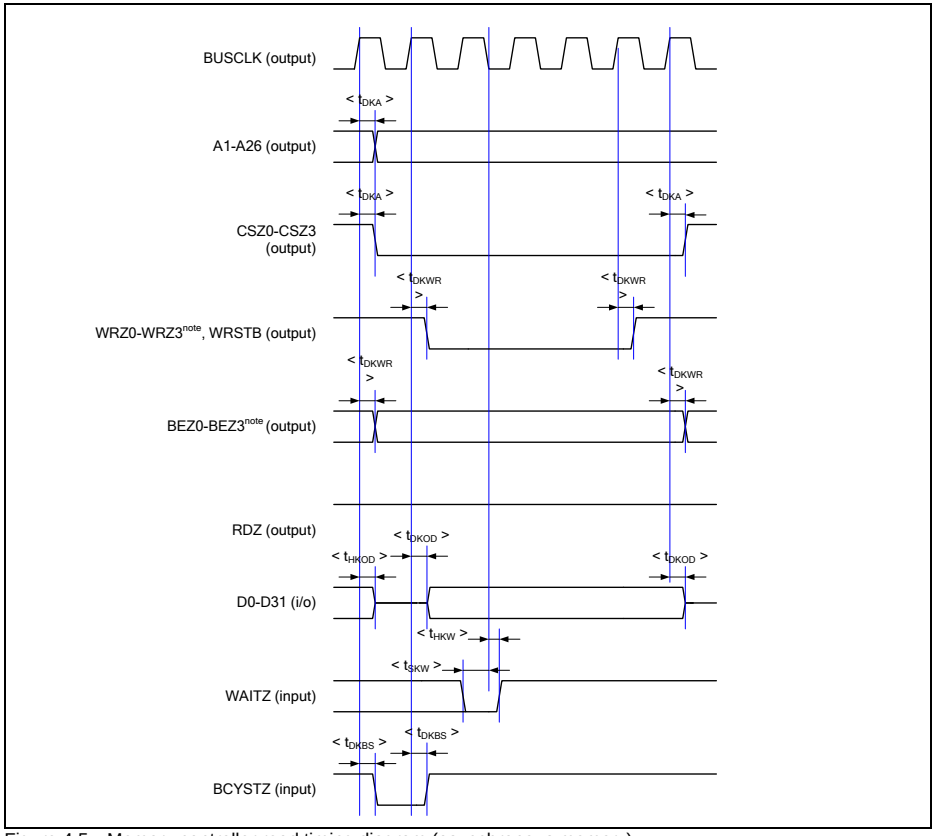

Figure 4.5 Memory controller read timing diagram (asynchronous memory)

Note WRZ0-WRZ3 and BENZ0-BENZ3 serve a dual purposes; the function is selected by the WREN registers.

Remark The timing diagram in Figure 4.4 shows the case for when “Idle Wait”, “Write Recovery Wait”,, and “Address Wait” are set to 0, and “Data Wait” is set to 3.

Rev4.00:

(b) Write timing

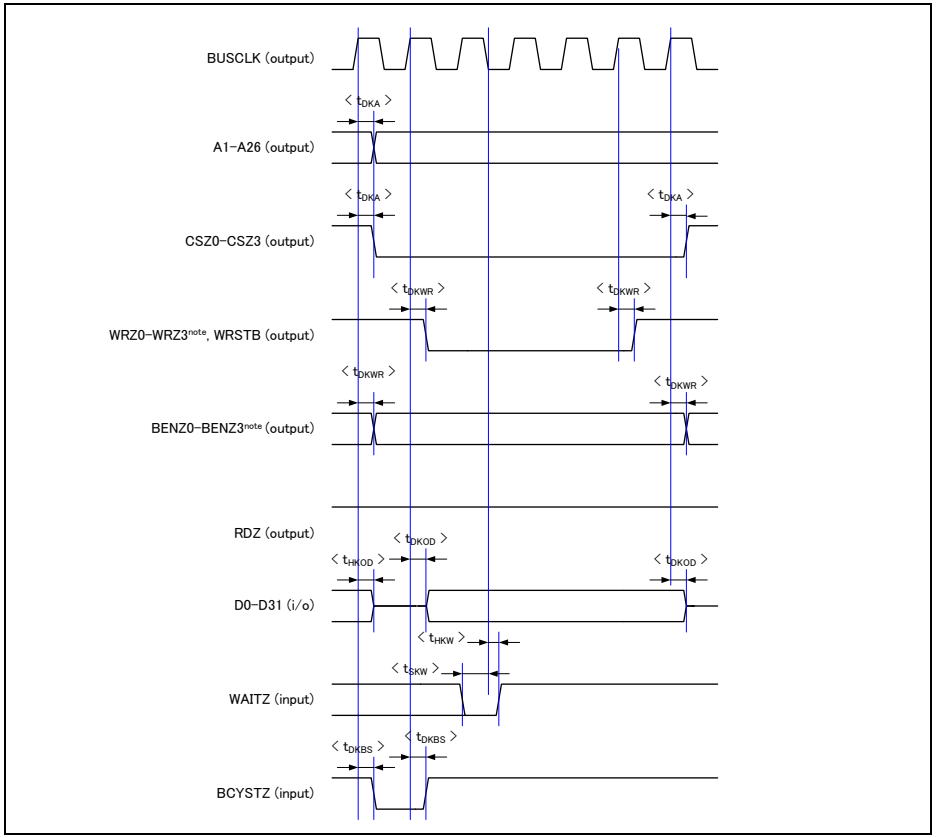

Figure4.5 Memory controller read timing diagram (asynchronous memory)

Note WRZ0-WRZ3 and BENZ0-BENZ3 serve a dual purposes; the function is selected by the WREN registers. For details see section 9.3.5, Write Enable Switch Registers (WREN), in the R-IN32M3 cSeries User's Manual: Peripherals.

Remark The timing diagram in Figure 4.4 shows the case for when “Idle Wait”, “Write Recovery Wait”,, and “Address Wait” are set to 0, and “Data Wait” is set to 3.

17. 4.8.3 External Memory Interface Signals

Note1 for WREN register (Figure4.4, 4.5), modified. Timing Diagram of asynchronous memory (Figure4.6, 4.7), modified. (p.78-82) continued

Rev3.01:

(a) Read timing

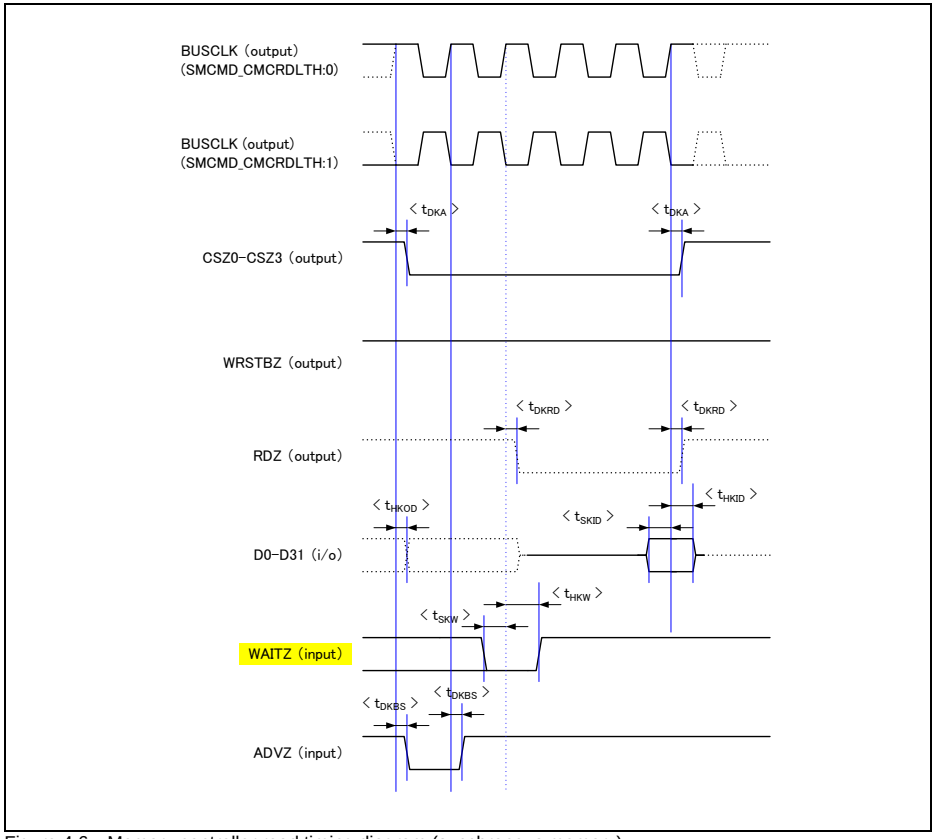

Figure 4.6 Memory controller read timing diagram (synchronous memory)

Remark Above timing is for the case where "t_ceoe" is 2 and "t_rc" is 4.

Rev4.00:

(a) Read timing

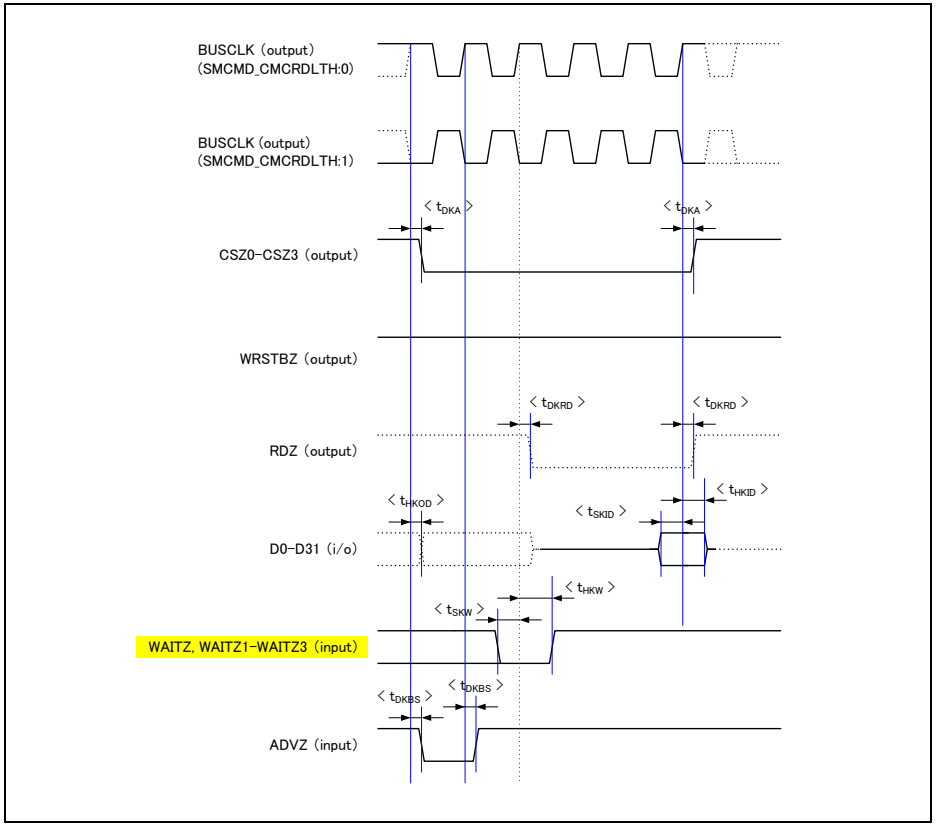

Figure 4.6 Memory controller read timing diagram (synchronous memory)

Remark Above timing is for the case where "t_ceoe" is 2 and "t_rc" is 4.

17. 4.8.3 External Memory Interface Signals

Note1 for WREN register (Figure4.4, 4.5), modified. Timing Diagram of asynchronous memory (Figure4.6, 4.7), modified. (p.78-82) continued

Rev3.01:

(a) Write timing

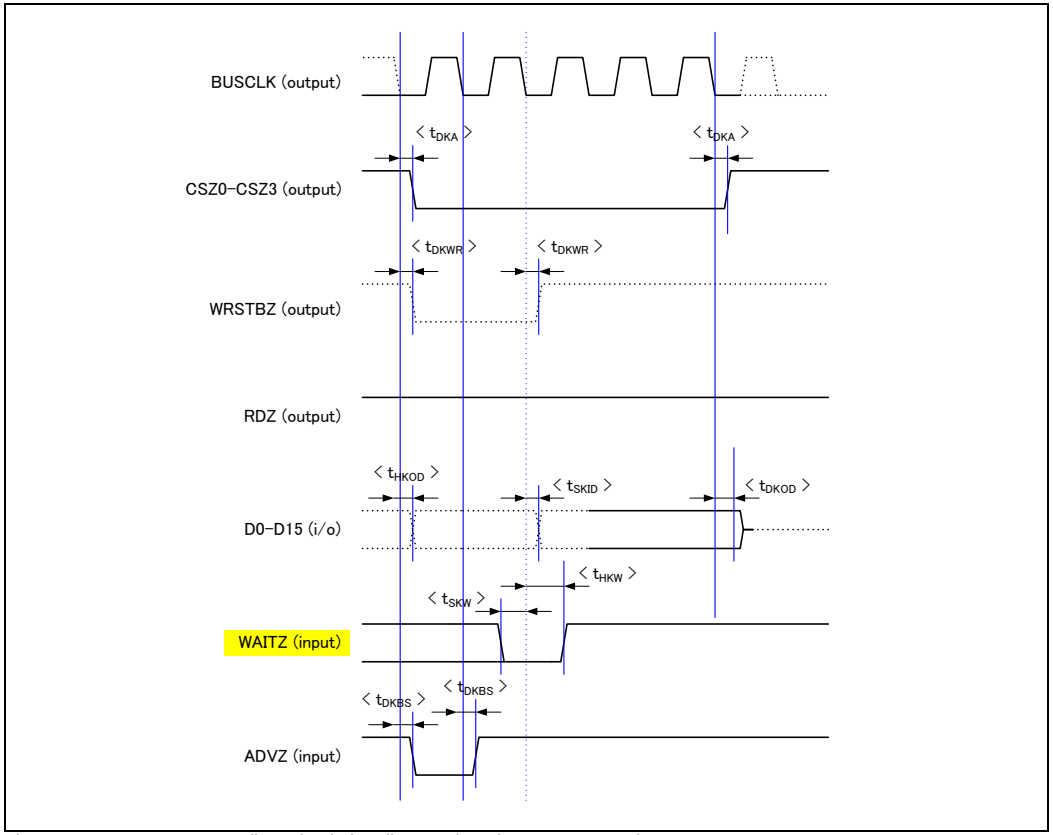

Figure 4.7 Memory controller write timing diagram (synchronous memory)

Remark Above timing is for the case where "t_ceoe" is 2 and "t_rc" is 4.

Rev4.00:

(a) Write timing

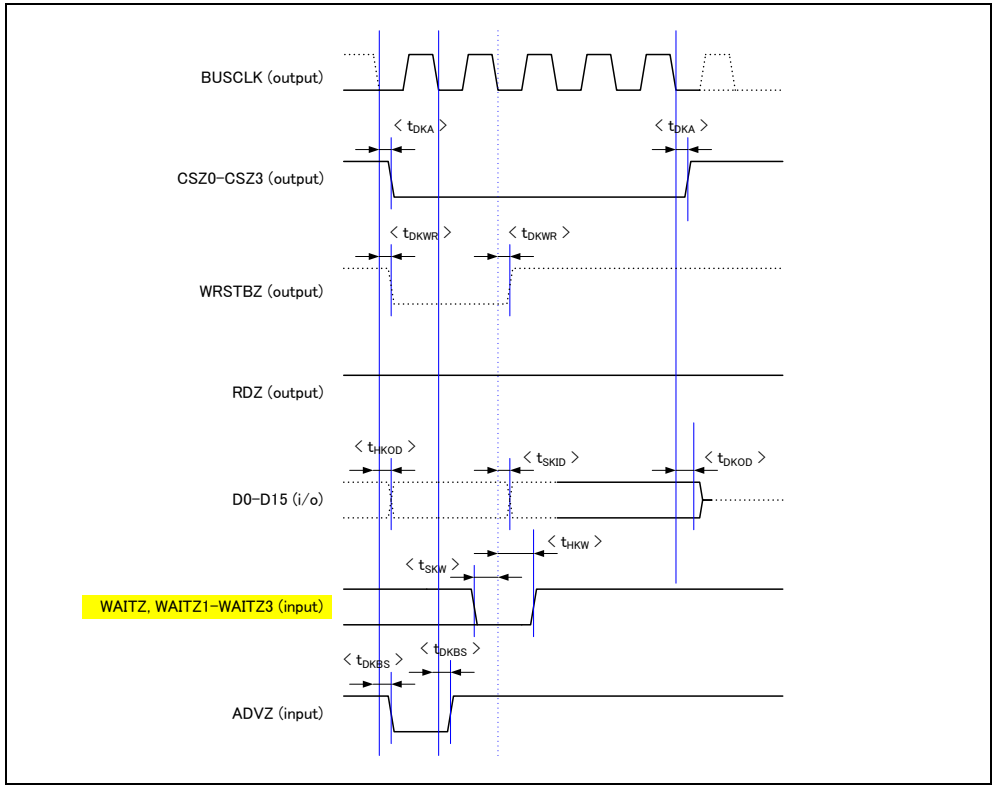

Figure 4.7 Memory controller write timing diagram (synchronous memory)

Remark Above timing is for the case where "t_ceoe" is 2 and "t_rc" is 4.

18. 4.8.6 External DMA Interface

“Parameter” and “Symbol” for DMA acknowledge signals output low level width, modified. Note2 modified. (p.100)

Rev3.01:

4.7.6 External DMA Interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
DMAREQZn, RTDMAREQZ input setup time (to BUSCLK↑)	t_{SKDR}	-	7.0	-	ns
DMAREQZn, RTDMAREQZ input hold time 1	t_{HKDR1}	-	Until DMAACKZn↓, RTDMAACKZ↓	-	ns
DMAREQZn, REDMAREQZ input hold time 2 (from BUSCLK↑)	t_{HKDR2}	-	-	t_{BUSCLK} Note1 × m Note2 - 7.0	ns
DMAACKZn, RTDMACKZ output delay time (from BUSCLK↑)	t_{DKDA}	C_L = 30pF	2.0	10.0	ns
DMAACKZn, RTDMAACKZ output high level width	t_{WDAH}	-	t_{BUSCLK} Note1 × m Note2 - 8	t_{BUSCLK} Note1 × m Note2 + 8	ns
DMATCZn, RTDMATCZ output delay time (from BUSCLK↑)	t_{DKTC}	C_L = 30pF	2.0	10.0	ns

Note1, t_{BUSCLK} is one cycle (10 ns) of BUSCLK.
Note2, n = 0-1, m = 1-31 (DMAIFC0, DMAIFC1, RTMDAIFC registers).

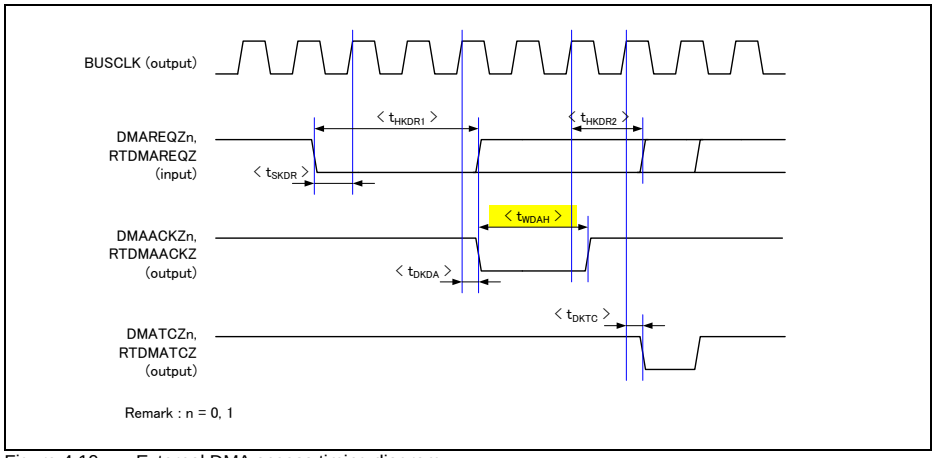

Figure 4.19 External DMA access timing diagram

Rev4.00:

4.7.6 External DMA Interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
DMAREQZn, RTDMAREQZ input setup time (to BUSCLK↑)	t_{SKDR}	-	7.0	-	ns
DMAREQZn, RTDMAREQZ input hold time 1	t_{HKDR1}	-	Until DMAACKZn↓, RTDMAACKZ↓	-	ns
DMAREQZn, REDMAREQZ input hold time 2 (from BUSCLK↑)	t_{HKDR2}	-	-	t_{BUSCLK} Note1 × m Note2 - 7.0	ns
DMAACKZn, RTDMACKZ output delay time (from BUSCLK↑)	t_{DKDA}	C_L = 30pF	2.0	10.0	ns
DMAACKZn, RTDMAACKZ output low level width	t_{WDAL}	-	t_{BUSCLK} Note1 × m Note2 - 8	t_{BUSCLK} Note1 × m Note2 + 8	ns
DMATCZn, RTDMATCZ output delay time (from BUSCLK↑)	t_{DKTC}	C_L = 30pF	2.0	10.0	ns

Note1, t_{BUSCLK} is one cycle (10 ns) of BUSCLK.
Note2, n = 0-1, m = 1-31 (DMAIFC0, DMAIFC1, RTMDAIFC registers).

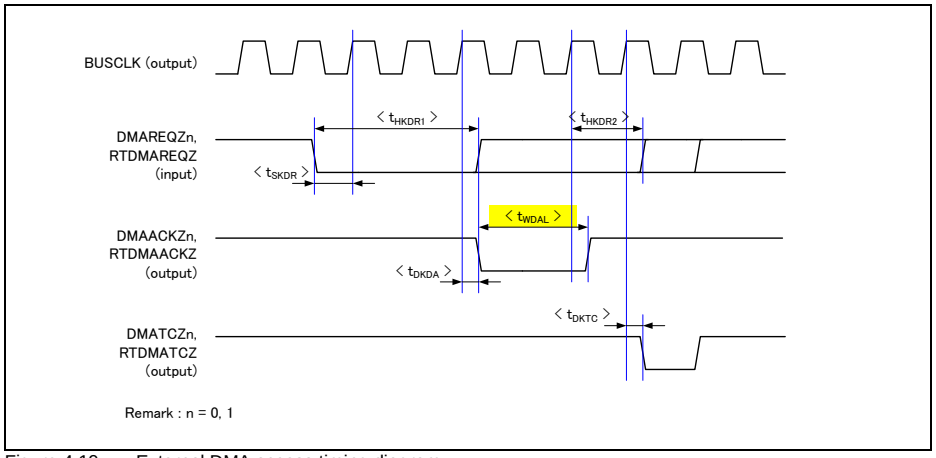

Figure 4.19 External DMA access timing diagram

* Applicable item except yellow hatched is description unification.

19. 4.8.7 CSI INterface

Characteristics for CSISCKn output high/low level width, added. Remark added. (p.101-102)

Rev3.01:

(1) Master mode

Parameter	Symbol	Conditions	MIN	MAX	Unit
CSISCKn output cycle	$t_{CSIMSCK}$	C_L = 15pF	40	-	ns
CSISIn input setup time (to CSISCKn↑)	t_{SMSI}	-	8.5	-	ns
CSISIn input setup time (to CSISCKn↓)	t_{SMSI}	-	8.5	-	ns
CSISIn input hold time (from CSISCKn↑)	t_{HMSI}	-	7.0	-	ns
CSISIn input hold time (from CSISCKn↓)	t_{HMSI}	-	7.0	-	ns
CSISOn output delay time (from CSISCKn↑)	t_{DMSO}	C_L = 15pF	-	7.0	ns
CSISOn output delay time (from CSISCKn↓)	t_{DMSO}		-	7.0	ns
CSISOn output hold time (from CSISCKn↑)	t_{HMSO}		$t_{CSIMSCK}$ × 0.5 - 5.0	-	ns
CSISOn output hold time (from CSISCKn↓)	t_{HMSO}		$t_{CSIMSCK}$ × 0.5 - 5.0	-	ns

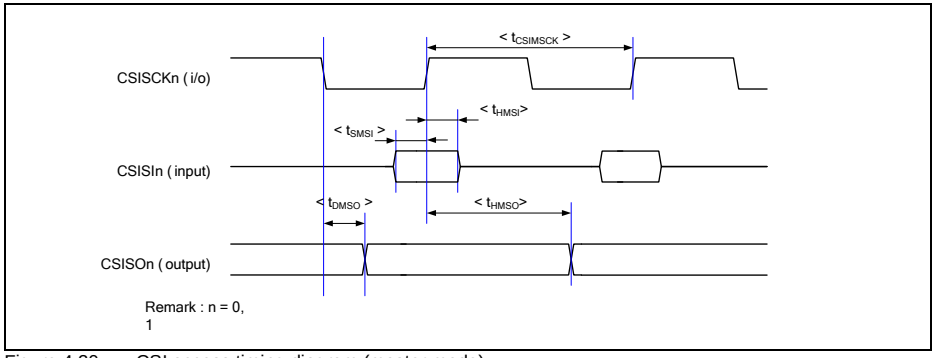

Figure 4.20 CSI access timing diagram (master mode)

Rev4.00:

(1) Master mode

Parameter	Symbol	Conditions	MIN	MAX	Unit
CSISCKn output cycle	$t_{CSIMSCK}$	C_L = 15pF	40	-	ns
CSISCKn output high level width	t_{WSKH}	C_L = 15pF	$t_{CSIMSCK}$×0.5 – 5.0	-	ns
CSISCKn output low level width	t_{WSKL}	C_L = 15pF	$t_{CSIMSCK}$×0.5 – 5.0	-	ns
CSISIn input setup time (to CSISCKn↑)	t_{SMSI}	-	8.5	-	ns
CSISIn input setup time (to CSISCKn↓)	t_{SMSI}	-	8.5	-	ns
CSISIn input hold time (from CSISCKn↑)	t_{HMSI}	-	7.0	-	ns
CSISIn input hold time (from CSISCKn↓)	t_{HMSI}	-	7.0	-	ns
CSISOn output delay time (from CSISCKn↑)	t_{DMSO}	C_L = 15pF	-	7.0	ns
CSISOn output delay time (from CSISCKn↓)	t_{DMSO}		-	7.0	ns
CSISOn output hold time (from CSISCKn↑)	t_{HMSO}		$t_{CSIMSCK}$ × 0.5 - 5.0	-	ns
CSISOn output hold time (from CSISCKn↓)	t_{HMSO}		$t_{CSIMSCK}$ × 0.5 - 5.0	-	ns

Remark n = 0, 1

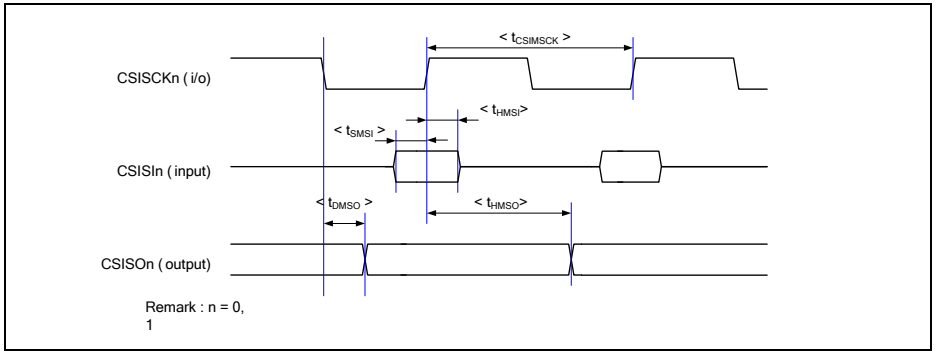

Figure 4.20 CSI access timing diagram (master mode)

Remark The timing diagram in Figure 4.20 shows the case for when "Data Output from CSISCKn ↓ " and "Data Input to CSISCKn ↑ ". See the timing diagram according to the operating mode.

19. 4.8.7 CSI INterface

Characteristics for CSISCKn output high/low level width, added. Remark added. (p.101-102) continued

Old:

(2) Slave mode

Parameter	Symbol	Conditions	MIN	MAX	Unit
CSISCKn input cycle	$t_{CSISSCK}$	-	60	-	ns
CSISIn input setup time (to CSISCKn↑)	t_{SSSI}	-	10.0	-	ns
CSISIn input setup time (to CSISCKn↓)	t_{SSSI}	-	10.0	-	ns
CSISIn input hold time (from CSISCKn↑)	t_{HSSI}	-	15	-	ns
CSISIn input hold time (from CSISCKn↓)	t_{HSSI}	-	15	-	ns
CSISOn output delay time (from CSISCKn↑)	t_{DSSO}	C_L = 15pF	-	10.0	ns
CSISOn output delay time (from CSISCKn↓)	t_{DSSO}		-	10.0	ns
CSISOn output hold time (from CSISCKn↑)	t_{HSSO}		$t_{CSISSCK}$ × 0.5 - 5.0	-	ns
CSISOn output hold time (from CSISCKn↓)	t_{HSSO}		$t_{CSISSCK}$ × 0.5 - 5.0	-	ns

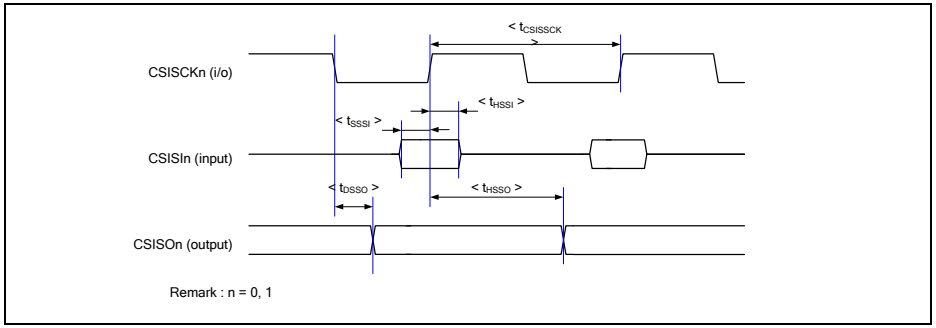

Figure 4.21 CSI access timing diagram (slave mode)

Rev4.00:

(2) Slave mode

Parameter	Symbol	Conditions	MIN	MAX	Unit
CSISCKn input cycle	$t_{CSISSCK}$	-	60	-	ns
CSISCKn output high level width	t_{WSKH}	-	$t_{CSIMSCK}$×0.5 – 5.0	-	ns
CSISCKn output low level width	t_{WSKL}	-	$t_{CSIMSCK}$×0.5 – 5.0	-	ns
CSISIn input setup time (to CSISCKn↑)	t_{SSSI}	-	10.0	-	ns
CSISIn input setup time (to CSISCKn↓)	t_{SSSI}	-	10.0	-	ns
CSISIn input hold time (from CSISCKn↑)	t_{HSSI}	-	15	-	ns
CSISIn input hold time (from CSISCKn↓)	t_{HSSI}	-	15	-	ns
CSISOn output delay time (from CSISCKn↑)	t_{DSSO}	C_L = 15pF	-	10.0	ns
CSISOn output delay time (from CSISCKn↓)	t_{DSSO}		-	10.0	ns
CSISOn output hold time (from CSISCKn↑)	t_{HSSO}		$t_{CSISSCK}$ × 0.5 - 5.0	-	ns
CSISOn output hold time (from CSISCKn↓)	t_{HSSO}		$t_{CSISSCK}$ × 0.5 - 5.0	-	ns

Remark n = 0, 1

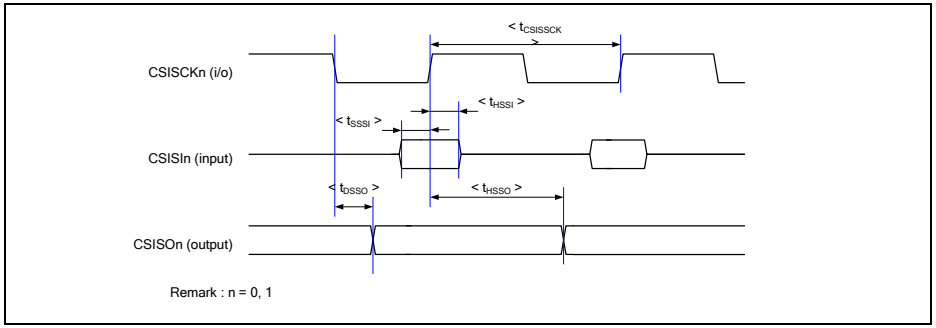

Figure 4.21 CSI access timing diagram (slave mode)

Remark The timing diagram in Figure 4.20 shows the case for when "Data Output from CSISCKn ↓ " and "Data Input to CSISCKn ↑ ". See the timing diagram according to the operating mode.

20. 4.8.10 Ethernet Interface (R-IN32M3-CL only)

Pin Name of ETHn_TXDm, ETHn_RXDm signals, modified (p.105-106)

Rev3.01:

(1) GMII interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
ETHn_GTXC output cycle	t_{GTXC}	C_L = 13pF	8	-	ns
ETHn_RXC input cycle	t_{GRXC}	-	8	-	ns
ETHn_TXDm output delay time (from ETHn_GTXC↑)	t_{DGTKTD}	C_L = 13pF	0.5	5.5	ns
ETHn_TXEN, ETHn_TXER output delay time (from ETHn_GTXC↑)	t_{DGTKTE}	C_L = 13pF	0.5	5.5	ns
ETHn_RXD input setup time (to ETHn_RXC↑)	t_{SGRDRK}	-	2.0	-	ns
ETHn_RXD input hold time (from ETHn_RXC↑)	t_{HGRDRK}	-	0	-	ns
ETHn_RXDV, ETHn_RXER input setup time (to ETHn_RXC↑)	t_{SGRVRK}	-	2.0	-	ns
ETHn_RXDV, ETHn_RXER input hold time (from ETHn_RXC↑)	t_{HGRVRK}	-	0	-	ns

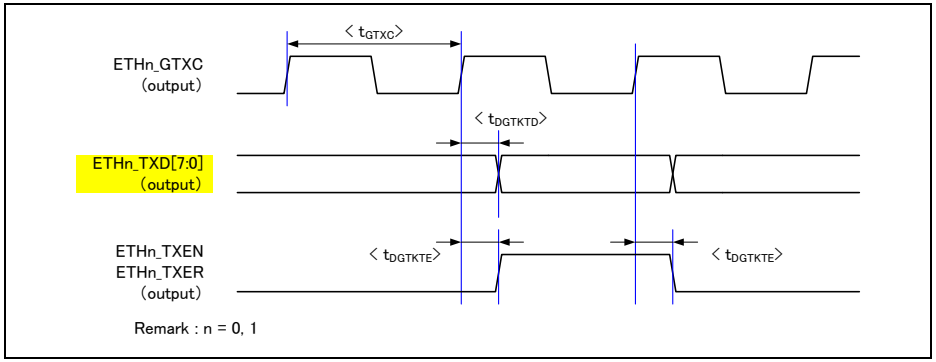

Figure 4.25 Ethernet access timing diagram (GMII transmission)

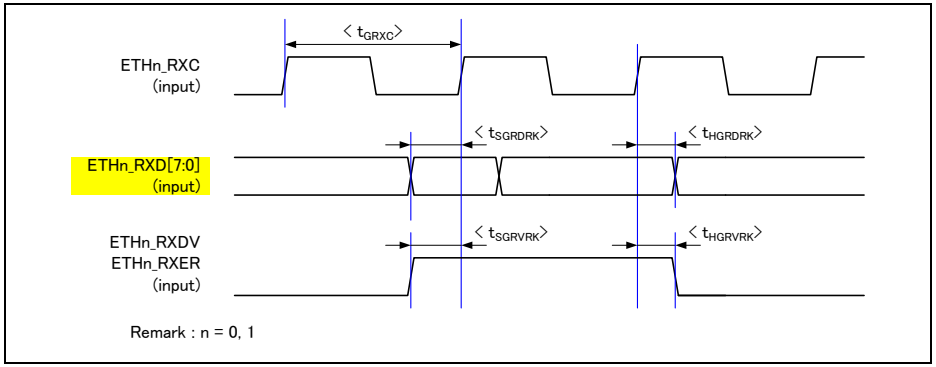

Figure 4.26 Ethernet access timing diagram (GMII reception)

Rev4.00:

(1) GMII interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
ETHn_GTXC output cycle	t_{GTXC}	C_L = 13pF	8	-	ns
ETHn_RXC input cycle	t_{GRXC}	-	8	-	ns
ETHn_TXDm output delay time (from ETHn_GTXC↑)	t_{DGTKTD}	C_L = 13pF	0.5	5.5	ns
ETHn_TXEN, ETHn_TXER output delay time (from ETHn_GTXC↑)	t_{DGTKTE}	C_L = 13pF	0.5	5.5	ns
ETHn_RXDm input setup time (to ETHn_RXC↑)	t_{SGRDRK}	-	2.0	-	ns
ETHn_RXDm input hold time (from ETHn_RXC↑)	t_{HGRDRK}	-	0	-	ns
ETHn_RXDV, ETHn_RXER input setup time (to ETHn_RXC↑)	t_{SGRVRK}	-	2.0	-	ns
ETHn_RXDV, ETHn_RXER input hold time (from ETHn_RXC↑)	t_{HGRVRK}	-	0	-	ns

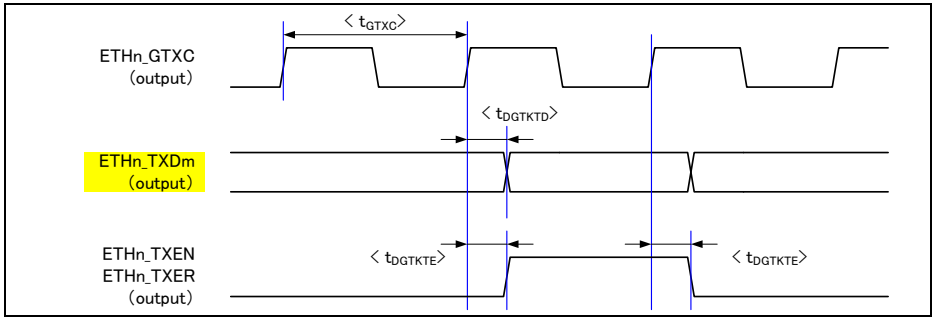

Figure 4.25 Ethernet access timing diagram (GMII transmission)

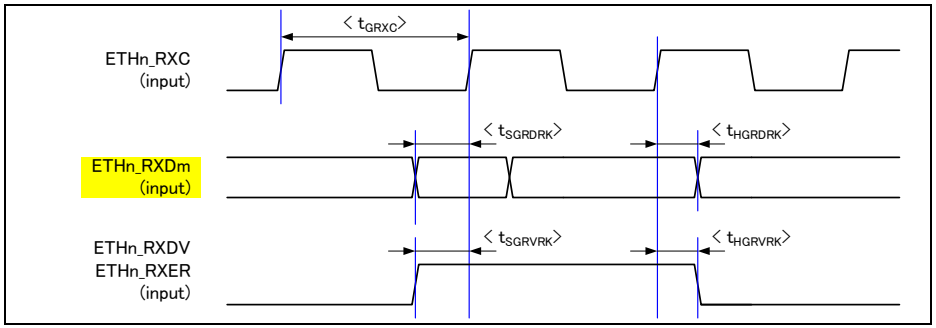

Figure 4.26 Ethernet access timing diagram (GMII reception)

Remark n = 0, 1, m = 0-7

20. 4.8.10 Ethernet Interface (R-IN32M3-CL only)

Pin Name of ETHn_TXDm, ETHn_RXDm signals, modified (p.105-106) continued

Rev3.01:

(2) MII interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
ETHn_TXC input cycle	t_{TXC}	-	40	-	ns
ETHn_RXC input cycle	t_{RXC}	-	40	-	ns
ETHn_TXDm output delay time	t_{DTKTD}	C_L = 30pF	0	25	ns
ETHn_TXEN, ETHn_TXER output delay time	t_{DTKTE}	C_L = 30pF	0	25	ns
ETHn_RXD input setup time	t_{SRDRK}	-	10	-	ns
ETHn_RXD input hold time	t_{HRDRK}	-	10	-	ns
ETHn_RXDV, ETHn_RXER input setup time	t_{SRVRK}	-	10	-	ns
ETHn_RXDV, ETHn_RXER input hold time	t_{HRVRK}	-	10	-	ns

Remark n = 0, 1, m = 0-7

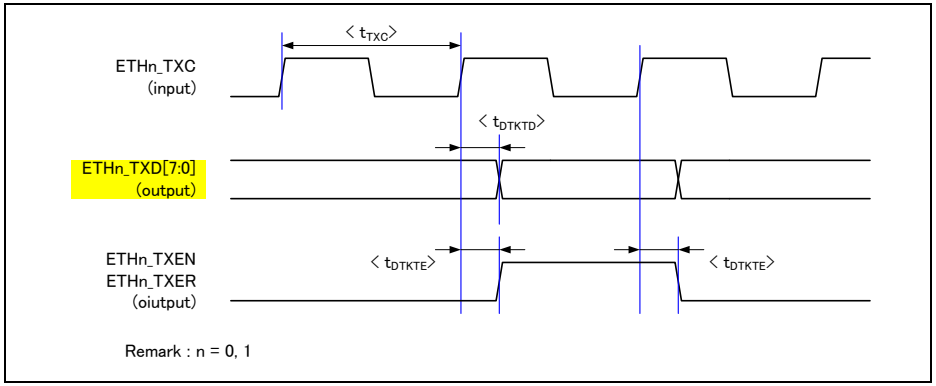

Figure 4.27 Ethernet access timing diagram (MII transmission)

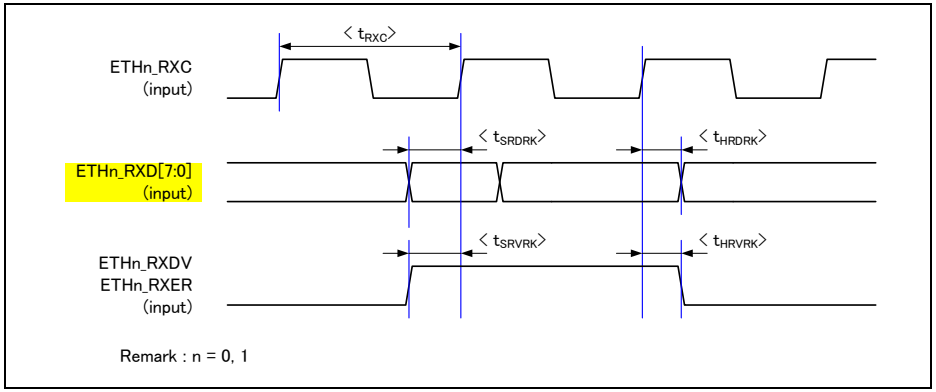

Figure 4.28 Ethernet access timing (MII reception)

Rev4.00:

(2) MII interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
ETHn_TXC input cycle	t_{TXC}	-	40	-	ns
ETHn_RXC input cycle	t_{RXC}	-	40	-	ns
ETHn_TXDm output delay time (from ETHn_TXC↑)	t_{DTKTD}	C_L = 30pF	0	25	ns
ETHn_TXEN, ETHn_TXER output delay time (from ETHn_TXC↑)	t_{DTKTE}	C_L = 30pF	0	25	ns
ETHn_RXDm input setup time (to ETHn_RXC↑)	t_{SRDRK}	-	10	-	ns
ETHn_RXDm input hold time (from ETHn_RXC↑)	t_{HRDRK}	-	10	-	ns
ETHn_RXDV, ETHn_RXER input setup time (to ETHn_RXC↑)	t_{SRVRK}	-	10	-	ns
ETHn_RXDV, ETHn_RXER input hold time (from ETHn_RXC↑)	t_{HRVRK}	-	10	-	ns

Remark n = 0, 1, m = 0-7

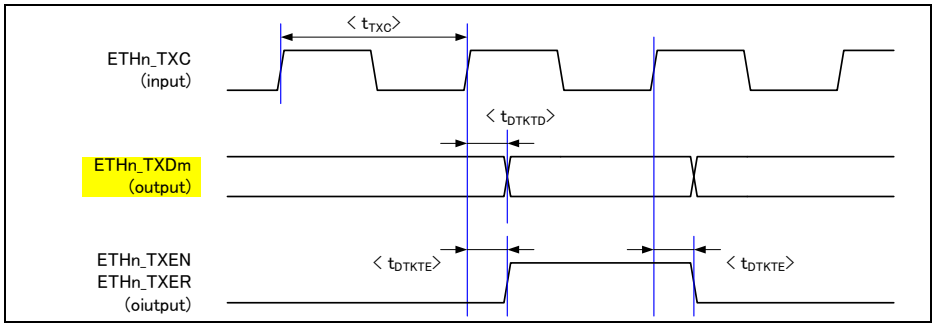

Figure 4.27 Ethernet access timing diagram (MII transmission)

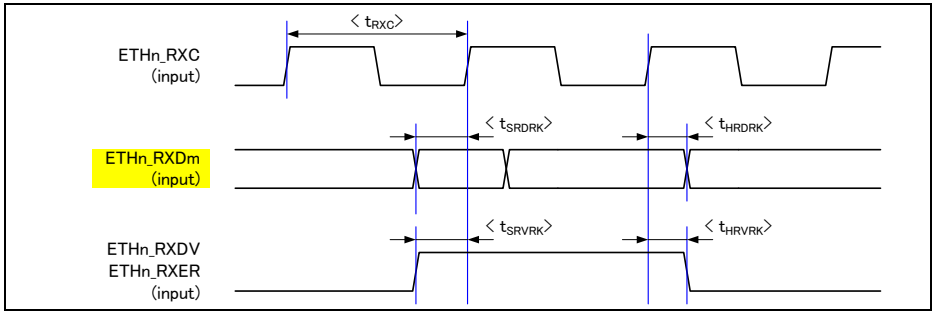

Figure 4.28 Ethernet access timing (MII reception)

Remark n = 0, 1, m = 0-7

21. 4.8.11(2) Trace interface

Characteristics of TRACEDATA output delay time, modified. (p.107)

Rev3.01:

(2) Trace interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
TRACECLK output frequency	t_{TRCCLK}	C_L = 15pF	20	-	ns
TRACEDATA output delay time	$t_{DTRCDAT}$	C_L = 15pF	0.26	3.43	ns

Rev4.00:

(2) Trace interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
TRACECLK output frequency	t_{TRCCLK}	C_L = 15pF	20	-	ns
TRACEDATA output delay time (from TRACECLK)	$t_{DTRCDAT}$	C_L = 15pF	0.26	8.43	ns